V370PDC Rev. A0

High Performance PCI SDRAM Controller with Integrated Peripheral Control Unit

- Fully compliant with PCI 2.2 specification target interface
- Multiplexed or Non-multiplexed 8-, 16-, or 32-bit generic peripheral bus interface
- Support up to 1 Gbyte of SDRA
- Support up to 2 single banks or 1 dual bank industrial standard 168-pin PC SDRAM DIMM
- Support up to 1Kbyte of burst access from PCI
- Up to 5 programmable chip select for peripheral strobe generation
- Large On-Chip FIFOs using V3's unique *DYNAMIC BANDWIDTH ALLOCATION™* architectu e
- Buffered PCI clock output
- Hot Swap Ready (PICMG™ Hot Swap Specification)
- Implementation of PCI Bus Power Management Interface Specification Version 1.0
- Initialization through PCI or serial EEPRO
- Programmable PCI and local interrupt management
- Two 32-bit General Purpose Timers
- Up to 66 MHz local bus clock with asynchronous PCI clock up to 33MHz
- 3.3V operation with 5V tolerant inputs
- Industrial Temperature Range (-40C to +85C)
- Low cost 160-pin PQFP package

The V370PDC PCI SDRAM Controller simplifies the design of PCI based memory sub-systems. System designers can replace many lower integration support components wit this single, high-integration device saving design time, board area, and manufacturing cost.

The V370PDC from V3 Semiconductor is a high performance PCI SDRAM Controller with integrated peripheral control unit operating at up to 66 MHz local bus speed. It features multiple address translation units from PCI which allow designers the freedom to customize their local address space. Access latency of slower peripherals are absorbed through the large On-Chip FIFOs.

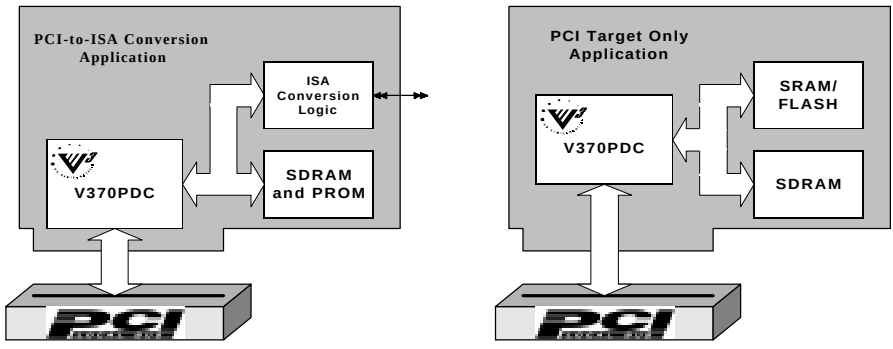
The peripheral bus provides low latency access t SDRAM. The peripheral control unit on the V370PDC also performs address decoding and chip-select strobes generation for SRAM, PROM and other slow peripherals. The peripheral bus can also be tri-stated through a simple hand-shaking protocol to allow other local bus masters control of the bus.

The SDRAM Controller connects the PCI bus through on-chip FIFOs to SDRAM arrays of up to 1 Gbytes in size. The fully programmable SDRAM controller also supports the use of Enhanced SDRAM to achiev even greater performance. Burst accesses of up to 1 Kbyte from PCI is supported.

The two general purpose 32-bit timers can be individually configured as a pulse width modulator, or used in other modes such as retriggerable or one-shot. Interrupts for a real time OS can be easily generated by the system heartbeat timer. A watchdog timer is also provided for graceful recovery from catastrophic program failures. Interrupt requests for all on-chip peripherals are managed by the Interrupt Control Unit. Additionally, off-chip interrupts can b routed to the Interrupt Control Unit.

The V370PDC is packaged in a low-cost 160-pin EIJA Plastic Quad Flat Pack (PQFP), and is available i 66MHz speed grade.

TYPICAL APPLICATIO



This document contains the product codes, pinout, package mechanical information, DC characteristics, and AC characteristics for the V370PDC. Detailed functional information is contained in the User's Manual.

V3 Semiconductor retains the rights to change documentation, specifications, or devic functionality at any time without notice. Please verify that you have the latest copy of all documents before finalizing a design.

1.0 Product Codes

Table 1: Product Codes

Product Code	Package	Frequency
V370PDC-66 REV A0	160-pin EIAJ PQFP	66MHz

2.0 Pin Description

Table 2 below lists the pin types found on the V370PDC. Table 3 describes the function of each pin on the V370PDC.

Table 2: Pin Types

Pin Type	Description
PCI I	PCI input only pin.
PCI O	PCI output only pin.
PCI I/O	PCI tri-state I/O pin.
PCI I/OD	PCI input with open drain output.
I/O_8	TTL I/O pin with 8mA output drive.
I/OD	TTL input with open drain output.
I	TTL input only pin.
O_2	TTL output pin with 2mA output drive.
O_8	TTL output pin with 8mA output drive.
O_{12}	TTL output pin with 12mA output drive.

Table 3: Signal Descriptions

PCI Bus Interface			
Signal	**Type**	**R[a]**	**Description**
AD[31:0]	PCI I/O	Z	Address and data, multiplexed on the same pins.
C/$\overline{\text{BE}}$[3:0]	PCI I		Bus Command and Byte Enables, multiplexed on the same pins.
PAR	PCI I/O	Z	Parity represents even parity across AD[31:0] and C/$\overline{\text{BE}}$[3:0].
$\overline{\text{FRAME}}$	PCI I		Cycle Frame indicates the beginning and burst length of an access.
$\overline{\text{IRDY}}$	PCI I		Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction.
$\overline{\text{TRDY}}$	PCI O	Z	Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction.
$\overline{\text{STOP}}$	PCI O	Z	Stop indicates the current target is requesting the master to stop the current transaction (retry or disconnect).
$\overline{\text{DEVSEL}}$	PCI O	Z	Device Select, when actively driven by a target, indicates the driving device has decoded its address as the target of the current access.
IDSEL	PCI I		Initialization Device Select is used as a chip select during configuration read and write transactions. It must be driven high in orde to access the chip's internal configuration space.
$\overline{\text{PERR}}$	PCI I/O	Z	Parity Error is used to report data parity errors during all PCI transactions except a Special Cycle.
$\overline{\text{SERR}}$	PCI I/OD	Z	System Error is used to report address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic.
PCLK	PCI I		PCLK provides timing for all transactions on the PCI bus.
SDRAM and Peripheral Bus Interface			
Signal	**Type**	**R**	**Description**
CLKIN	I		Local clock input
CLKOUT	O_{12}	X	Buffered PCI clock output
$\overline{\text{DCS}}$[3:0]	O_8	Z	SDRAM Chip Select
MA[14:0]	O_{12}	Z	SDRAM Memory Address (also, A[16:2] for peripheral access). MA[14:13] are typically used for BA[1:0]
$\overline{\text{RAS}}$	O_{12}	Z	SDRAM Row Address Strobe

Table 3: Signal Descriptions (cont'd)

$\overline{CAS}$	O_{12}	Z	SDRAM Column Address Strobe
$\overline{MWE}$	O_{12}	Z	SDRAM Memory Write Enable
MAD[31:0]	I/O_8	Z	SDRAM and peripheral bus data
$\overline{DQM}$[3:0]	O_8	Z	SDRAM Data Mask (these act as $\overline{MBE}$[3:0], A[1:0] for peripheral access)
MARB_IN	I		Peripheral bus arbitration input: Treated as bus request input when V370PDC is the primary bus master. When V370PDC is the secondary bus master, this input acts as bus grant.
MARB_OUT	O_8	0	Peripheral bus arbitration output: Treated as bus grant output when V370PDC is the primary bus master. When V370PDC is the secondary bus master, this output acts bus request.
ALE	O_8	Z	Address Latch Enable: used to latch the address on MAD[31:0] during the address phase of a peripheral bus access.
$\overline{ADS}$	O_8	Z	Asserted low to indicate the beginning of a bus cycle.
$\overline{BLAST}$	O_8	Z	Burst last.
$\overline{READY}$	I		Data ready.
WNR	O_8	Z	Write/$\overline{Read}$.
SDA	I/OD	Z	Serial EEPROM Data
SCL	O_2	Z	Serial EEPROM Clock
IOC[11:0]	I/O_8	Z	Multi-purpose I/O that can be configured for many functions
$\overline{INT}$[3:0]	I/O_8	Z	General purpose interrupt inputs/outputs: may be used for either PCI or local processor interrupts
Mode and Reset			
Signal	**Type**	**R**	**Description**
$\overline{RSTIN}$	I		Reset Input: Active low reset input used to initialize all internal functions of the chip.
$\overline{RSTOUT}$	O_8	0	Reset Output: Driven active when the input reset is driven active. Driven inactive when the RSTOUT bit in the system register is set. The $\overline{RSTOUT}$ signal is synchronous to the rising edge of CLKIN.
$\overline{CH}$	I		PCI Precharge Bias: This signal is driven low to activate the on-chip precharge bias for use in PICMG Hot Swap applications. Non-Hot Swap applications should pull this signal high.

Table 3: Signal Descriptions (cont'd)

MODE	I		MODE Input: selects mastership of V370PDC: 0 = Secondary master 1 = Primary master
Power and Ground Signals			
Signal	**Type**	**R**	**Description**
V_{CC}	-		POWER leads for external connection to a 3.3V V_{CC} board plane.
GND	-		GROUND leads for external connection to a GND board plane.
NC	-		No connect.

a. **R** indicates state during reset.

2.1 Pinout

Table 4 lists the pins by pin number. Figure 1 shows the pinout for the 160-pin EIAJ PQFP package and Figure 2 shows the mechanical dimensions of the package

Table 4: Pin Assignments

PIN #	Signal	PIN #	Signal	PIN #	Signal	PIN #	Signal
1	RSTIN	41	Vcc	81	Vcc	121	Vcc
2	PCLK	42	AD14	82	MAD9	122	MA5
3	GND	43	AD13	83	MA13	123	MAD27
4	Vcc	44	AD12	84	MAD10	124	MA4
5	NC	45	AD11	85	MA12	125	MAD28
6	CH	46	AD10	86	MAD11	126	MA3
7	AD31	47	AD9	87	MA11	127	MAD29
8	AD30	48	AD8	88	MAD12	128	MAD30
9	AD29	49	C_BE0	89	MA10	129	MAD31
10	AD28	50	MODE	90	GND	130	GND
11	AD27	51	GND	91	MAD13	131	MA2
12	AD26	52	AD7	92	IOC11	132	MA1
13	AD25	53	AD6	93	MAD14	133	MA0
14	AD24	54	AD5	94	IOC10	134	IOC3
15	GND	55	AD4	95	MAD15	135	IOC2
16	C_BE3	56	AD3	96	IOC9	136	READY
17	IDSEL	57	AD2	97	MAD16	137	MARB_OUT
18	AD23	58	AD1	98	IOC8	138	MARB_IN
19	AD22	59	AD0	99	MAD17	139	ADS
20	Vcc	60	Vcc	100	Vcc	140	Vcc
21	AD21	61	GND	101	GND	141	GND
22	AD20	62	MAD0	102	MA9	142	CLKIN
23	AD19	63	DCS0	103	MAD18	143	IOC1
24	AD18	64	MAD1	104	MA8	144	IOC0
25	AD17	65	DCS1	105	MAD19	145	DQM3
26	AD16	66	MAD2	106	MA7	146	DQM2
27	GND	67	DCS2	107	MAD20	147	DQM1
28	C_BE2	68	MAD3	108	MA6	148	DQM0
29	FRAME	69	DCS3	109	MAD21	149	BLAST
30	IRDY	70	MAD4	110	GND	150	WNR
31	TRDY	71	GND	111	MAD22	151	GND
32	DEVSEL	72	MAD5	112	IOC7	152	CLKOUT
33	STOP	73	MWE	113	MAD23	153	RSTOUT
34	PERR	74	MAD6	114	IOC6	154	ALE
35	SERR	75	CAS	115	MAD24	155	SDA
36	PAR	76	MAD7	116	IOC5	156	SCL
37	Vcc	77	RAS	117	MAD25	157	INT0
38	C_BE1	78	MAD8	118	IOC4	158	INT1
39	AD15	79	MA14	119	MAD26	159	INT2
40	GND	80	GND	120	GND	160	INT3

Figure : Pinout for 160-pin EIAJ PQFP (top view)

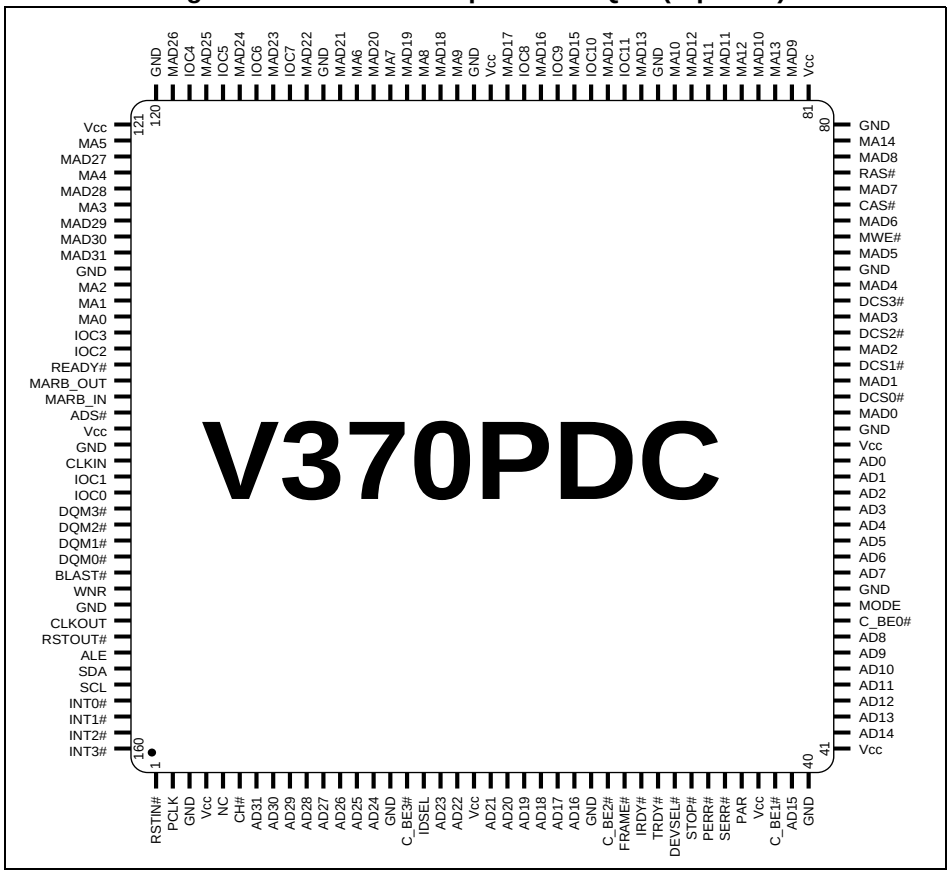
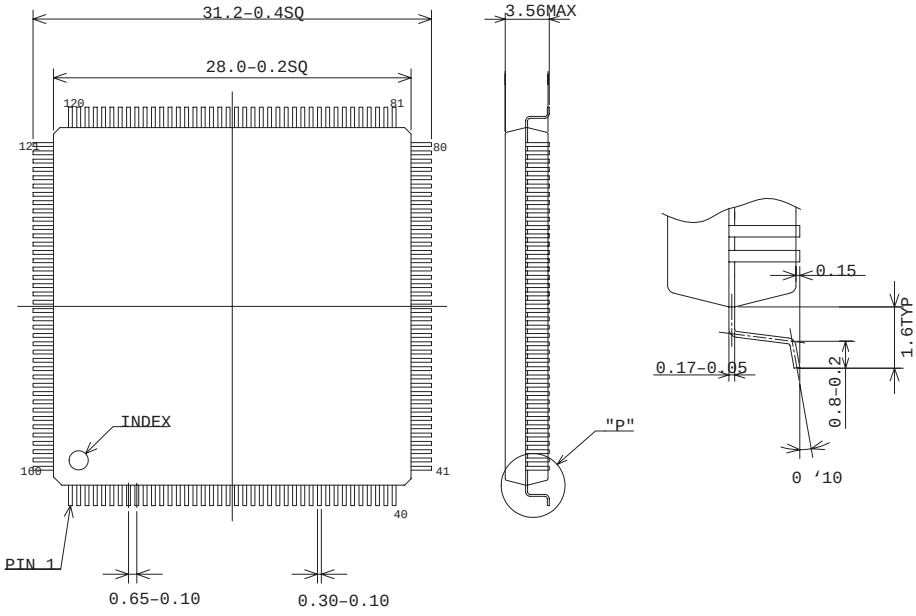


Figure 2: 160-pin EIAJ PQFP mechanical details



3.0 DC Specifications

The DC specifications for the PCI bus signals match exactly those given in the PCI Specification, Rev. 2.2 Section 4.2.1.1. For more information on the PCI DC specifications, see the PCI Specification.

Table 5: Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage	-0.3 to +3.6	V
V_{IN}	DC input voltage	-0.3 to 6.0	V
I_{OUT}	DC output current	TBA	mA
T_{STG}	Storage temperature range	-55 to +125	°C

Table 6: Guaranteed Operating Conditions

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage	3.0 to 3.6	V
Theta Ja	Thermal resistance	TBA	°C/w
T_A	Ambient temperature range	-40 to +85	°C

3.1 PCI Bus DC Specifications

Table 7: PCI Bus Signals DC Operating Specifications

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{IH}	Input high voltage		$0.5V_{CC}$	V_{CC} + 0.5	V	
V_{IL}	Input low voltage		-0.5	$0.3V_{CC}$	V	
I_{IH}	Input high leakage current		$0.7V_{CC}$		µA	1
I_{IL}	Input low leakage current	$0 < V_{IN} < V_{CC}$		$\pm$10	µA	1
V_{OH}	Output high voltage	I_{OUT} = -500µA	$0.9V_{CC}$		V	
V_{OL}	Output low voltage	I_{OUT} = 1500µA		$0.1V_{CC}$	V	2
C_{IN}	Input pin capacitance			10	pF	3
C_{CLK}	PCLK pin capacitance		5	12	pF	
C_{IDSEL}	IDSEL pin capacitance			8	pF	4

Table 7: PCI Bus Signals DC Operating Specifications

Symbol	Parameter	Condition	Min	Max	Units	Notes
L_{PIN}	Pin inductance			20	nH	

Notes:
1. Input leakage currents include high impedance output leakage for all bi-directional buffers with tri-state outputs.
2. Signals without pull-up resistors have greater than 3mA low output current. Signals requiring pull resistors have greater than 6mA output current. The latter include FRAME, TRDY, IRDY, STOP, SERR, PERR.
3. Absolute maximum pin capacitance for a PCI unit is 10pF (except for CLK).
4. Lower capacitance on this input-only pin allows for non-resistive coupling to AD[xx].

3.2 Local Bus DC Specification

Table 8: Local Bus Signals DC Operating Specifications (V_{CC} = 3.3V± 0.3V)

Symbol	Parameter	Condition	Min	Max	Units
V_{IH}	Input high voltage		2.0		V
V_{IL}	Input low voltage			0.8	V
I_{IH}	Input high leakage current	$V_{IN} = V_{CC}$	-10	10	µA
I_{IL}	Input low leakage current	V_{IN}=GND	-10	10	µA
V_{OH}	Output high voltage	I_{OUT} = -2, -8, -12mA	2.4		V
V_{OL}	Output low voltage	I_{OUT} = 2, 8, 12mA		0.4	V
I_{OZL}	Low level float input leakage	V_{OL} = GND	-10	10	µA
I_{OZH}	High level float input leakage	$V_{OH} = V_{CC}$	-10	10	µA
I_{CC} (max)	Maximum supply current			TBA	mA
I_{CC} (typ)	Typical supply current			TBA	mA
C_{IO}	Input and output capacitance			TBA	pF

3.3 AC Specifications

The AC specifications for the PCI bus signals match exactly those given in the PCI Specification, Rev. 2.1, Section 4.2.1.2. For more information on the PCI AC specifications, including the V/I curves for 5V signalling, see section 4.2.1.2 of Rev 2.1 PCI Specification.

3.4 PCI Bus Timings

Table 9: PCI Bus Signals AC Operating Specifications

Symbol	Parameter	Condition	Min	Max	Units	Notes
$I_{OH(AC}$	Switching Current high	$0V< V_{OUT}\leq 0.3V_{CC}$	$-12V_{CC}$		mA	
		$0.3V_{CC}<V_{OUT}<0.9V$	$-17.1(V_{CC}-V_{OUT})$		mA	
		$0.7V_{CC}<V_{OUT}<V_{CC}$		Equation C		
	(Test point)	$V_{OUT} = 0.7V_{CC}$		$-32V_{CC}$		
$I_{OL(AC)}$	Switching Current low	$V_{CC} > V_{OUT} >0.6V_{CC}$	$16V_{CC}$		mA	
		$0.6V_{CC} > V_{OUT} >0.1V_{CC}$	$26.7V_{CC}$		mA	
	(Test point)	$V_{OUT}=0.18V_{CC}$		$38V_{CC}$	mA	
I_{CL}	Low clamp current	$-3V<V_{IN}<-1V$	$-25+(V_{IN}+1)/0.015$		mA	
t_R	Unloaded output rise time	$0.2V_{CC}$ to $0.6V_{CC}$	1	4	V/ns	
t_F	Unloaded output fall time	0.6V to 0.2V	1	4	V/ns	

3.5 Local Bus Timings

Table 10: Local Bus AC Test Conditions

Symbol	Parameter	Limits	Units
V_{CC}	Supply voltage 3.3 volt operation	3.0 to 3.60	V
V_{IN}	Input low and high voltages	0.4 and 2.0	V
C_{OUT}	Capacitive load on output and I/O pins	50	pF

Table 11: Capacitive Derating for Output and I/O Pins

Output Drive Limit	Supply voltage	Derating
8mA	3.3 volt	TBA
12mA	3.3 volt	TBA

Figure 3: Clock and Synchronous Signals

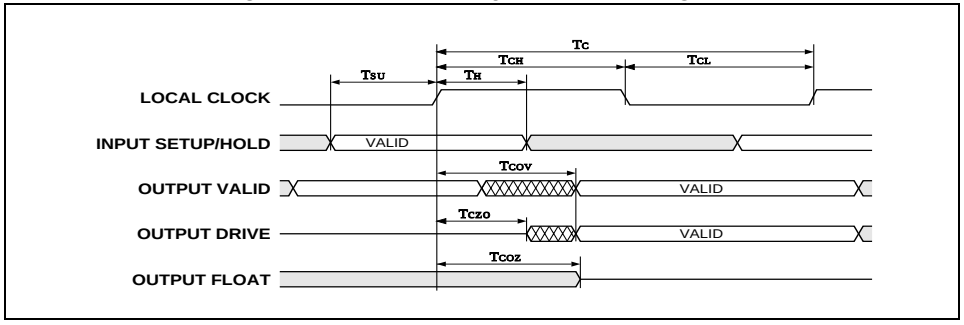


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Table 12: Local Bus Timing Parameters for Vcc =3.3 Volts +/- 5%

				66MHz		
#	Symbol	Description	Notes	Min	Max	Units
1	T_C	CLKIN period		15		ns
2	T_{CH}	CLKIN high time		5.5		ns
3	T_{CL}	CLKIN low time		5.5		ns
4	T_{SU}	Synchronous input setup		3		ns
4a	T_{SU}	Synchronous input setup ($\overline{\text{READY}}$)	1	TBA		ns
5	T_H	Synchronous input hold		1		ns
6	T_{COV}	CLKIN to output valid delay		3	11	ns
7	T_{CZO}	CLKIN to output driving delay		3	11	ns
8	T_{COZ}	CLKIN to high impedance delay		4	12	ns
9	T_{ALE}	ALE Pulse Width		T_{CH}+0.5	T_{CH}+1	ns
10	T_{CLH}	CLKIN rising to ALE rising		2	10	ns
11	T_{AH}	CLKIN falling to ALE falling		2	10	ns

Notes:
1. Applies only to $\overline{\text{READY}}$ pin when i960_RDY bit in LB_BUS_CFG register is set to '1'.

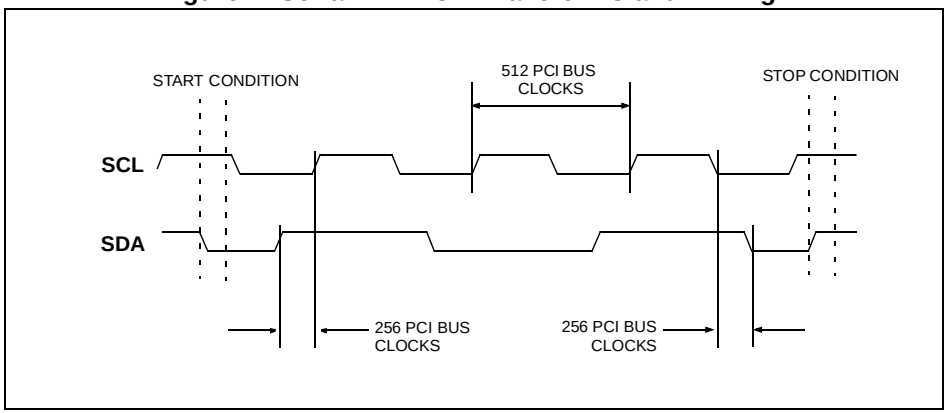
Table 13: PCI Bus Timing Parameters for Vcc = 3.3 Volts +/- 10%

#	Symbol	Description	Notes	Min	Max	Units
1	T_C	PCLK period		30		ns
2	T_{SU}	Synchronous input setup to PCLK	1	7		ns
3	T_H	Synchronous input hold from PCLK		0		ns
4	T_{COV}	PCLK to output valid delay	2	3	11	ns
5	T_{CZO}	PCLK to output driving delay		4	11	ns
6	T_{COZ}	PCLK to high impedance delay		5	18	ns
7	T_{RST}	Reset period when PRST used as input		$16 \cdot T_C$		

3.6 Serial EEPROM Port TImings

The clock for the serial EEPROM interface is derived by dividing the PCI bus clock. The waveforms generated are shown in Figure 4.

Figure 4: Serial EEPROM Waveforms and Timing



4.0 Revision History

Table 14: Revision Histo r

Revision Number	Date	Comments and Changes
0.8	01/99	First pre-silicon revision of preliminary data sheet.
0.9	03/99	Update Figure 2: Mechanical Drawing; Update Table 8: Local Bus Signals DC Operating Specifications; Update Table 10: Local Bus ACTest Conditions; Update Table 12: Local Bus Signals AC Operating Specifications.
1.0	03/99	Initial Release.

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