



# STQ2NK60ZR-AP STP2NK60Z - STD2NK60Z-1

N-CHANNEL 600V - 7.2Ω - 1.4A TO-220/TO-92/IPAK  
Zener-Protected SuperMESH™ MOSFET

**Table 1: General Features**

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>	P <sub>w</sub>
STQ2NK60ZR-AP	600 V	< 8 Ω	0.4 A	3 W
STP2NK60Z	600 V	< 8 Ω	1.4 A	45 W
STD2NK60Z-1	600 V	< 8 Ω	1.4 A	45 W

- TYPICAL R<sub>DS(on)</sub> = 7.2 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- ESD IMPROVED CAPABILITY
- 100% AVALANCHE TESTED
- NEW HIGH VOLTAGE BENCHMARK
- GATE CHARGE MINIMIZED

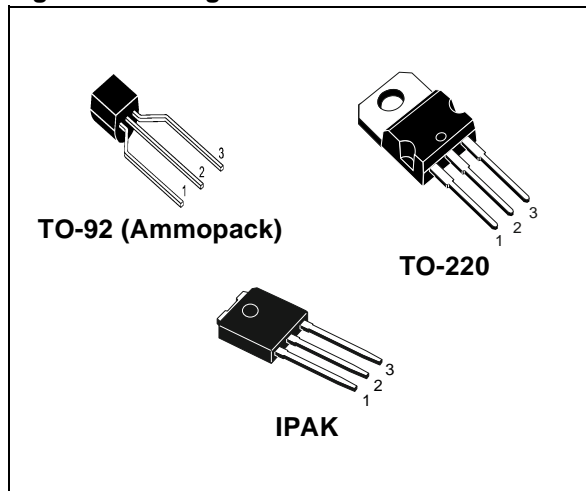
## DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

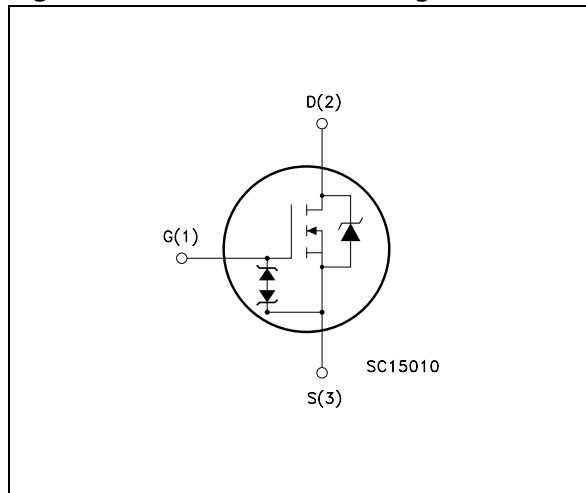
## APPLICATIONS

- LOW POWER BATTERY CHARGERS
- SWITCH MODE LOW POWER SUPPLIES(SMPS)
- LOW POWER, BALLAST, CFL (COMPACT FLUORESCENT LAMPS)

**Figure 1: Package**



**Figure 2: Internal Schematic Diagram**



**Table 2: Order Codes**

SALES TYPE	MARKING	PACKAGE	PACKAGING
STQ2NK60ZR-AP	Q2NK60ZR	TO-92	AMMOPAK
STP2NK60Z	P2NK60Z	TO-220	TUBE
STD2NK60Z-1	D2NK60Z	IPAK	TUBE

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Rev. 3

**Table 3: Absolute Maximum ratings**

Symbol	Parameter	Value		Unit
		TO-220 / IPAK	TO-92	
$V_{DS}$	Drain-source Voltage ( $V_{GS} = 0$ )	600		V
$V_{DGR}$	Drain-gate Voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	600		V
$V_{GS}$	Gate- source Voltage	$\pm 30$		V
$I_D$	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	1.4	0.4	A
$I_D$	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	0.77	0.25	A
$I_{DM}(\bullet)$	Drain Current (pulsed)	5.6	1.6	A
$P_{TOT}$	Total Dissipation at $T_C = 25^\circ\text{C}$	45	3	W
	Derating Factor	0.36	0.025	W/ $^\circ\text{C}$
$V_{ESD(G-S)}$	Gate source ESD (HBM-C= 100pF, R=1.5k $\Omega$ )	1500		V
dv/dt (1)	Peak Diode Recovery voltage slope	4.5		V/ns
$T_j$ $T_{stg}$	Operating Junction Temperature Storage Temperature	-55 to 150		$^\circ\text{C}$

( $\bullet$ ) Pulse width limited by safe operating area

(1)  $I_{SD} \leq 1.4\text{A}$ ,  $di/dt \leq 200\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_j \leq T_{JMAX}$ .

**Table 4: Thermal Data**

		TO-220 / IPAK	TO-92	Unit
Rthj-case	Thermal Resistance Junction-case Max	2.77	--	$^\circ\text{C}/\text{W}$
Rthj-amb	Thermal Resistance Junction-ambient Max	100	120	$^\circ\text{C}/\text{W}$
Rthj-lead	Thermal Resistance Junction-lead Max	--	40	$^\circ\text{C}/\text{W}$
$T_l$	Maximum Lead Temperature For Soldering Purpose	300	260	$^\circ\text{C}$

**Table 5: Avalanche Characteristics**

Symbol	Parameter	Max Value	Unit
$I_{AR}$	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by $T_j$ max)	1.4	A
$E_{AS}$	Single Pulse Avalanche Energy (starting $T_j = 25^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{V}$ )	90	mJ

**Table 6: Gate-Source Zener Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}$	Gate source Breakdown Voltage	$I_{gs} = \pm 1 \text{ mA}$ (Open Drain)	30			V

### PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

**ELECTRICAL CHARACTERISTICS** ( $T_{CASE} = 25^{\circ}C$  UNLESS OTHERWISE SPECIFIED)**Table 7: On/Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 1mA, V_{GS} = 0$	600			V
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}, T_C = 125^{\circ}C$			1 50	$\mu A$ $\mu A$
$I_{GSS}$	Gate-body Leakage Current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20V$			$\pm 10$	$\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 50 \mu A$	3	3.75	4.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10V, I_D = 0.7 A$		7.2	8	$\Omega$

**Table 8: Dynamic**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (1)$	Forward Transconductance	$V_{DS} = 15 V, I_D = 0.7 A$		1		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25V, f = 1 MHz, V_{GS} = 0$		170 27 5		pF pF pF
$C_{oss \text{ eq.}} (3)$	Equivalent Output Capacitance	$V_{GS} = 0V, V_{DS} = 0V \text{ to } 480V$		30		pF
$t_{d(on)}$ $t_r$ $t_{d(off)}$ $t_f$	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	$V_{DD} = 300 V, I_D = 0.65 A,$ $R_G = 4.7 \Omega, V_{GS} = 10 V$ (Resistive Load see, Figure 21)		8 30 22 55		ns ns ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 480V, I_D = 1.5 A,$ $V_{GS} = 10V$ (see, Figure 24)		7.7 1.7 4	10	nC nC nC

**Table 9: Source Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM} (2)$	Source-drain Current Source-drain Current (pulsed)				1.5 6	A A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 1.5 A, V_{GS} = 0$			1.6	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 1.3 A, di/dt = 100 A/\mu s$ $V_{DD} = 25V, T_j = 25^{\circ}C$ (see test circuit, Figure 22)		250 550 4.4		ns $\mu C$ A
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 1.3 A, di/dt = 100 A/\mu s$ $V_{DD} = 25V, T_j = 150^{\circ}C$ (see test circuit, Figure 22)		300 690 4.6		ns $\mu C$ A

(1) Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %.

(2) Pulse width limited by safe operating area.

(3)  $C_{oss \text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

Figure 3: Safe Operating Area For TO-220

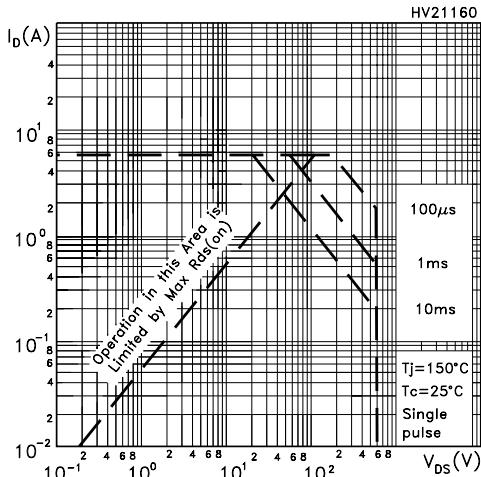


Figure 4: Safe Operating Area For IPAK

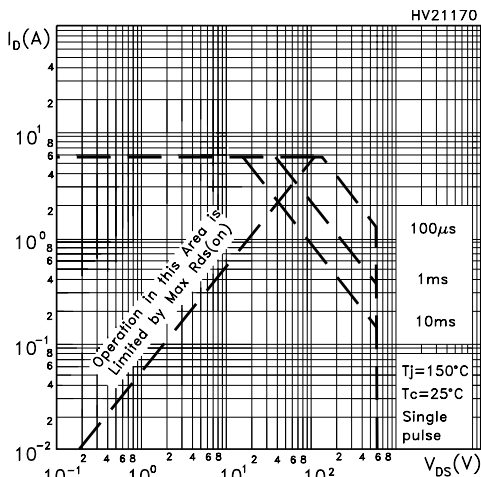


Figure 5: Safe Operating Area For TO-92

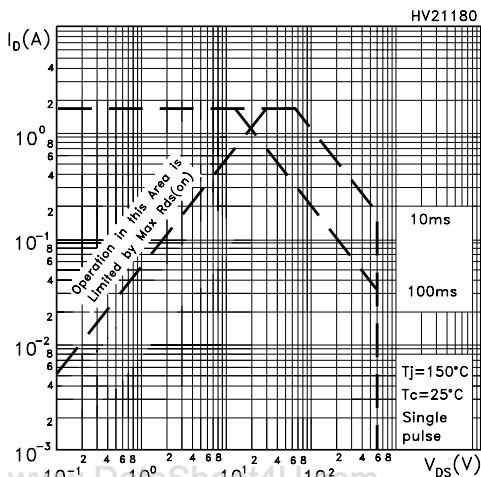


Figure 6: Thermal Impedance For TO-220

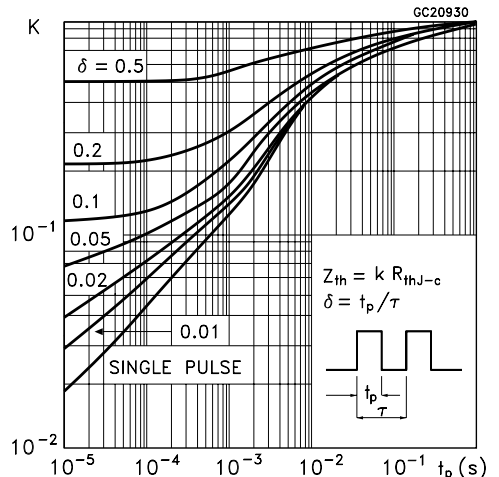


Figure 7: Thermal Impedance For IPAK

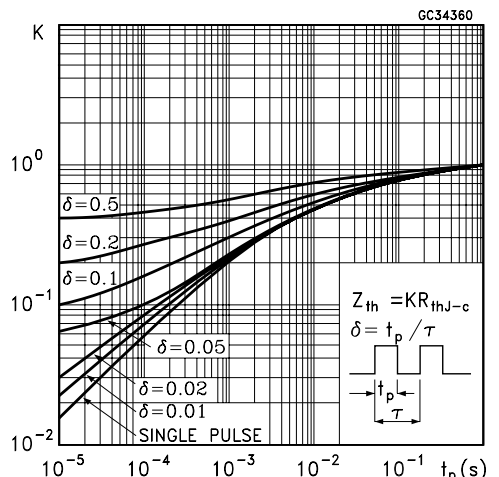


Figure 8: Thermal Impedance For TO-92

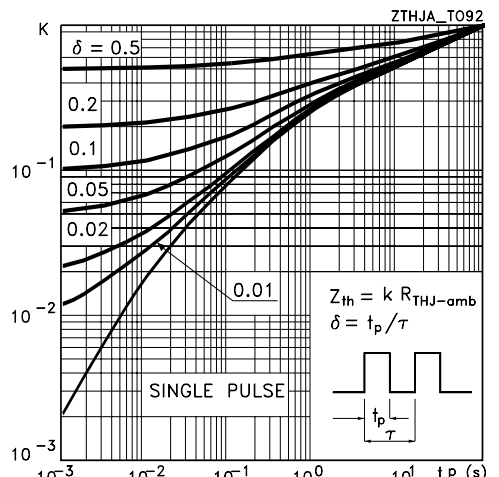


Figure 9: Output Characteristics

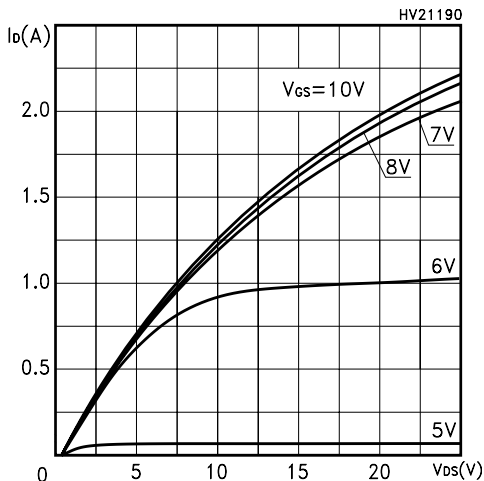


Figure 10: Transconductance

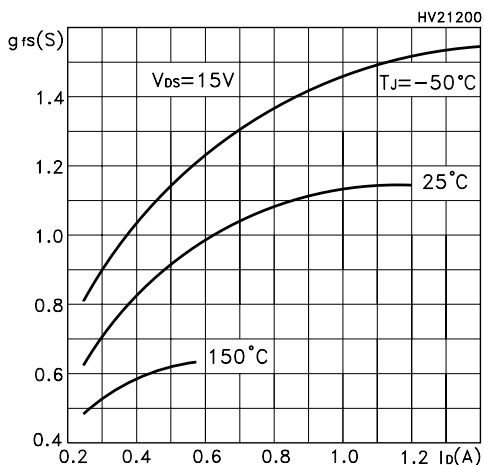


Figure 11: Gate Charge vs Gate-source Voltage

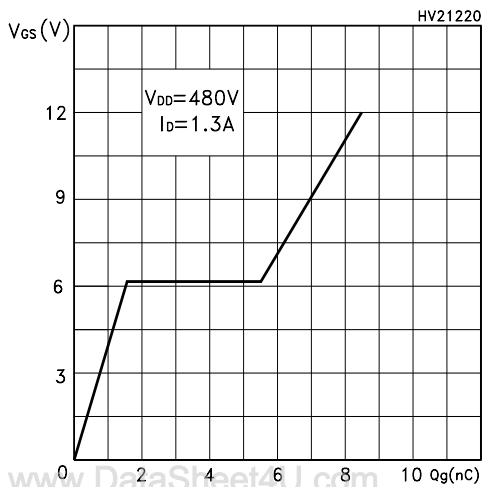


Figure 12: Transfer Characteristics

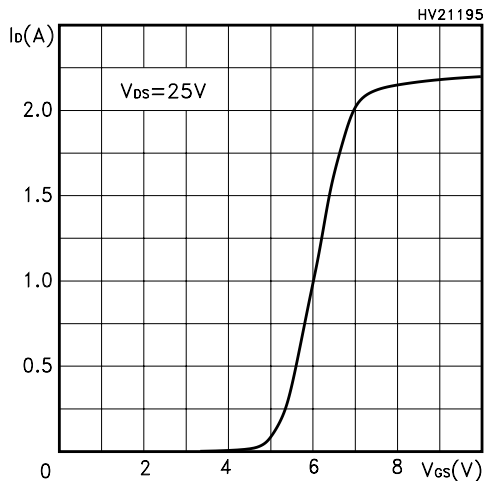


Figure 13: Static Drain-source On Resistance

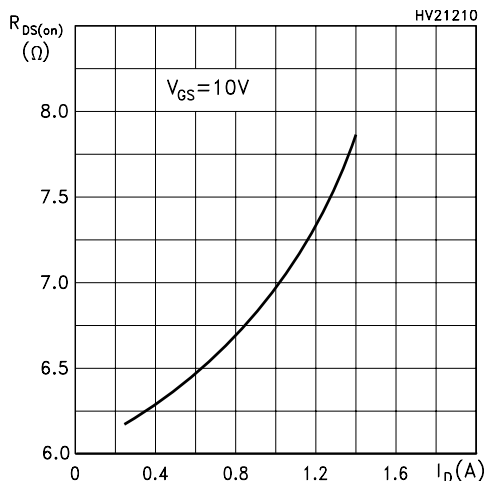
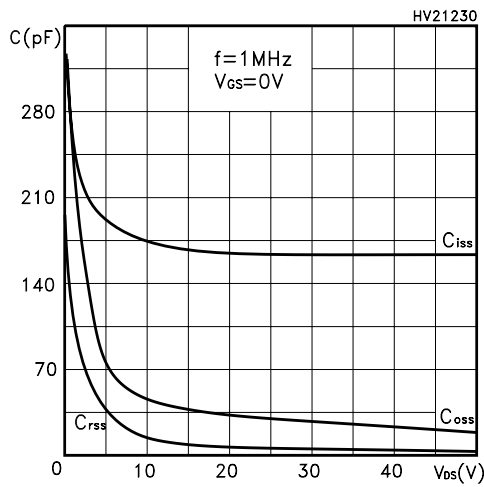


Figure 14: Capacitance Variations



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Figure 15: Normalized Gate Threshold Voltage vs Temperature

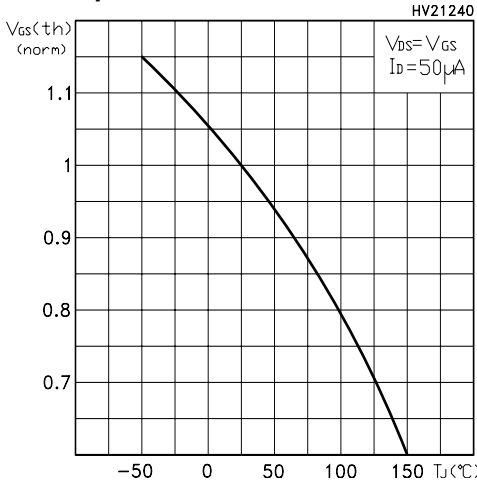


Figure 18: Normalized On Resistance vs Temperature

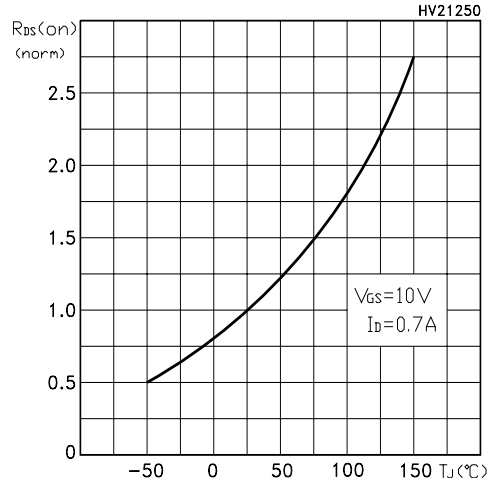


Figure 16: Source-Drain Forward Characteristics

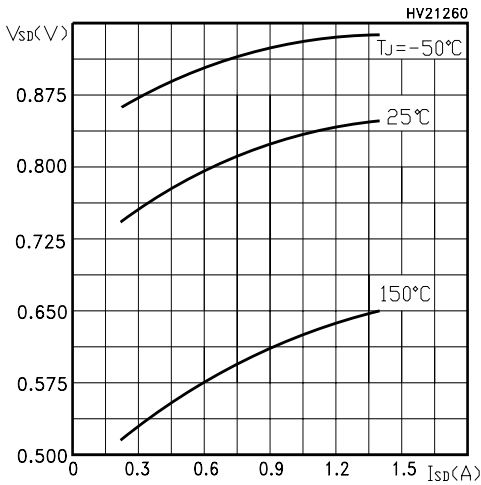


Figure 19: Normalized BV<sub>DSS</sub> vs Temperature

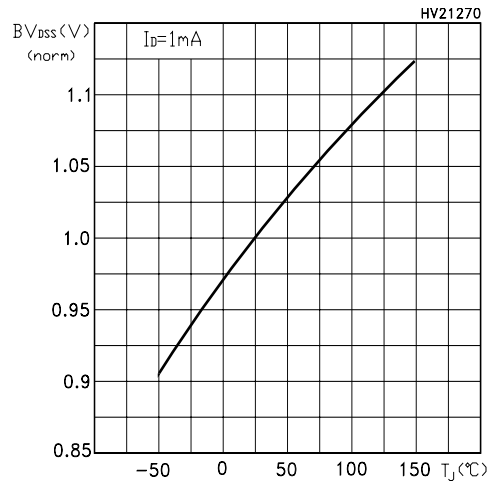
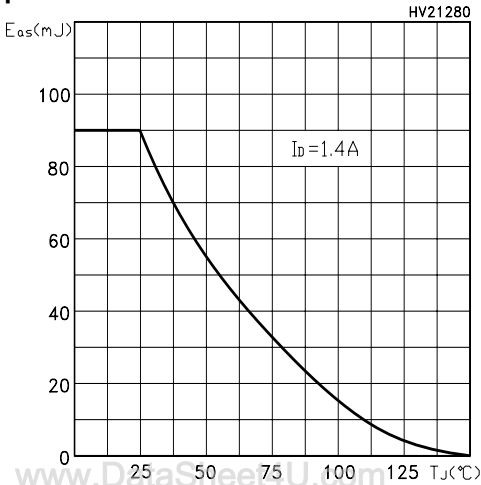


Figure 17: Maximum Avalanche Energy vs Temperature



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Figure 20: Unclamped Inductive Load Test Circuit

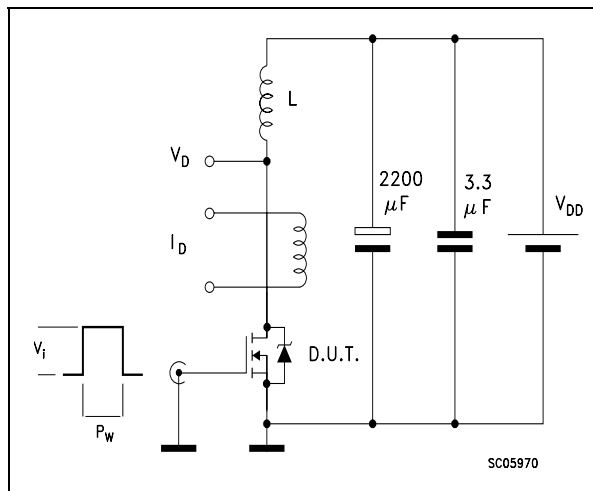


Figure 21: Switching Times Test Circuit For Resistive Load

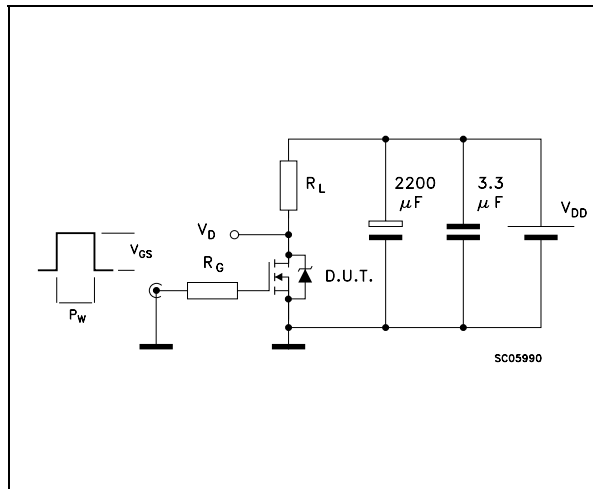


Figure 22: Test Circuit For Inductive Load Switching and Diode Recovery Times

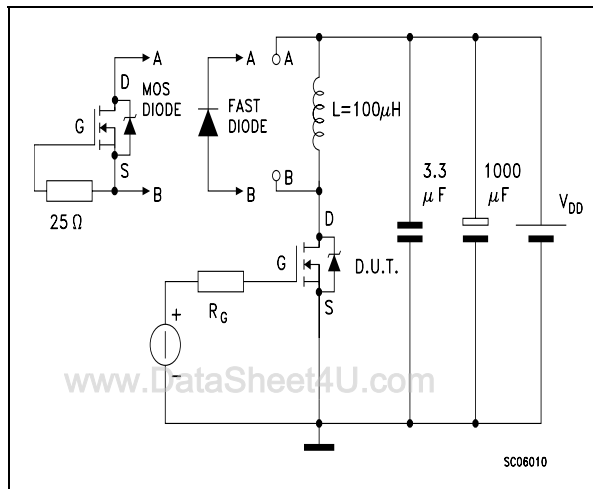


Figure 23: Unclamped Inductive Waferform

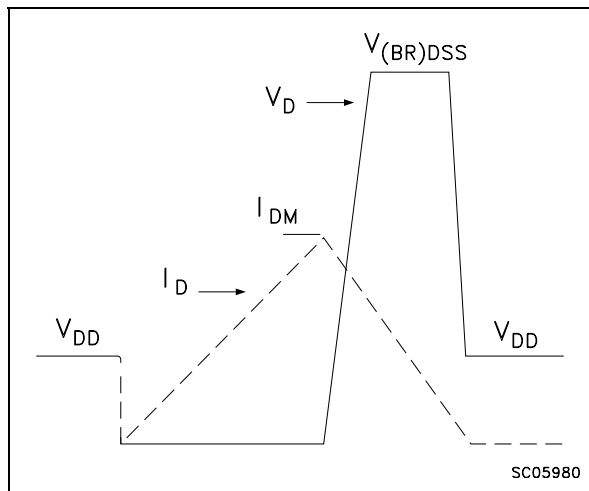


Figure 24: Gate Charge Test Circuit

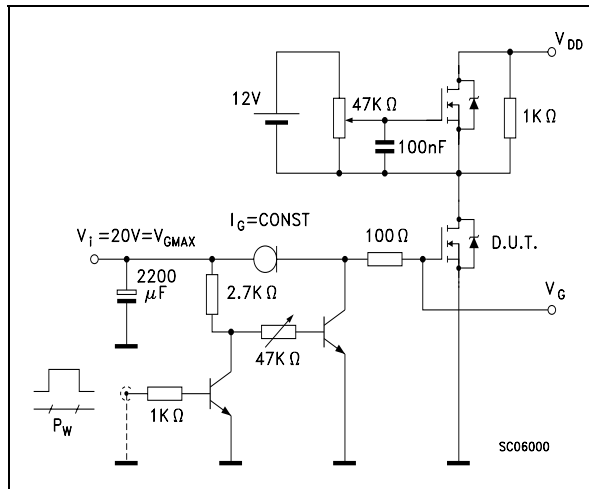
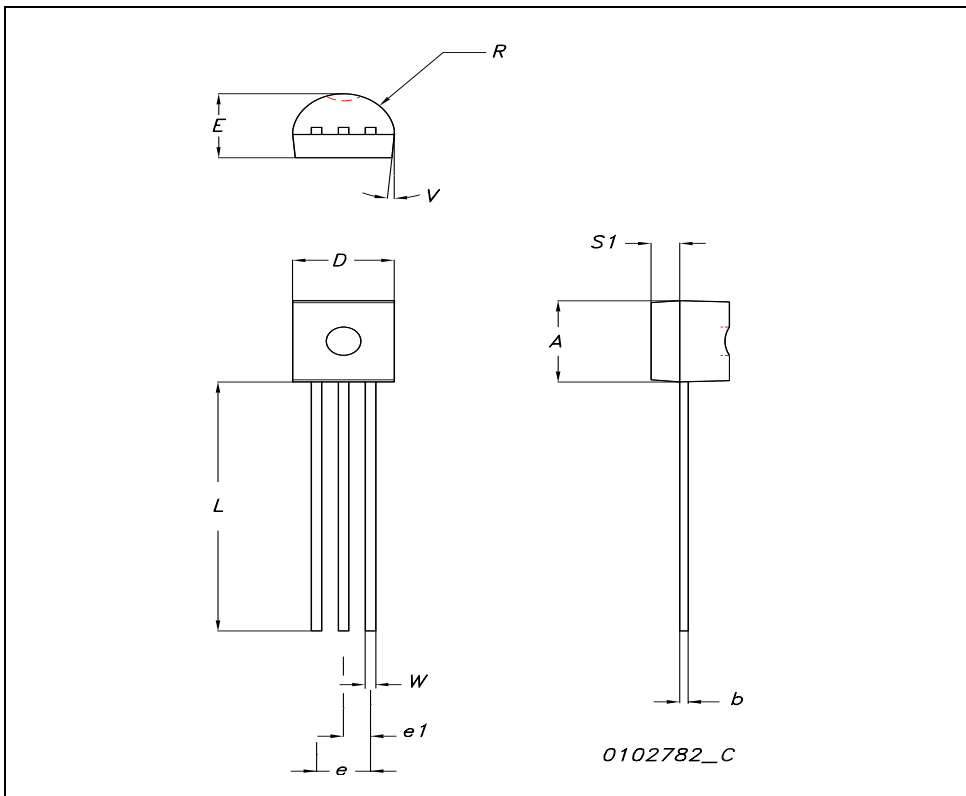


Figure 25: Test Circuit For Inductive Load Switching and Diode Recovery Times



**TO-92 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.32		4.95	0.170		0.194
b	0.36		0.51	0.014		0.020
D	4.45		4.95	0.175		0.194
E	3.30		3.94	0.130		0.155
e	2.41		2.67	0.094		0.105
e1	1.14		1.40	0.044		0.055
L	12.70		15.49	0.50		0.610
R	2.16		2.41	0.085		0.094
S1	0.92		1.52	0.036		0.060
W	0.41		0.56	0.016		0.022
V		5°			5°	

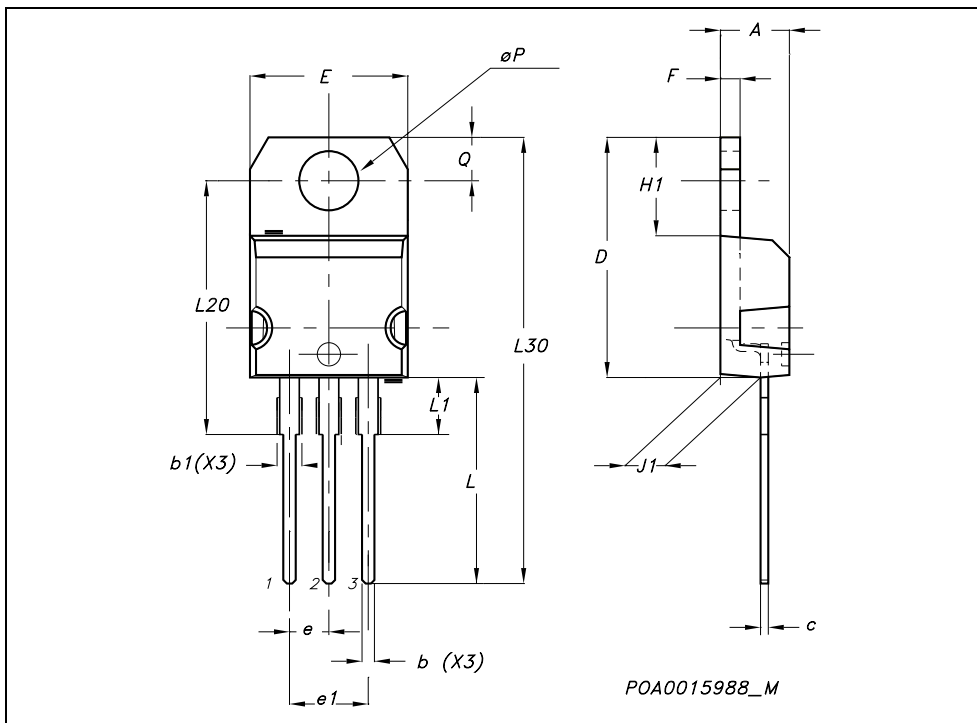


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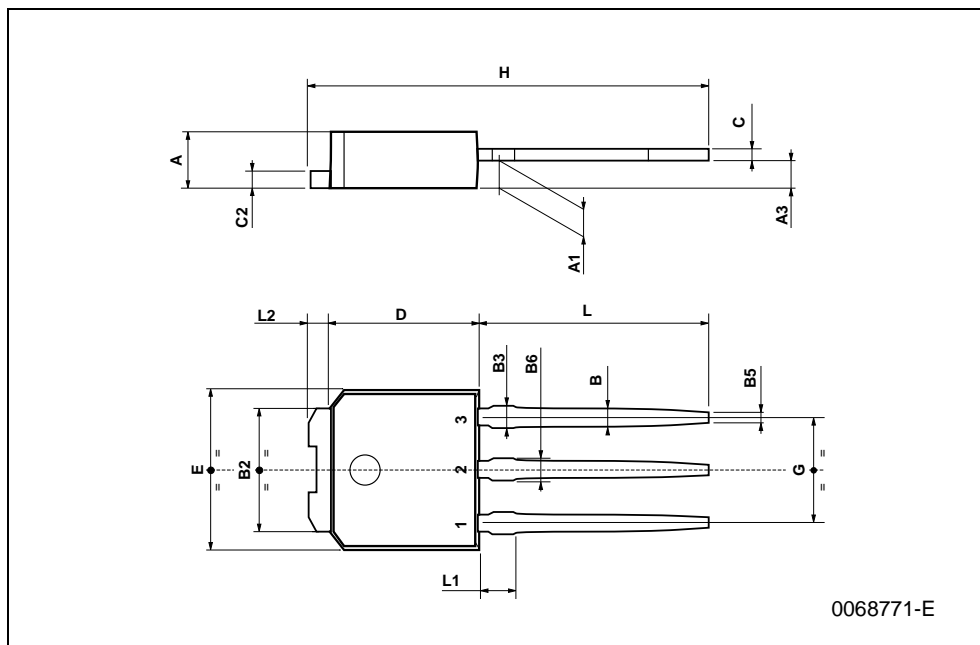
**TO-220 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



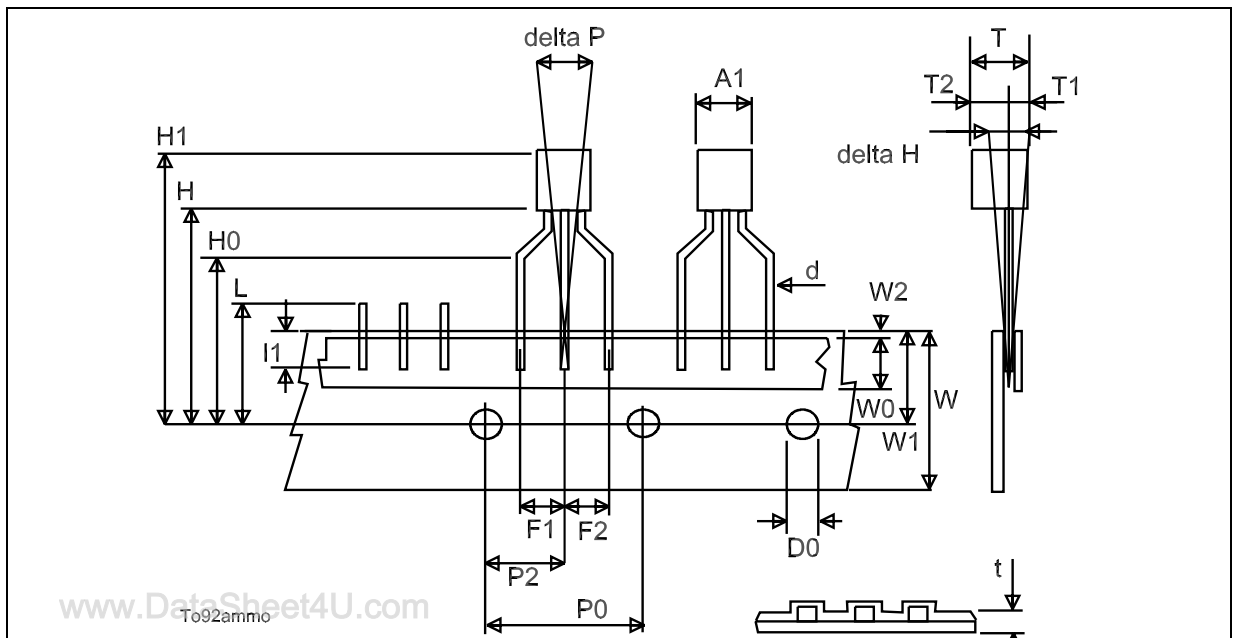
TO-251 (IPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



## TO-92 AMMOPACK

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A1	4.45		4.95	0.170		0.194
T	3.30		3.94	0.130		0.155
T1			1.6			0.06
T2			2.3			0.09
d	0.41		0.56	0.016		0.022
P0	12.5	12.7	12.9	0.49	0.5	0.51
P2	5.65	6.35	7.05	0.22	0.25	0.27
F1, F2	2.44	2.54	2.94	0.09	0.1	0.11
delta H	-2		2	-0.08		0.08
W	17.5	18	19	0.69	0.71	0.74
W0	5.7	6	6.3	0.22	0.23	0.24
W1	8.5	9	9.25	0.33	0.35	0.36
W2			0.5			0.02
H	18.5		20.5	0.72		0.80
H0	15.5	16	16.5	0.61	0.63	0.65
H1			25			0.98
D0	3.8	4	4.2	0.15	0.157	0.16
t			0.9			0.035
L			11			0.43
I1	3			0.11		
delta P	-1		1	-0.04		0.04



**Table 10: Revision History**

Date	Revision	Description of Changes
07-Jul-2004	3	The document change from "TARGET" to "COMPLETE" New stylesheet

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