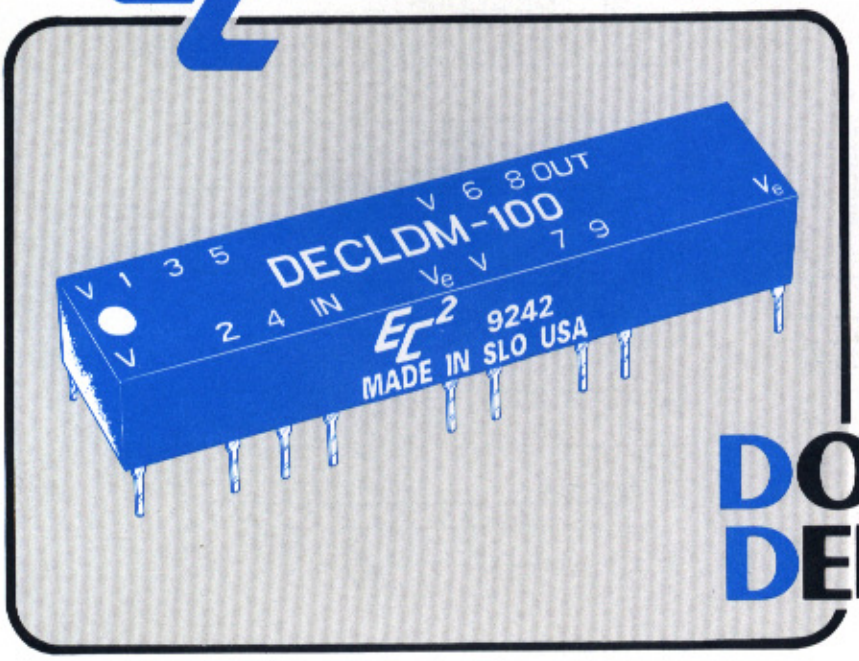
EC²



low profile

ECL COMPATIBLE DOUBLE LOGIC DELAY MODULE

- ECL input and outputs
- Delays stable and precise
- 32-pin DIP package (.250 high)
- Available in delays from 11 to 1000ns
- 10% taps—each isolated and with 70 ECL DC fan-out capacity
- Fast rise time on all outputs

design notes

The "DIP Series" Logic Delay Modules developed by Engineered Components Company have been designed to provide precise tapped delays with required driving and pick-off circuitry contained in a single 32-pin DIP package compatible with ECL "10,000 series" circuits. These logic delay modules are of hybrid construction utilizing the proven technologies of active integrated circuitry and of passive networks utilizing capacitive, inductive and resistive elements. The ICs utilized in these modules are burned-in to Level B of MIL-STD-883 to ensure a high MTBF. The MTBF on these modules, when calculated per MIL-HDBK-217B for a 50°C ground fixed environment, is in excess of 1.5 million hours. Module design includes compensation for propagation delays and incorporates internal termination at the output; no additional external components are needed to obtain the desired delay.

The DECLDM is offered in 23 delays from 11ns to 1000ns with each module incorporating taps at 10% increments of total delay. Delay tolerances and rise times are maintained as shown in the accompanying part number table, when tested under the "Test Conditions" shown. Delay time is measured at the −1.3V level on the leading edge; rise times are measured from 20% to 80% pulse amplitude. Temperature coefficient of delay is approximately +300 ppm/°C over the operating temperature range of −30 to +85°C.

These modules accept either logic "1" or logic "0" inputs and reproduce the logic at the selected output tap without inversion. The delay modules are intended primarily for use with positive going pulses and are calibrated to the tolerances shown in the table on rising edge delay; where best accuracy is desired in applications using falling edge timing, it is recommended that a special unit be calibrated for the specific application. Each module has the capability of driving up to 70 ECL DC loads on any one tap.

These "DIP Series" modules are packaged in a 32-pin DIP housing, molded of flame-proof Diallyl Phthalate per MIL-M-14, Type SDG-F, and are fully encapsulated in epoxy resin. Flat metal leads meet the solderability requirements of MIL-STD-202, Method 208. Leads provide positive standoff from the printed circuit board to permit solder-fillet formation and flush cleaning of solder-flux residues for improved reliability.

Marking consists of manufacturer's name, logo (EC²), part number, terminal identification and date code of manufacture. All marking is applied by silk screen process using white epoxy paint in accordance with MIL-STD-130, to meet the permanency of identification required by MIL-STD-202, Method 215.

EC² **engineered components company**

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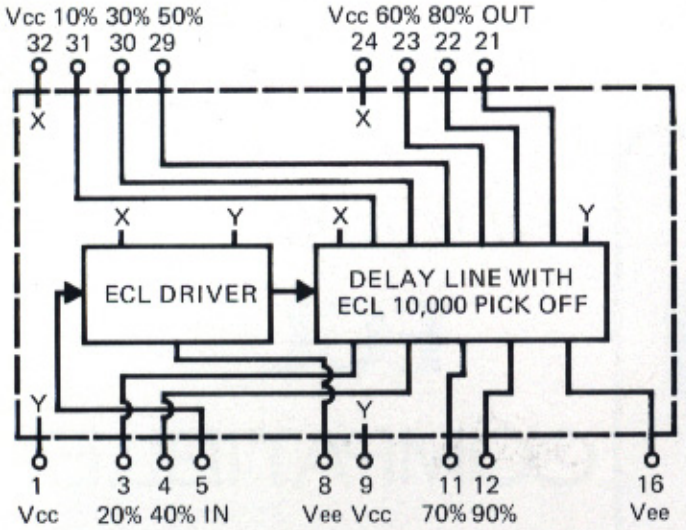
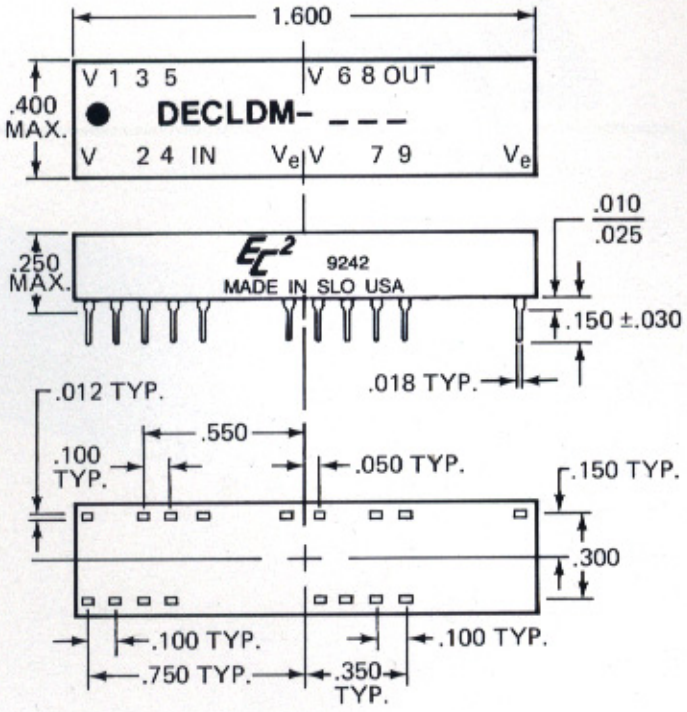
BLOCK DIAGRAM IS SHOWN BELOW



MECHANICAL DETAIL IS SHOWN BELOW



OPERATING SPECIFICATIONS

*Supply voltage:	−5.2V ±5% to Vee (can be operated on +5V to Vcc)
Supply current:	110ma typical
Logic 1 input at 25°C:	
Voltage	−.98 min.
Current	265ua max.
Logic 0 input at 25°C:	
Voltage	−1.63 max.
Current	.5ua min.
Logic 1 Voltage out at 25°C:	−.96 min.
Logic 0 Voltage out at 25°C:	−1.65 max.
Operating temperature range:	−30 to +85°C.
Storage temperature:	−55 to +125°C.

*Delays increase or decrease less than .5% for a respective increase or decrease of 5% in supply voltage.

TEST CONDITIONS

1. All measurements are made at 25°C.
2. Vee supply voltage is maintained at −5.2V DC.
3. All units are tested using a positive input pulse provided by a standard open emitter ECL 10,000 gate. The input and output utilize a 100 ohm pulldown resistor to −2V; the output is also loaded with one ECL 10,000 gate.

φ4. Input pulse width used is 5 to 10ns longer than full delay of module under test; spacing between pulses (falling edge to rising edge) is three times the pulse width used.

PART NUMBER TABLE

φ DELAYS AND TOLERANCES (in ns)											
Part Number	Rise Time Max.	Tap 1	Tap 2	Tap 3	Tap 4	Tap 5	Tap 6	Tap 7	Tap 8	Tap 9	Output
DECLDM-11	4	2 ±.5	3 ±.5	4 ±.5	5 ±1	6 ±1	7 ±1	8 ±1	9 ±1	10 ±1	11 ±1
DECLDM-20	4	2 ±.5	4 ±.5	6 ±1	8 ±1	10 ±1	12 ±1	14 ±1	16 ±1	18 ±1	20 ±1
DECLDM-30	4	3 ±.5	6 ±1	9 ±1	12 ±1	15 ±1	18 ±1	21 ±1	24 ±1.5	27 ±1.5	30 ±1.5
DECLDM-40	4	4 ±.5	8 ±1	12 ±1	16 ±1	20 ±1	24 ±1.5	28 ±1.5	32 ±1.5	36 ±1.5	40 ±2
DECLDM-50	4	5 ±1	10 ±1	15 ±1	20 ±1	25 ±1.5	30 ±1.5	35 ±1.5	40 ±2	45 ±2	50 ±2
DECLDM-60	4	6 ±1	12 ±1	18 ±1	24 ±1.5	30 ±1.5	36 ±1.5	42 ±2	48 ±2	54 ±2	60 ±2.5
DECLDM-70	4	7 ±1	14 ±1	21 ±1	28 ±1.5	35 ±1.5	42 ±2	49 ±2	56 ±2	63 ±2	70 ±2.5
DECLDM-80	4	8 ±1	16 ±1	24 ±1.5	32 ±1.5	40 ±2	48 ±2	56 ±2	64 ±2.5	72 ±2.5	80 ±3
DECLDM-90	5	9 ±1	18 ±1	27 ±1.5	36 ±1.5	45 ±2	54 ±2	63 ±2	72 ±2.5	81 ±3	90 ±3
DECLDM-100	5	10 ±1	20 ±1	30 ±1.5	40 ±2	50 ±2	60 ±2.5	70 ±2.5	80 ±3	90 ±3	100 ±3
DECLDM-150	8	15 ±1	30 ±1.5	45 ±2	60 ±2.5	75 ±2.5	90 ±3	105 ±4	120 ±4	135 ±4	150 ±5
DECLDM-200	10	20 ±1	40 ±2	60 ±2.5	80 ±3	100 ±3	120 ±4	140 ±5	160 ±5	180 ±6	200 ±6
DECLDM-250	15	25 ±1.5	50 ±2	75 ±2.5	100 ±3	125 ±4	150 ±5	175 ±5	200 ±6	225 ±7	250 ±8
DECLDM-300	15	30 ±1.5	60 ±2.5	90 ±3	120 ±4	150 ±5	180 ±6	210 ±7	240 ±7	270 ±8	300 ±9
DECLDM-350	20	35 ±1.5	70 ±2.5	105 ±4	140 ±5	175 ±5	210 ±7	245 ±8	280 ±9	315 ±10	350 ±11
DECLDM-400	20	40 ±2	80 ±3	120 ±4	160 ±5	200 ±6	240 ±7	280 ±9	320 ±10	360 ±11	400 ±12
DECLDM-450	25	45 ±2	90 ±3	135 ±4	180 ±6	225 ±7	270 ±8	315 ±10	360 ±11	405 ±12	450 ±14
DECLDM-500	25	50 ±2	100 ±3	150 ±5	200 ±6	250 ±8	300 ±9	350 ±11	400 ±12	450 ±14	500 ±15
DECLDM-600	30	60 ±2.5	120 ±4	180 ±6	240 ±7	300 ±9	360 ±11	420 ±13	480 ±15	540 ±16	600 ±18
DECLDM-700	35	70 ±2.5	140 ±5	210 ±7	280 ±9	350 ±11	420 ±13	490 ±15	560 ±17	630 ±19	700 ±20
DECLDM-800	40	80 ±3	160 ±5	240 ±7	320 ±10	400 ±12	480 ±15	560 ±17	640 ±19	720 ±20	800 ±20
DECLDM-900	45	90 ±3	180 ±6	270 ±8	360 ±11	450 ±14	540 ±16	630 ±19	720 ±20	810 ±20	900 ±22
DECLDM-1000	50	100 ±3	200 ±6	300 ±9	400 ±12	500 ±15	600 ±18	700 ±20	800 ±20	900 ±22	1000 ±22

φAll modules can be operated with a minimum input pulse width of 20% of full delay and pulse period approaching square wave; since delay accuracies may be somewhat degraded, it is suggested that the module be evaluated under the intended specific operating conditions. Special modules can be readily manufactured to improve accuracies and/or provide customer specified random delay times for specific applications.