DAC-562
Monolithic, High Performance 12-Bit D/A Converter

FEATURES

- **12-Bit resolution**
- **300 Nanoseconds settling time**
- **±10 ppm/°C maximum tempco**
- **5 Output ranges**
- **±¼ LSB linearity**
- **562 Pin compatibility**

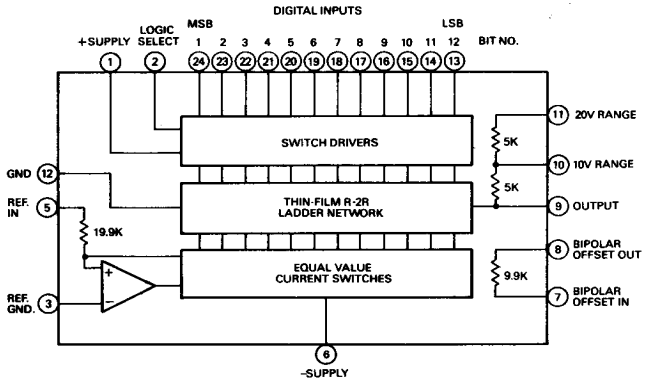
GENERAL DESCRIPTION

The DAC-562 is a new high performance monolithic 12-bit D/A converter fabricated with advanced bipolar technology. The circuit uses a precision, laser-trimmed thin film R-2R ladder network driven by equal-value switched current sources to achieve ¼ LSB typical linearity, 300 nanoseconds setting time, and ±10 ppm/°C maximum gain tempco.

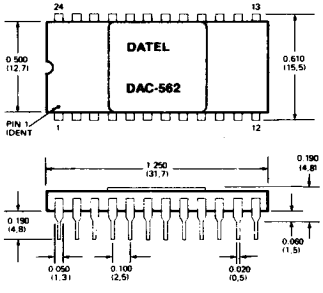
The DAC-562 operates from TTL or CMOS input logic and provides a 0 to 2 mA or ±1 mA output current. The converter contains tracking feedback and bipolar offsetting resistors to provide five output voltage ranges when used with an external operational amplifier: 0 to +5V, 0 to +10V, ±2.5, ±5V, and ±10V. Since these resistors closely track the R-2R ladder with temperature, gain stability of better than 10 ppm/°C is achieved. Differential linearity error is ¼ LSB typical and ½ LSB maximum, with output monotonicity guaranteed over the operating temperature range.

Output settling time for a full-scale change to ½ LSB is 300 nanoseconds typical and 400 nanoseconds maximum.

The DAC-562 is completely pin and function compatible with industry standard 562 D/A converters. The package is a 24-pin hermetically sealed ceramic DIP; power requirement is +5V to +15V and −15V dc. The DAC-562C operates over a 0°C to +70°C temperature range.



MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+ SUPPLY	13	BIT 12 IN (LSB)
2	LOGIC SELECT	14	BIT 11 IN
3	REF. GROUND	15	BIT 10 IN
4	N.C.	16	BIT 9 IN
5	REFERENCE IN	17	BIT 8 IN
6	− SUPPLY	18	BIT 7 IN
7	BIP. OFF IN	19	BIT 6 IN
8	BIP. OFF OUT	20	BIT 5 IN
9	OUTPUT	21	BIT 4 IN
10	10V RANGE	22	BIT 3 IN
11	20V RANGE	23	BIT 2 IN
12	GROUND	24	BIT 1 IN (MSB)

ABSOLUTE MAXIMUM RATINGS	DAC-562C
Positive Supply, pin 1	+20V
Negative Supply, pin 6	−20V
Reference Input, pin 5	± Supply
Reference Ground, pin 3	0V
Digital Inputs, pins 13-24	−1V to +12V
Logic Select Input, pin 2	−1V to +12V
Output, pin 9	+ Supply, −5V
Resistors, pins 7, 8, 10, 11	± Supply

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, +5V and −15V Supplies, +10V reference unless otherwise noted.

INPUTS	DAC-562C
Resolution	12 Bits
Coding, unipolar output	Straight Binary
Coding, bipolar output	Offset Binary
Input Logic Level, bit ON ("1")[1]	+2.0 min. at 100 nA max.
Input Logic Level, bit OFF ("1")[1]	+0.8V max. at −100 μA max.
Reference Input Voltage	+10V
Reference Input Resistance	20 KΩ
OUTPUTS	
Output Current, unipolar	0 to −2 mA
Output Current, bipolar	±1 mA
Output Voltage Ranges, unipolar	0 to +5V
	0 to +10V
Output Voltage Ranges, bipolar	±2.5V
	±5V
	±10V
Output Voltage Compliance	±1V
Output Resistance	2 KΩ
Output Capacitance	20 pF
PERFORMANCE	
Linearity Error, max.	±½ LSB
Linearity Error Over Temp., max.	±1 LSB
Differential Linearity Error, max.	±½ LSB
Monotonicity	Over Oper. Temp. Range
Gain Error, max.[2]	±0.25%
Unipolar Zero Error, max.[2]	±0.05%
Bipolar Offset Error, max.[2]	±0.25%
Gain Tempco, max.[3]	±10 ppm/°C
Zero Tempco, max.[3]	±2 ppm/°C
Bipolar Offset Tempco, max.[3]	±4 ppm/°C
Settling Time to ½ LSB[4]	300 nsec. typ., 400 nsec. max.
Power Supply Sensitivity, max.	±3.5 ppm of FSR/% Supply
POWER REQUIREMENTS	
Rated Power Supply Voltage	+5V dc, −15V dc
Positive Supply Range[5]	+4.75V to +16.5V
Negative Supply Range	−15V dc ±10%
Power Supply Quiescent Current, max.[6]	+15 mA, −23 mA
PHYSICAL/ENVIRONMENTAL	
Operating Temp. Range	0°C to +70°C
Storage Temp. Range	−65°C to +150°C
Package, Hermetically Sealed	24 pin ceramic DIP
*Specifications same as first column	

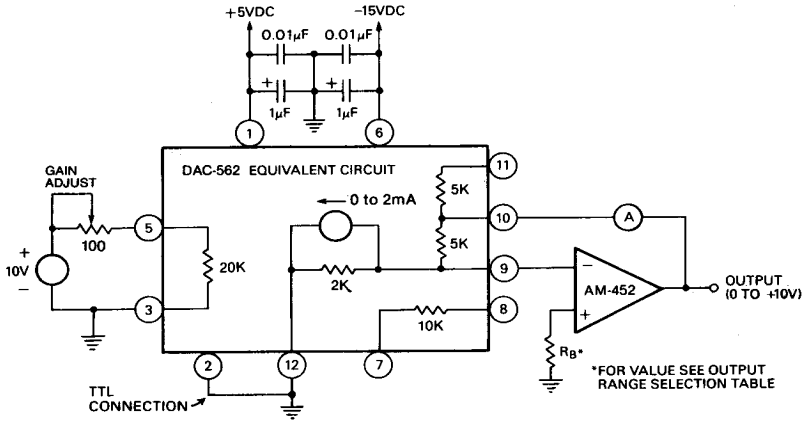
FOOTNOTES:

1. + Supply must be +5V ±5%. For operation with CMOS logic, see Technical Note 1.
2. Adjustable to zero using external potentiometers. Specified error is for 100 ohm trim resistors and external operational amplifier using internal feedback resistor.
3. Using external operational amplifier and internal feedback and offset resistor. Zero Tempco and Bipolar Offset Tempco are in ppm/°C or FSR (Full Scale Range)
4. For full-scale change: all bits ON-to-OFF, or all bits OFF-to-ON.
5. Maximum Positive Supply Voltage is +16V for high level logic only, i.e., when Pin 2 is tied to Pin 1. See Technical Note 1.
6. Allow 30 seconds warm-up time.

TECHNICAL NOTES

1. For TTL input logic; pin 2 should be connected to pin 12 and the + supply must be +5V dc (±5%). For CMOS input logic, connect pin 2 to pin 1 and use any + supply voltage from +9.5V to +12V dc. CMOS threshold levels are then + Vs x 0.7 for bit ON and + Vs x 0.3 for bit OFF. Logic input current is the same as that specified for TTL.
2. Gain and bipolar offset errors are adjustable to zero by means of two 100 ohm trimming pots. The adjustment range is ±0.3% of FSR for gain and ±0.6% of FSR for bipolar offset. The unipolar zero error is adjustable to zero by means of the offset adjustment of the external output amplifier.
3. The output voltage compliance range of ±1V should not be exceeded or else accuracy will be affected. If a resistor load is driven instead of an operational amplifier summing junction then the maximum resistor value is 500 ohms for unipolar operation and 1K ohms for bipolar operation.
4. Output settling time is specified for current output and is measured with a small current sampling resistor to ground (100 ohms). Voltage output settling time depends on the output operational amplifier used. DATEL's AM-500 is recommended for about 500 nanoseconds settling and AM-452-2 is recommended for about 1.5 microseconds settling. Both should be used with a 3-20 pF variable compensating capacitor across the feedback resistor which should be adjusted for optimum settling time.
5. For best high speed performance, both power supplies should be bypassed with 1 μF electrolytics in parallel with 0.01 μF ceramic capacitors as close as possible to the ± supply pins.
6. The gain and bipolar offset temperature coefficients are specified with the internal feedback and offset resistors used in conjunction with an external operational amplifier. This is because these resistors track the R-2R ladder with temperature and therefore the tempco's do not depend on absolute resistor tempco. The tempco of the external +10V reference must also be included in the total converter tempco, however.
7. The DAC-562 wideband output noise with all bits ON is typically 100 μV peak-to-peak over 0.1 Hz to 5 MHz.

UNIPOLAR OPERATION—See Output Range Selection Table

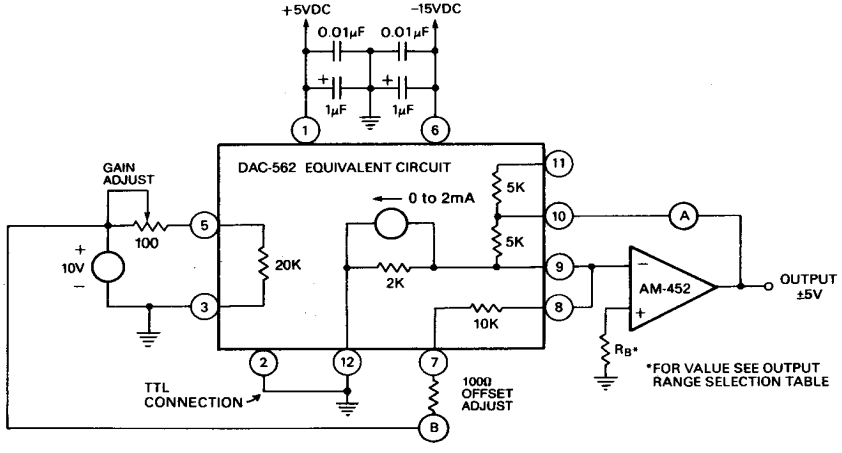


OUTPUT VOLTAGE RANGE SELECTION (See Connection Diagrams)

OUTPUT VOLTAGE RANGE	CONNECT THESE PINS TOGETHER				R_B, BIAS COMP. RESISTOR*
0 to +5V	A & 10	9 & 11			1.11 kΩ
0 to +10V	A & 10				1.43 kΩ
±2.5V	A & 10	9 & 11	8 & 9	7 & B	1 kΩ
±5V	A & 10		8 & 9	7 & B	1.25 kΩ
±10V	A & 11		8 & 9	7 & B	1.43 kΩ

*Carbon composition resistor value used from amplifier positive input terminal to ground to compensate for offset due to bias current.

BIPOLAR OPERATION—See Output Range Selection Table



CALIBRATION AND APPLICATION

CODING TABLE—See Calibration Procedure

INPUT CODE	OUTPUT VOLTAGE RANGE				
	0 to +5V	0 TO +10V	±2.5V	±5V	±10V
1111 1111 1111	+4.9988V	+9.9976V	+2.4988V	+4.9976V	+9.9951V
1100 0000 0000	+3.7500	+7.5000	+1.2500	+2.5000	+5.0000
1000 0000 0000	+2.5000	+5.0000	0.0000	0.0000	0.0000
0100 0000 0000	+1.2500	+2.5000	−1.2500	−2.5000	−5.0000
0000 0000 0001	+0.0012	+0.0024	−2.4988	−4.9976	− 9.9951
0000 0000 0000	0.0000	0.0000	−2.5000	−5.0000	−10.0000

CALIBRATION PROCEDURE

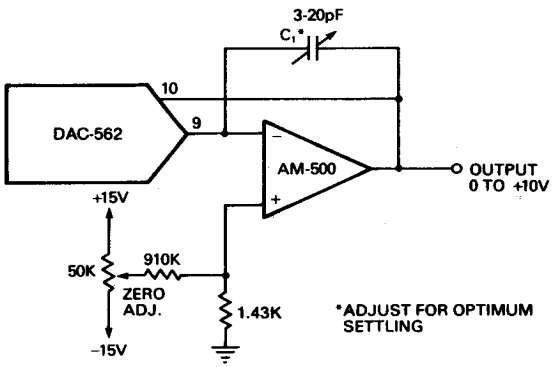
UNIPOLAR OPERATION

1. Set all digital inputs low. Adjust the output amplifier offset for 0 volts output.
2. Set all digital inputs high. Adjust Gain trimming pot for an output of +FS − 1 LSB.
   FS − 1 LSB = +9.9976V for 0 to +10V range.
   = +4.9988V for 0 to +5V range.

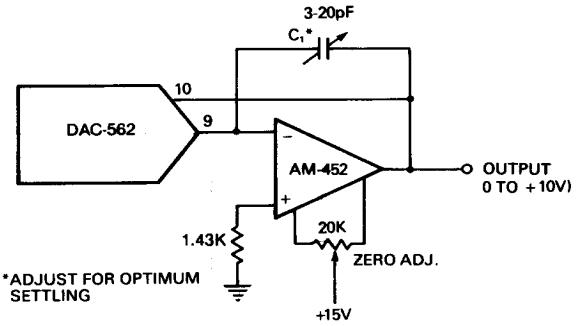
BIPOLAR OPERATION

1. Set all digital inputs low. Adjust Bipolar Offset trimming pot for one of the following output voltages:
   −2.5V for ±2.5V range
   −5.0V for ±5V range
   −10.0V for ±10V range
2. Set bit 1 (MSB) input high and all other digital inputs low. Adjust Gain trimming pot for 0 volts output.

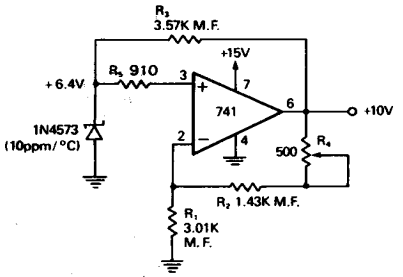
CIRCUIT FOR FAST VOLTAGE OUTPUT (≈0.5 μSEC. SETTLING)



CIRCUIT FOR FAST VOLTAGE OUTPUT (≈1.5 μSEC. SETTLING)



+10V REFERENCE CIRCUIT



Adjust R_4 for +10.000V output. For best stability R_1 & R_2 should track each other closely with temperature. R_4 should be a low tempco trimming pot or else a selected metal film trim resistor.

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE
DAC-562C	0 to +70°C

ACCESSORIES Part Number	Description
TP50 —	Trimming potentiometer