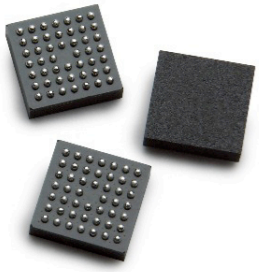
ASDL-7021

IrDA® FIR/VFIR Controller in TFBGA Package

Data Sheet



Description

The ASDL-7021 is a new generation large scale integration (LSI) IrDA controller supporting speeds of SIR (up to 115Kbps), MIR(1.152Mbps), FIR(4Mbps) and VFIR (16Mbps). It consists of IrDA Control Block, Remote Control Block, Timer Control Block, Global Control block including Buffer Memory and Direct Memory Access Control Block (DMA) integrated into one single chip.

It has all the hardware including Buffer Memory and Direct Memory Access (DMA) that enables convenient access to its peripheral IO and memories from system bus which is similar to simple memory devices. ASDL-7021 is a class of its own as unlike conventional LSI which utilizes external DMA for implementing fast infrared transfer, complicated bus timing and required additional logic for its interface.

ASDL-7021 utilizes two memory banks for external access and internal DMA access; these 2 banks are interchangeable to prevent bus contention. These two banks can be switched using memory select function of the internal register and separates internal bus from external, which enables parallel operation of external microcontroller operation and internal IrDA data transfer operation. ASDL-7021 has embedded Universal Remote Control (RC) function for general purpose remote control communication.

Together with Lite-On FIR transceiver and IrSimple software, ASDL-7021 is designed to provide Industry a total solution for high speed wireless connectivity solution in miniature packaging.

Applications

- Mobile Data Communication and Universal Remote Control
  - Mobile Phones
  - PDAs
  - Digital Still Camera
  - Printer
  - Notebooks
  - Handy Terminal
  - Dongles
  - Industrial and Medical Instrument

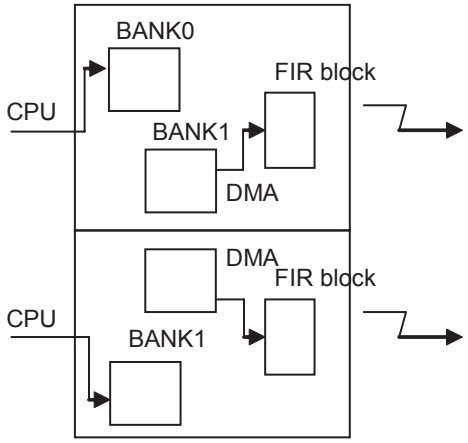
Features

General Features

- Interfaces with IrDA® Compliant IR Transceiver up to VFIR
- Miniature 48 pin TFBGA Package
  - Height : 1.2 mm
  - Width : 4.0 mm
  - Depth : 4.0 mm
- 8-bit Memory Mapped Interface
- Input clock of 48 MHz
- 4 transmission speed in 3 Blocks
  - SIR Block (2.4 to 115.2Kbps)
  - FIR Block (1.152Mbps for MIR and 4Mbps for FIR)
  - VFIR Block (16Mbps)
- Operating temperature from -40° C ~ 85°C
  - Critical parameters are guaranteed over temperature and supply voltage
- Core Power Supply = 1.8V

  Clock Power Supply = 3.3V

  IO Power Supply =1.8V, 2.5V, 3.3V
- RAM Block with On-Chip buffer memory of 8KByte x 2 Bank Configuration
  - 1 bank for external access x 8 bit width
  - 1 bank for internal access x 8 bit width through on-chip DMA block
  - These 2 banks can be switched
  - Each transmit and receive have their own buffer memory of 8KByte x 2



Features (Cont.)

- Infrared Interface Block
  - IrDA send/receive functions (IRTX0, IRRX0)
  - Remote Control send function (IRTX1)
- DMA Block
  - DMA transfer function between buffer memory and SIR, FIR, VFIR block
- Remote Control Block
  Generate Remote Control burst signal
- Timer Block
  - 2 channels of generic 16 bit timer
  - 1 channel of Mediabusy timer
- Moisture Level 3
- Lead-Free and ROHS Compliant

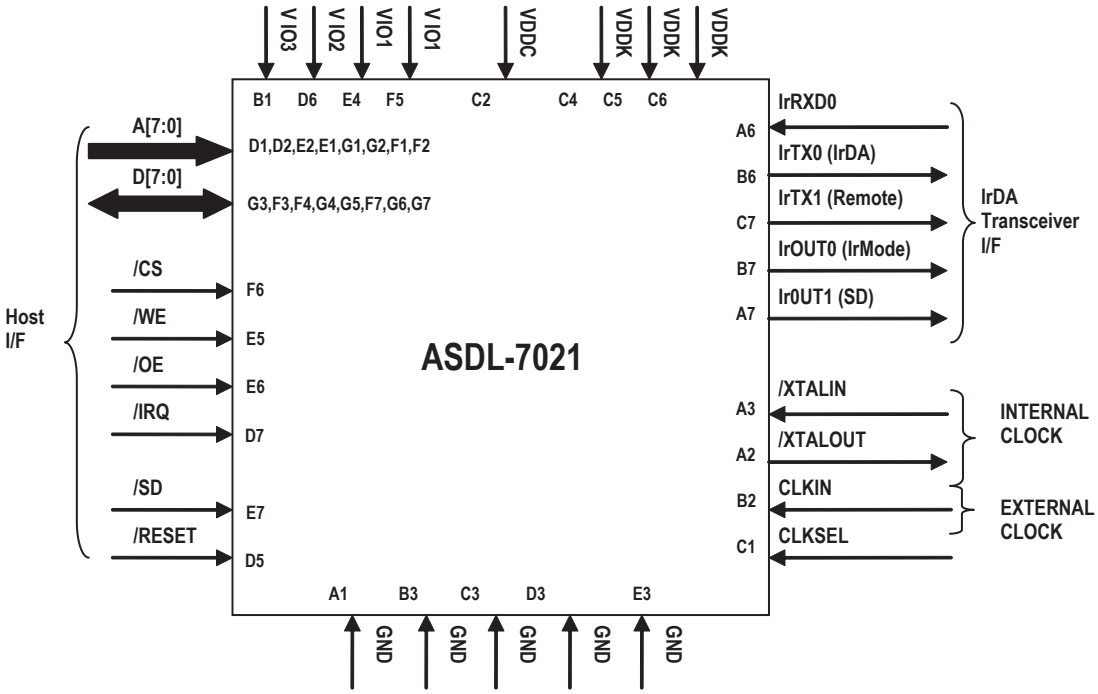


Figure 1a. Pin Layout of ASDL-7021

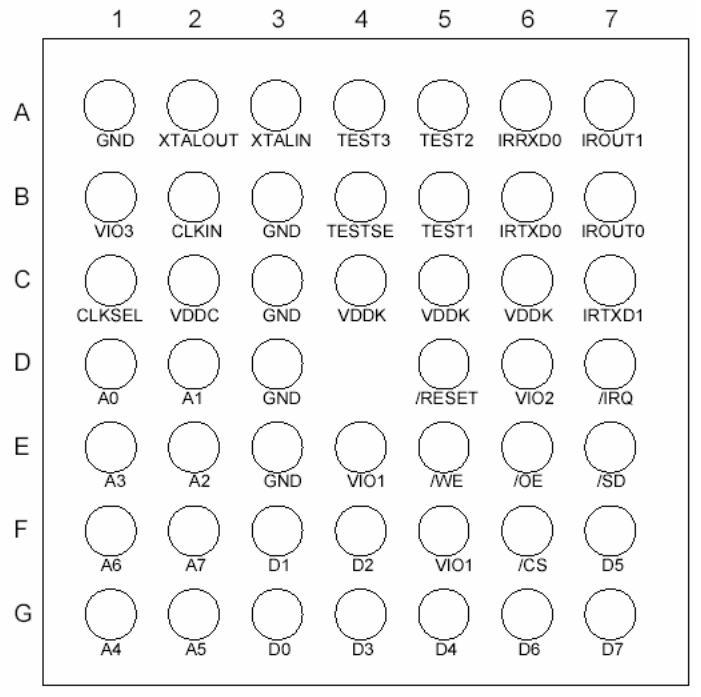


Figure 1b. Pin layout of ASDL-7021 (Top View)

Application Support Information

The Application Engineering Group is available to assist you with the application design associated with ASDL-7021 FIR/VFIR Controller. You can contact them through your local sales representatives for additional details.

Order Information

Part Number	Packaging Type	Quantity
ASDL-7021	Tape and Reel	4000

I/O Pins Configuration Table

Pins Description

Symbol	Pin(s)	Type	Buffer Type (Refer to Figure 2)	Description
Power				
VDDK	C4,C5,C6	POWER		1.8V Power
VDDC	C2	POWER		3.3V Power
VIO1	E4,F5	POWER		1.8V, 2.5V, 3.3V
VIO2	D6	POWER		1.8V, 2.5V, 3.3V
VIO3	B1	POWER		1.8V, 2.5V, 3.3V
GND	A1,B3,C3,D3,E3	POWER		GND

Bus Interface Signals (VIO1 Voltage)

A0-A7	D1,D2,E2,E1, G1,G2,F1,F2	I	I	An 8-bit address signal line connects itself directly with an external address bus. It selects the internal buffer memory and the register addresses of each function module. With the assertion of the CS signal, A0 - A7 turn out to be valid, which decides the internal addresses.
D0-D7	G3,F3,F4,G4 G5,F7,G6,G7	I/O	IO4	An 8-bit data signal line connects itself directly with an external data bus. It is a signal that performs data conversion with the internal buffer memory and each function module.The bus direction is determined by WE and OE.
/CS	F6	I	I	CS is a chip select signal for the IC. Asserting CS activates the external bus of this LSI.
/WE	E5	I	I	The WE signal turns the direction of a data bus to the input direction, and takes it into the IC for the internal buffer memory and registers designated by the address bus, at the start-up of the signal.
/OE	E6	I	I	The OE signal turns the data bus direction to the output direction, and outputs to the data bus the contents of the internal buffer memory and register designated by the address bus.
/IRQ	D7	O	O4	This is a signal line that notifies to the outside that ASDL-7021 requests an interrupt.

Other Signals (VIO1 Voltage)

/RESET	D5	I	I	This RESET signal resets ASDL-7021.
/SD	E7	I	I (internal PullDown)	1. Low: Shutdown IC is suspending the clock supply to the core. The output signal retains the condition. 2. High: IC is keeping the clock supply to the core. However, when the externally connected quartz crystal is used with CLKSEL=Low, the oscillation of the quartz crystal is kept performed under the condition of CLKSEL=Low, and SD: Low. When you want to stop the quartz crystal oscillation, you must set CLKSEL=High. 3. After wake up from SD, the IC must be reset.
CLKSEL	C1	I	I	This is used for selecting whether the input signal from CLKIN should be used for the clock input or whether the quartz crystal should be used at XTALIN and XTALOUT. Using quartz crystal, CLKSEL = Low, external quartz crystal is kept under oscillation CLKSEL = High, external quartz crystal is suspending oscillation Using CLKIN signal, set CLKSEL = High

Infrared Interface Signal (VIO2 voltage)

IrTXD0	B6	O	O4	This outputs the IrDA infrared signal and remote control send signal.
IrTXD1	C7	O	O4	This outputs the IrDA infrared signal and remote control send signal.
IrRXD0	A6	I	I	This inputs a signal from the infrared module.
IrOUT0	B7	O	O4	This is an output signal for controlling the infrared module.
IrOUT1	A7	O	O4	This is an output signal for controlling the infrared module.

Clock Signal (VIO3 voltage)

CLKIN	B2	I	I	Clock input

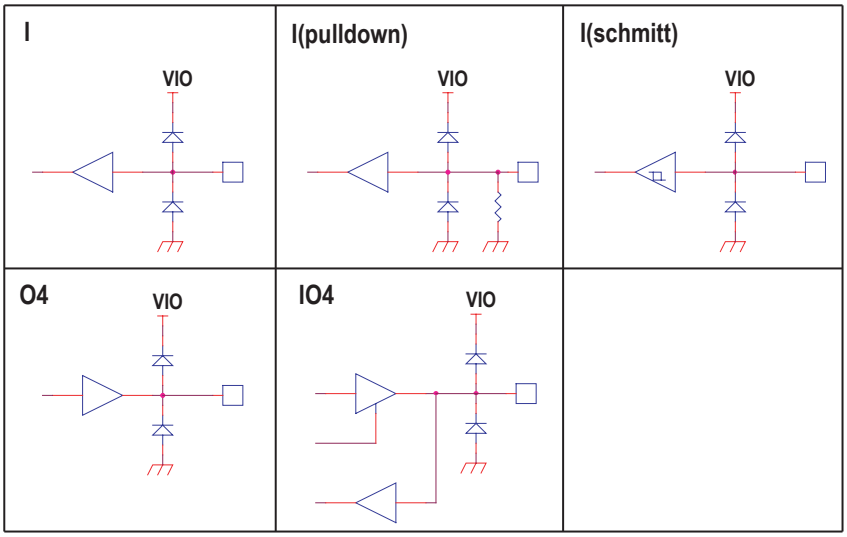
Clock Signal (VDDC Voltage)

/XTALIN	A3	I	You must connect quartz crystal to create a basic clock or input the clock from outside. Usually you must connect the quartz crystal between XTALIN and XTALOUT. The oscillation frequency of the crystal must be 48MHz.
/XTALOUT	A2	O	

TEST Signal

TEST1	B5	I	I (Internal PullDown)	Test signal (Set to N.C).
TEST2	A5	I	I (Internal PullDown)	Test signal (Set to N.C).
TEST3	A4	I	I (Internal PullDown)	Test signal (Set to N.C).
TESTSE	B4	I	I (Internal PullDown)	Test signal (Set to N.C).

Output BufferType



O4:

IOL=4mA,IOH=4mA(VIO = 3.3V)

IOL=2.2mA,IOH=2.2mA(VIO = 2.5V)

IOL=1.4mA,IOH=1.4mA(VIO = 1.8V)

Figure 2. I/O Description

Block Diagram

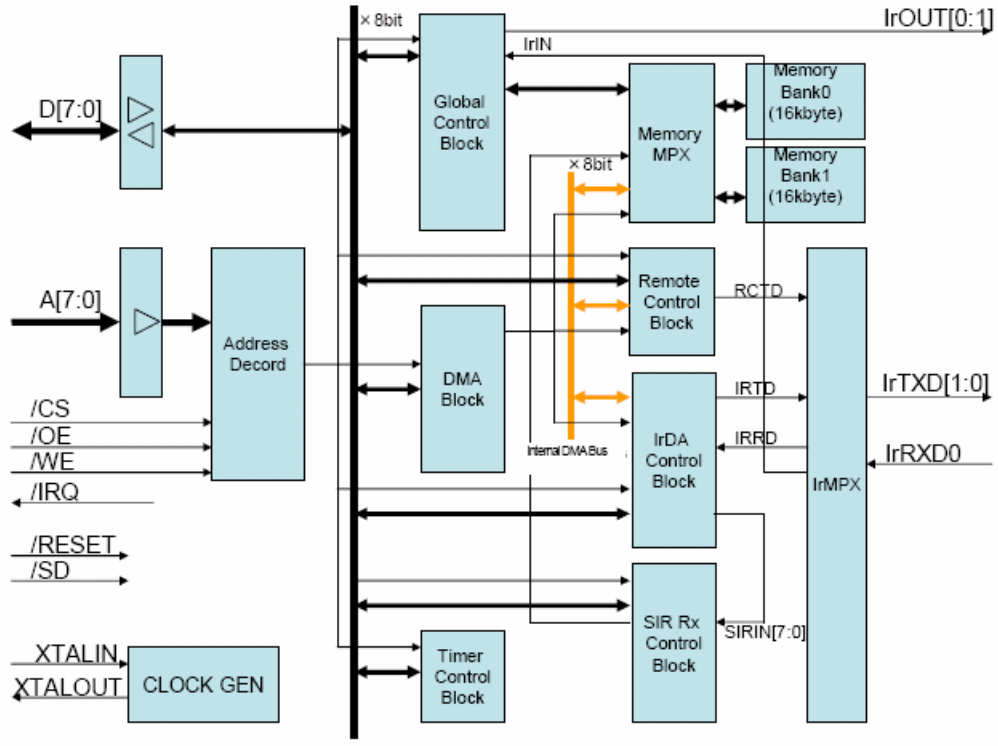


Figure 3. Block Diagram of internal blocks of ASDL-7021

Registers Descriptions

Block Name	Base Address	Offset	Register Name
IrDA	0x0000	0000h	IRBA0R(IR Base Address0 Register)
		0001h	IRBA1R(IR Base Address1 Register)
		0002h	IRBA2R(IR Base Address2 Register)
		0003h	IRRSR(IR Ring Size Register)
		0004h	IRPLC0R(IR Physical Layer Config0 Register) (unused)
		0005h	IRPLC1R(IR Physical Layer Config1 Register) (unused)
		0006h	IRPLC2R(IR Physical Layer Config2 Register)
		0007h	IRPLC3R(IR Physical Layer Config3 Register)
		0008h	IRC0R(IR Config0 Register)
		0009h	IRC1R (IR Config1 Register)
		000Ah	IRC2R (IR Config2 Register)
		000Bh	IRC3R (IR Config3 Register)(unused)
		000Ch	IRE0R(IR Enable0 REG.)
		000Dh	IRE1R (IR Enable1REG.)
		000Eh	IRMPL0R(IR Max Packet Length0 REG.)
		000Fh	IRMPL1R (IR Max Packet Length1REG.)
		0010h	IRRP0R(IR Ring Prompt0 REG.)
		0011h	IRRP1R (IR Ring Prompt Register1 REG.) (unused)
		0012h	IRRP2R (IR Ring Prompt Register2 REG.) (unused)
		0013h	IRRP3R (IR Ring Prompt Register3 REG.) (unused)
		0014h	IRRBC0R(IR Receive Byte Count0 REG.)
		0015h	IRRBC1R (IR Receive Byte Count1 REG.)
		0016h	IRRRPR0R(IR Rx Ring Pointer Readback REG.)
		0017h	IRTRPR0R (IR Tx Ring Pointer Readback REG.)
		0018h	IRSF0R(IR SIR Flags0 REG.)
		0019h	IRSF1R (IR SIR Flags1 REG.)
		001Ah	IRLPC0R(IR Latched Phy Config0 REG.)
		001Bh	IRLPC1R (IR Latched Phy Config 1REG.)
		001Ch	IRAC0R(IR Address Compare0 REG.)
		001Dh	IRAC1R (IR Address Compare1 REG.)
		001Eh	IRAC2R (IR Address Compare2 REG.)
		001Fh	IRAC3R (IR Address Compare3 REG.)
		0020h	IRLT0R(IR Latency Timer0 REG.)
		0021h	IRLT1R (IR Latency Timer1 REG.)
		0022h	IRLT2R (IR Latency Timer2 REG.)
		0023h	IRLT3R (IR Latency Timer3 REG.)
		0024h	IRLIV0R(IR LED Indicator and Rx value0 REG.)
		0025h	IRLIV1R (IR LED Indicator and Rx value1 REG.) (unused)
		0026h	IRLIV2R (IR LED Indicator and Rx value2 REG.) (unused)
		0027h	IRLIV3R (IR LED Indicator and Rx value3 REG.) (unused)
		0028h	IRCS0R(IR Clock Speed0 REG.)
		0029h	IRCS1R (IR Clock Speed1 REG.)
		002Ah	IRCS2R (IR Clock Speed2 REG.) (unused)
		002Bh	IRCS3R (IR Clock Speed3 REG.) (unused)
		002Ch	IRPM0R(IR Power management REG.)
		002Dh	IRPM1R (IR Power management REG.) (unused)
		002Eh	IRPM2R (IR Power management REG.) (unused)
		002Fh	IRPM3R (IR Power management REG.) (unused)
		0030h	IRIS0R(Interrupt status read back0 REG.)
		0031h	IRIS1R (Interrupt status read back1 REG.) (unused)
		0032h	IRIS2R (Interrupt status read back2 REG.) (unused)
		0033h	IRIS3R (Interrupt status read back3 REG.) (unused)
		0034h	IRIE0R (Interrupt enable read back0 REG.)
		0035h	IRIE1R (Interrupt enable read back1 REG.) (unused)
		0036h	IRIE2R (Interrupt enable read back2 REG.) (unused)
		0037h	IRIE3R (Interrupt enable read back3 REG.) (unused)

Block Name	Base Address	Offset	Register Name
IrDA	0x0080	0000h	TXFL0R(TX Frame Length0 REG.)
	(TXFL FIFO)	0001h	TXFL1R(TX Frame Length1 REG.)
		0002h	Unused
		0003h	TXSR(TX Status REG.)
		0004h	TXFA0R(TX Frame Address0 REG.)
		0005h	TXFA1R(TX Frame Address1 REG.)
		0006h	TXFA2R(TX Frame Address2 REG.)
		0007h	TXFA3R(TX Frame Address3 REG.)
		0008h	TXSIR(TX Status IncrementREG.)
		0009h	TXFCR(TX Frame Count REG)
IrDA	0x0090	0000h	RXFL0R(RX Frame Length0 REG.)
	(RXFL FIFO)	0001h	RXFL1R(RX Frame Length1 REG.)
		0002h	Unused
		0003h	RXSR(RX Status REG.)
		0004h	RXFA0R(RX Frame Address0 REG.)
		0005h	RXFA1R(RX Frame Address1 REG.)
		0006h	RXFA2R(RX Frame Address2 REG.)
		0007h	RXFA3R(RX Frame Address3 REG.)
		0008h	RXSIR(RX Status IncrementREG.)
Global Control	0x00A0	0000h	MTDR (Memory Transmit Data REG) Write Only
		0000h	MRDR(Memory Receive Data REG) Read Only
		0001h	MCR(Memory Control REG.)
		0002h	GISR(Global Interrupt Status REG.)
		0003h	IRSR (IR Select REG.)
		0004h	IOR(Ir Output REG)
		0005h	IIR(Ir Input REG)
		0006h	ISIER(Ir Sir Interupt Enable REG)
		0007h	ISISR(Ir Sir Interupt Status REG)
DMA Control	0x00B0	0000h	DMACR(DMA Control REG)
Remote Control	0x00C0	0000h	RCCCLR(Remote Control Carrier Count Low REG)
		0001h	RCCCHR(Remote Control Carrier Count High REG)
		0002h	RCLLR(Remote Control Length Low REG.)
		0003h	RCLHR(Remote Control Length High REG.)
		0004h	RCCR(Remote Control Control REG)
		0005h	RCCRCLR(Remote Control Carrier RX Count Low REG)
		0006h	RCCRCHR (Remote Control Carrier RX Count High REG)
Timer Control	0x00D0	0000h	TSSR0(Timer Source Setting REG.0)
		0001h	TIER0(Timer Interrupt Enable REG.0)
		0002h	TCSR0(Timer Contorol Status REG.0)
		0003h	TCMLR0(Timer Compare Mach Low REG.0)
		0004h	TCMHR0(Timer Compare Mach High REG.0)
		0005h	TCLR0(Timer Count Low REG.0)
		0006h	TCHR0(Timer Count High REG.0)
	0x00E0	0000h	TSSR1(Timer Source Setting REG.1)
		0001h	TIER1(Timer Interrupt Enable REG.1)
		0002h	TCSR1(Timer Contorol Status REG.1)
		0003h	TCMLR1(Timer Compare Mach Low REG.1)
		0004h	TCMHR1(Timer Compare Mach High REG.1)
		0005h	TCLR1(Timer Count Low REG.1)
		0006h	TCHR1(Timer Count High REG.1)
	0x00F0	0000h	TSSR2(Timer Source Setting REG.2)
		0001h	TIER2(Timer Interrupt Enable REG.2)
		0002h	TCSR2(Timer Contorol Status REG.2)
		0003h	TCMLR2(Timer Compare Mach Low REG.2)
		0004h	TCMHR2(Timer Compare Mach High REG.2)
		0005h	TCLR2(Timer Count Low REG.2)
		0006h	TCHR2(Timer Count High REG.2)

Absolute Maximum Ratings

For implementations where case to ambient thermal resistance is ≤ 50°C/W.

Parameter	Symbol	Min.	Max.	Units
Core Power Supply Voltage	VDDK	-0.3	VIO+0.3	V
Clock Power Supply Voltage	VDDC	-0.3	3.63	V
IO Power Supply Voltage	VIO	-0.3	3.63	V
Input Output Voltage	VI/VO	-0.3	3.63	V
Operating Environnent Temperature	TA	-40	85	℃
Storage Temperature	TS	-40	150	℃

Electrical Specifications (DC)

Specifications (Min. & Max. values) hold over the recommended operating conditions unless otherwise noted. Unspecified test conditions may be anywhere in their operating range and VIO = 3.3+0.33V

VIO= 3.3+/-0.33V, TA=-40 to +85°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Core Power Supply	VDDK	1.62	1.8	1.98	V	
Clock Power Supply	VDDC	2.97	3.3	3.63	V	
IO Power Supply	VIO	2.97	3.3	3.63	V	
Input Low Voltage	VIL			0.8	V	LVTTL
Input High Voltage	VIH	2.0			V	LVTTL
Switch Threshold	Vt		1.5		V	LVTTL
Schmitt-Trigger –ve Threshold Voltage	Vt-	0.8	1.1		V	LVTTL
Schmitt- Trigger +ve Threshold Voltage	Vt+		1.6	2.0	V	LVTTL
Input Leakage Current	IIN	-10	±1	10	μA	VI=VIO or GND
Tri-State Output Leakage Current	IOZ	-10	±1	10	μA	VI=VIO or GND
Output Low Voltage	VOL			0.4	V	IOL = 2 ~16mA
Output High Voltage	VOH	2.4			V	IOH = 2 ~16mA
Input Pull-Down Resistance	RPD	40	75	190	kΩ	VIN =VIO
Current (VFIR running state) – VDDK	Ioz1k	18.6	20.5	22.5	mA	SD:High
Current (IDLE state) – VDDK	IOZ2k	18.0	20.3	22.0	mA	SD:High
Current (VFIR running state) – VIO1	IOZ1IO1			940	μA	SD:High
Current (IDLE state) – VIO1	IOZ2IO1		14	30	μA	SD:High
Current (VFIR running state) – VIO2	IOZ1IO2			52	μA	SD:High
Current (IDLE state) – VIO2	IOZ2IO2		0.1	1	μA	SD:High
Current (IDLE state) – VIO3	IOZ2IO3			38	μA	SD:High
Clock Power Supply Current-VDDC	IOZ1C	4.01	4.8	5.93	mA	Capacitor 20pF

VIO= 2.5+/-0.25V, TA=-40 to +85°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Core Power Supply	VDDK	1.62	1.8	1.98	V	
Clock Power Supply	VDDC	2.97	3.3	3.63	V	
IO Power Supply	VIO	2.25	2.5	2.75	V	
Input Low Voltage	VIL			0.25*VIO	V	CMOS
Input High Voltage	VIH	0.625*VIO			V	CMOS
Switch Threshold	Vt		1.15		V	CMOS
Schmitt-Trigger –ve Threshold Voltage	Vt-	0.25*VIO	0.94		V	CMOS
Schmitt- Trigger +ve Threshold Voltage	Vt+		1.4	0.625*VIO	V	CMOS
Input Leakage Current	IIN	-10	±1	10	µA	VI=VIO or GND
Tri-State Output Leakage Current	IOZ	-10	±1	10	µA	VI=VIO or GND
Output Low Voltage	VOL			0.4	V	IOL = 1.1 ~8.8mA
Output High Voltage	VOH	1.85			V	IOH = 1.1 ~8.8mA
Input Pull-Down Resistance	RPD	45	115	290	kΩ	VIN =VIO

VIO= 1.8+/-0.18V, TA=-40 to +85°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Core Power Supply	VDDK	1.62	1.8	1.98	V	
Clock Power Supply	VDDC	2.97	3.3	3.63	V	
IO Power Supply	VIO	1.62	1.8	1.98	V	
Input Low Voltage	VIL			0.3*VIO	V	CMOS
Input High Voltage	VIH	0.7*VIO			V	CMOS
Switch Threshold	Vt		0.85		V	CMOS
Schmitt-Trigger –ve Threshold Voltage	Vt-	0.3*VIO	0.65		V	CMOS
Schmitt- Trigger +ve Threshold Voltage	Vt+		1.08	0.7*VIO	V	CMOS
Input Leakage Current	IIN	-10	±1	10	µA	VI=VIO or GND
Tri-State Output Leakage Current	IOZ	-10	±1	10	µA	VI=VIO or GND
Output Low Voltage	VOL			0.4	V	IOL = 0.7 ~5.6mA
Output High Voltage	VOH	0.75*VIO			V	IOH = 0.7 ~5.6mA
Input Pull-Down Resistance	RPD	80	210	510	kΩ	VIN =VIO

Shutdown Currents (Internal Clock is Used) [1]

Parameter	Min.	Typ.	Max.	Unit	Conditions	Note
Shutdown Current 1 (VDDK)	17.8	18.8	19.7	μA	/SD: LOW CLKSEL: LOW CLKIN: LOW	External quartz crystal is kept under oscillation
Shutdown Current 2 (VDDK)		0.4		μA	/SD: LOW CLKSEL: HIGH CLKIN: LOW	External quartz crystal is suspending oscillation
Clock Power Supply Current (VDDC)		0.1		μA	/SD: LOW CLKSEL: HIGH CLKIN: LOW	
Shutdown Current (VIO1)		0.1		μA	/SD: LOW CLKSEL: HIGH CLKIN: LOW	
Shutdown Current (VIO2)		0.1		μA	/SD: LOW CLKSEL: HIGH CLKIN: LOW	
Shutdown Current (VIO3)		0.1		μA	/SD: LOW CLKSEL: HIGH CLKIN: LOW	

Shutdown Currents (External Clock is Used) [1]

Parameter	Min.	Typ.	Max.	Unit	Conditions	Note
Shutdown Current 3 (VDDK)		13.2	21.9	μA	/SD: LOW CLKSEL: HIGH CLKIN: 48MHz /XTALIN: LOW	
Clock Power Supply Current (VDDC)		0.1		μA	/SD: LOW CLKSEL: HIGH LKIN: 48MHz /XTALIN: LOW	
Shutdown Current (VIO1)		0.1		μA	/SD: LOW CLKSEL: HIGH CLKIN: 48MHz /XTALIN: LOW	
Shutdown Current (VIO2)		0.1		μA	/SD: LOW CLKSEL: HIGH CLKIN: 48MHz /XTALIN: LOW	
Shutdown Current (VIO3)			8.5	μA	/SD: LOW CLKSEL: HIGH CLKIN: 48MHz /XTALIN: LOW	

(1) Test Conditions:

- /RESET = HIGH (VIO1)
- A[7:0] = Must be driven either HIGH (VIO1) or LOW (0V)
- D[7:0] = Must be driven either HIGH (VIO1) or LOW (0V)
- /CS = HIGH (VIO1)
- /WE = HIGH (VIO1)
- /OE = HIGH (VIO1)
- IrRXD0 = HIGH (VIO2)

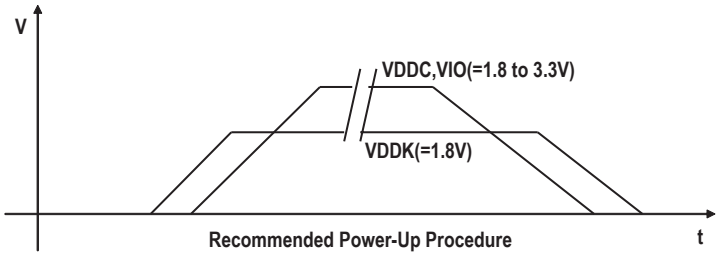
Clock Standards

Standard values of the system clock input

Frequency: 48MHz ± 100ppm

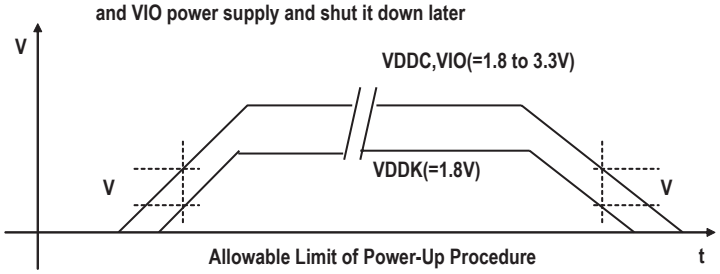
Input Duty: Must be within 50% ± 5%.

Power-up Procedures



Recommended Power-Up Procedure

Turn on the core power supply VDDK before you turn on the VDDC and VIO power supply and shut it down later

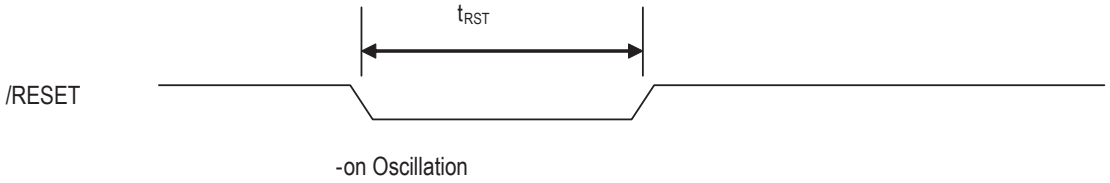


Allowable Limit of Power-Up Procedure

If you want to turn on the core power supply VDDK after you turn on VDDC and VIO power supply, you must keep V = VIO-VDDK < 0.5V during the time before VDDK becomes stable

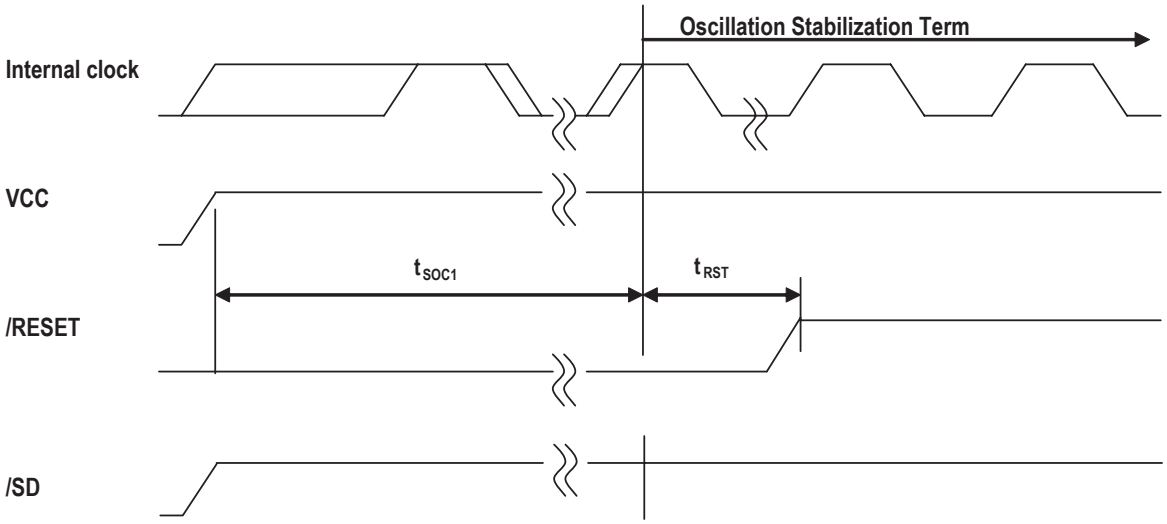
A.C Timing

1) Reset Input Timing



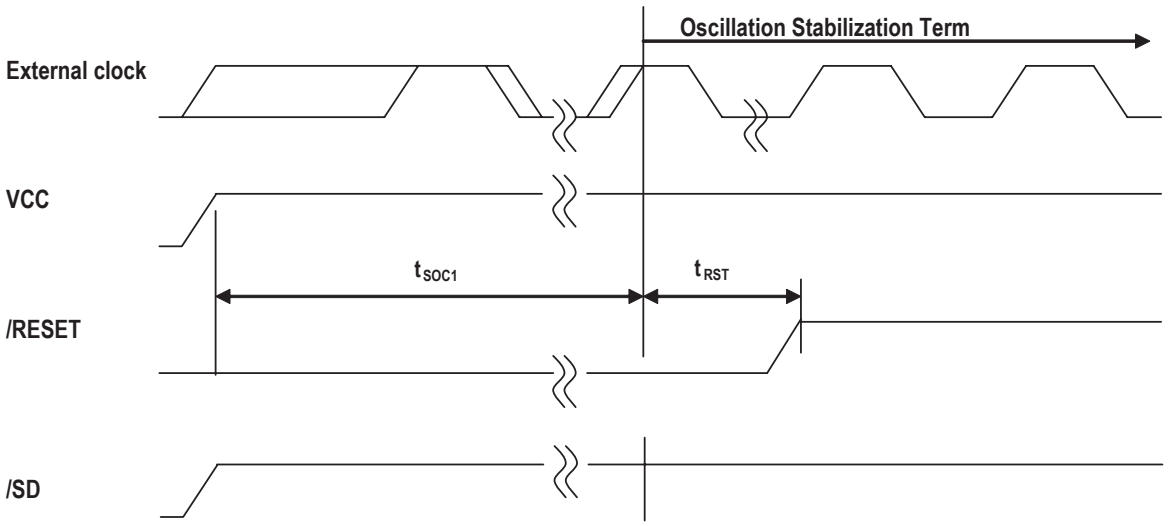
Item	Symbol	Min	Typ	Max	Unit
Reset Pulse Width	tRST		50		ns

2) Stabilization Time of Power-on Oscillation (Internal Clock is Used)



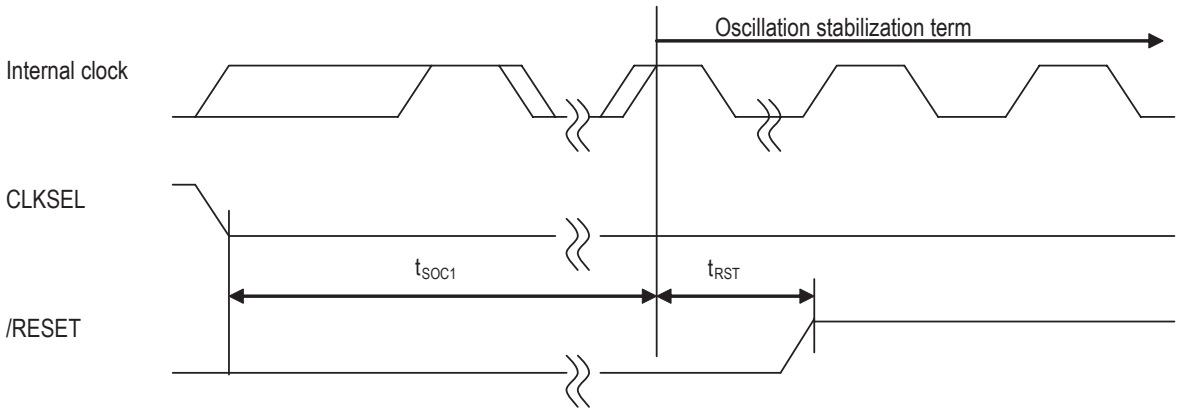
Parameter	Symbol	Typical Value
Power-on Oscillation stabilization time	t_{SOC1}	20ms
Reset Pulse Width	t_{RST}	50ns

Stabilization Time of Power-on Oscillation (External Clock is Used)



Parameter	Symbol	Typical Value
Power-on Oscillation stabilization time	t_{SOC1}	50ns
Reset Pulse Width	t_{RST}	50ns

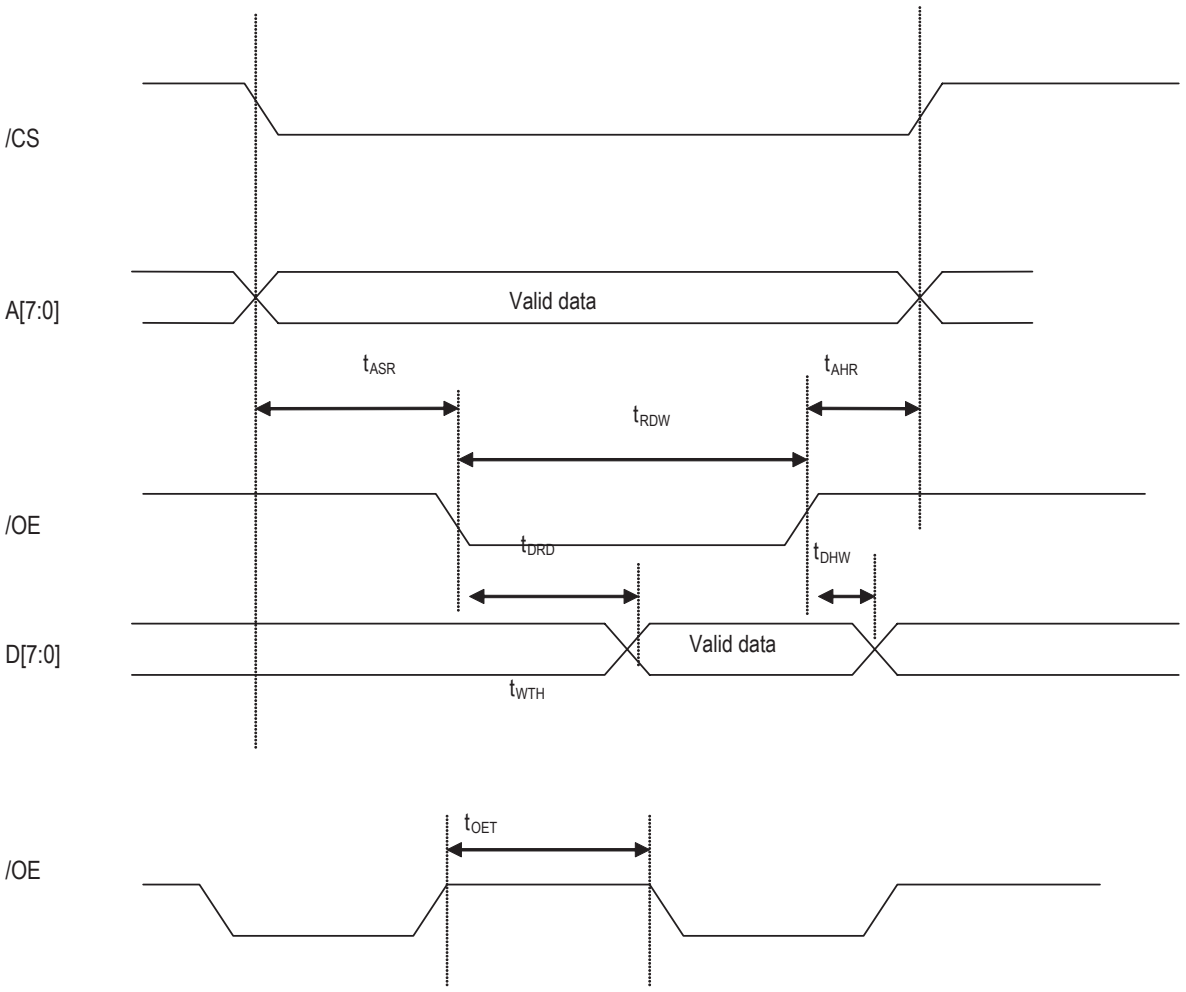
3) Return Oscillation Stabilization Time via CLKSEL



Item	Symbol	Min	Typ	Max	Unit
CLKSEL return oscillation stabilization time	TSOC1		20		msec

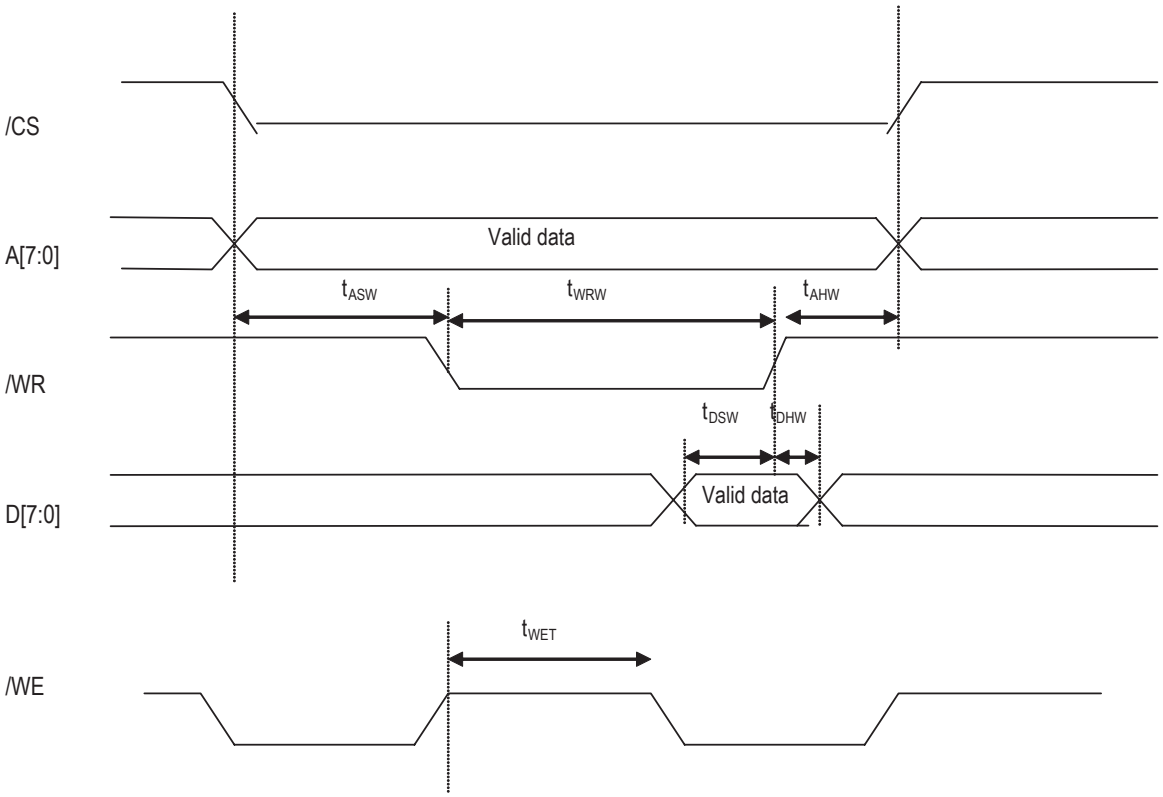
Oscillation stabilization time when the quartz crystal is connected

4) Read Operations



Item	Symbol	Min	Max	Unit
Address setting time	tASR	0		ns
Address retaining time	tAHR	0		ns
Data delay time	tDRD		80	ns
Read pulse amplitude	tRDW	80		ns
Output retaining time	tDHW	0		ns
Turnaround time	tOET	50		ns

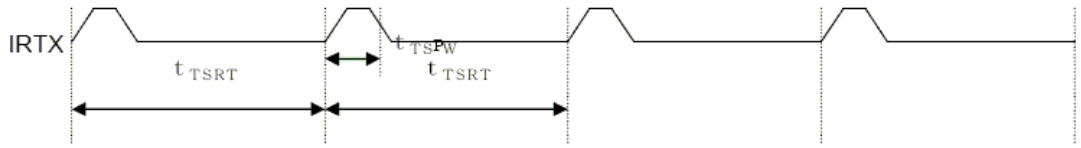
5) Write Operations



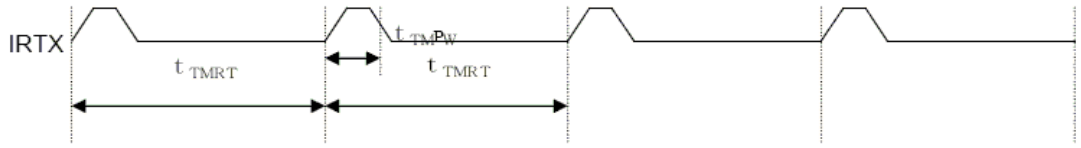
Item	Symbol	Min	Max	Unit
Address setting time	tASW	0		ns
Address retaining time	tAHW	0		ns
Write pulse amplitude	tWRW	50		ns
Data setting time	tDSW	10		ns
Data retaining time	tDHW	0		ns
Turnaround time	tWET	70		ns

6) Send Pulse Amplitude

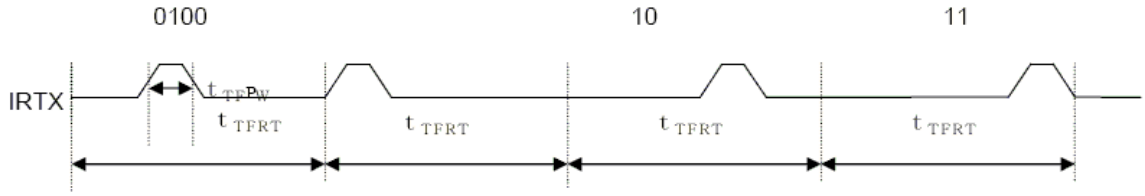
• SIR



• MIR

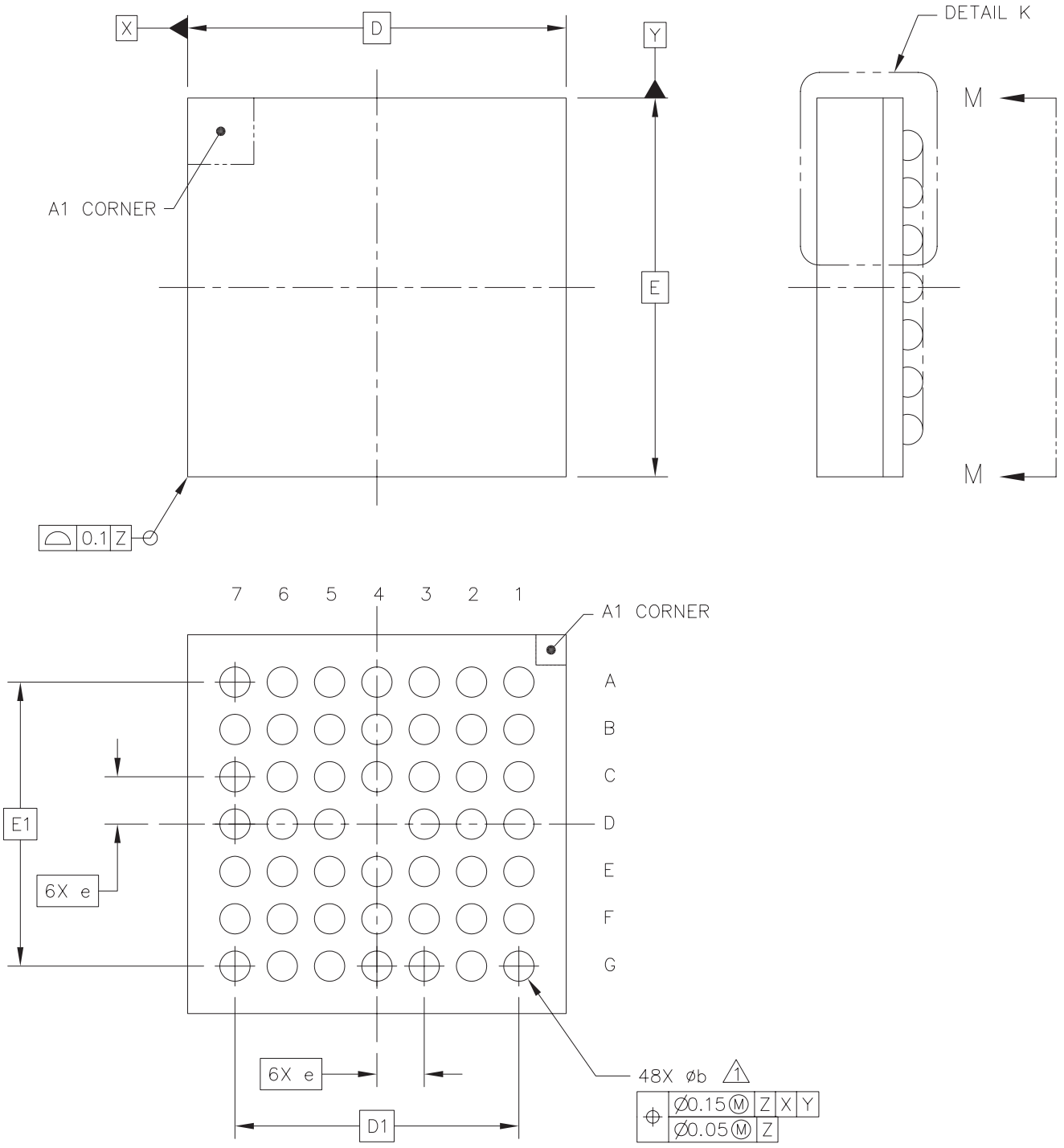


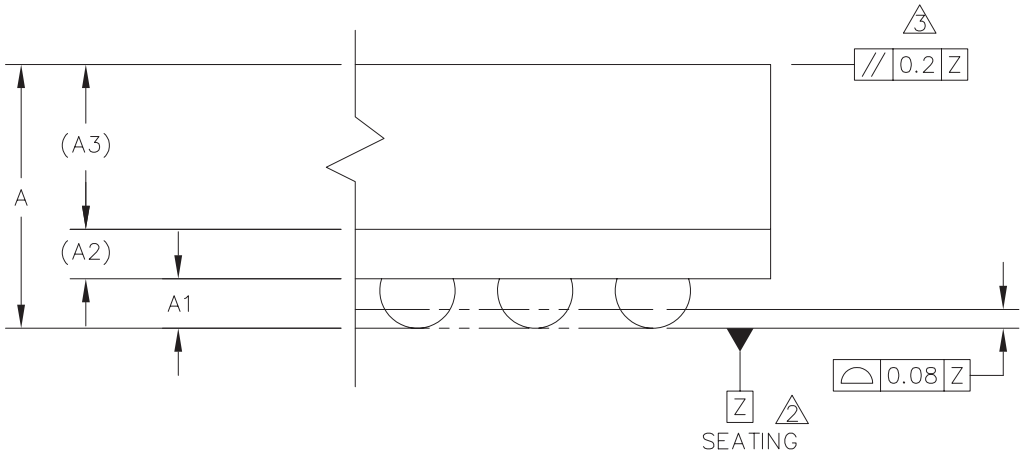
• FIR



Item		Symbol	Conditions	Min	Typ	Max	Unit
SIR send pulse amplitude	9,600bps	tTSPW	3/16 pulse amplitude	20.7	20.8	20.9	µs
	19,200bps			10.3	10.4	10.5	µs
	38,400bps			5.16	5.18	5.19	µs
	57,600bps			3.43	3.40	3.47	µs
	115,200bps			1.70	1.72	1.74	µs
	1.6µS		pulse amplitude 1.6µs fixed Typ register IRPLC2R,IRPLC3R PW[4:0] = 0x4E 20.8nsec Step changeable	1.665	1.72	1.769	µs
SIR send cycle	9,600bps	tTSRT		104.0	104.1	104.2	µs
	19,200bps			52.0	52.1	52.2	µs
	38,400bps			25.2	26.0	26.1	µs
	57,600bps			17.2	17.3	17.4	µs
	115,200bps			8.5	8.6	8.7	µs
MIR send pulse amplitude	1.152Mbps	tTMPW	Typ register IRPLC2R,IRPLC3R PW[4:0] = 0x4E 20.8nsec Step changeable	226	227	228	s
MIR send cycle	1.152Mbps	tTMRT		854	868	875	s
FIR send pulse amplitude	4Mbps	tTFPW		124	125	126	s
FIR send cycle	4Mbps	tTFRT			500		s
VFIR send pulse amplitude	16Mbps	tTFPW		41.0	41.7	43.0	s

ASDL-7021 Package Dimension:





DETAIL K
SCALE 30/1
(ROTATE 90°)

DIM	MIN.	NOR.	MAX.
A	---		1.2
A1	0.16		0.26
A2		0.21 REF	
A3		0.7 REF	
b	0.27		0.37
D	3.9	4	4.1
E	3.9	4	4.1
e		0.5 BSC	
D1	2.85	3	3.15
E1	2.85	3	3.15

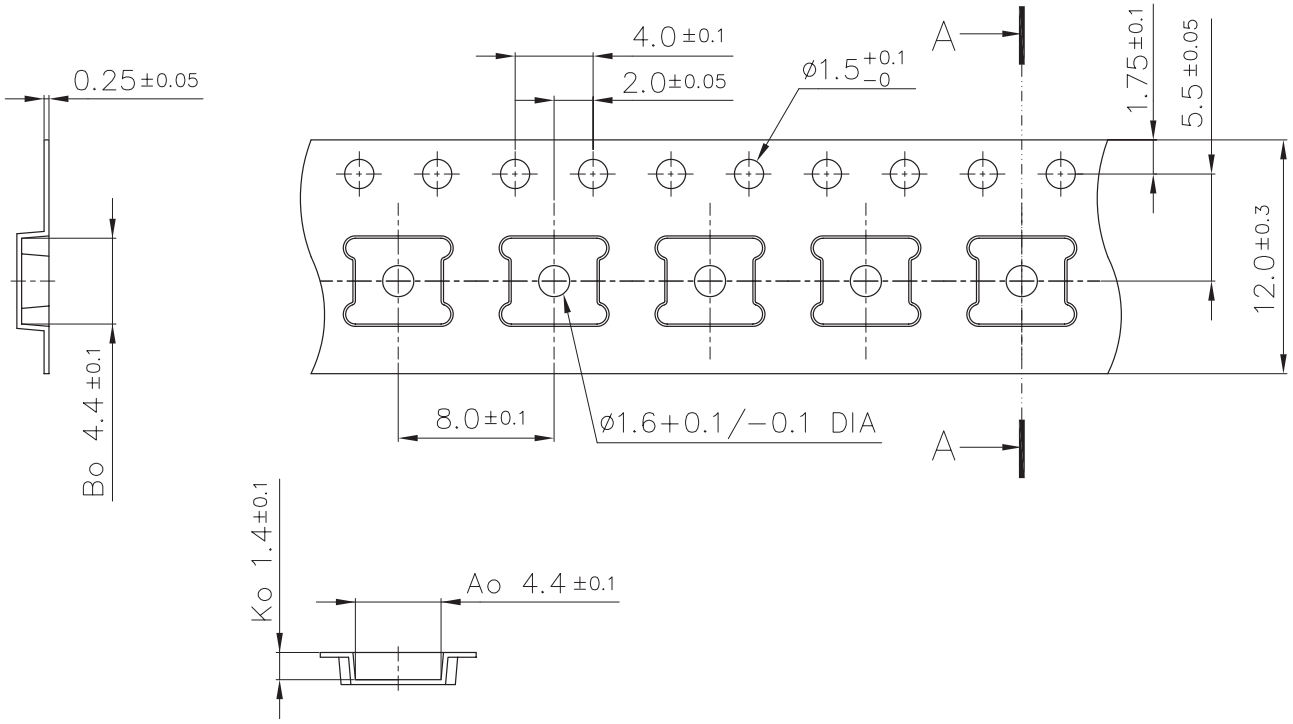
NOTES

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
2. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

UNIT	DIMENSION AND TOLERANCES	REFERENCE DOCUMENT
MM	ASME Y14.5M	---

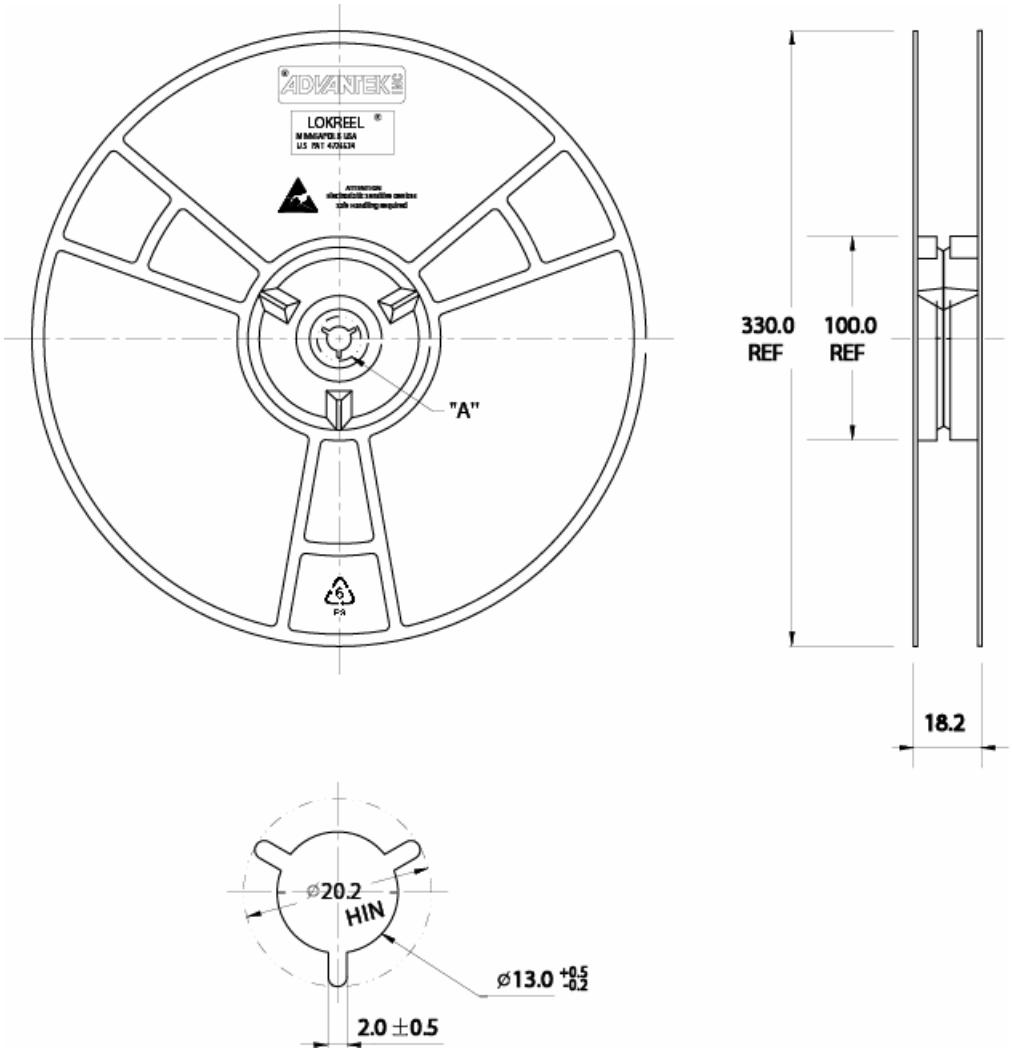
TITLE:	COMPANY	ASECL
TFBGA 48 BALLS 4X4X1.2 PKG 0.5 PITCH POD (FOR FARADAY ONLY)	SHEET	2 OF 3

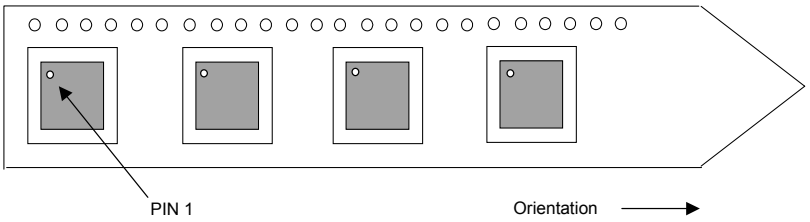
ASDL-7021 Tape and Reel Dimension:

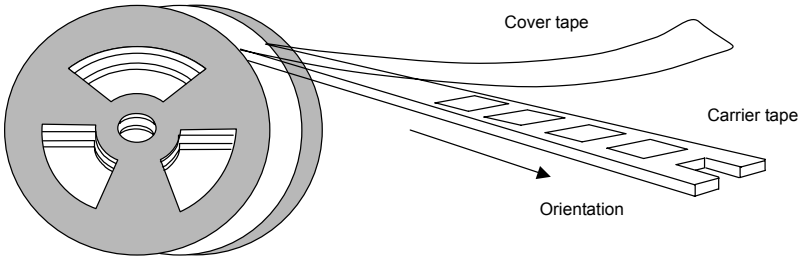


NOTES:

1. MATERIAL: CONDUCTIVE POLYSTYRENE.
2. DIM IN MM.
3. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2.
4. CAMBER NOT TO EXCEED 1 MM IN 100 MM.
5. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE.
6. SURFACE RESISTIVTY LESS THAN OR EQUAL TO 1.0X10E7 OHMS/SQ.


LOKREEL
"A"
330.0
REF
100.0
REF
18.2
ø20.2
MIN
ø13.0 +0.5 -0.2
2.0 ±0.5


PIN 1
Orientation


Cover tape
Carrier tape
Orientation

Moisture Proof Packaging

All ASDL-7021 options are shipped in moisture proof package. Once opened, moisture absorption begins.

This part is compliant to JEDEC Level 3.

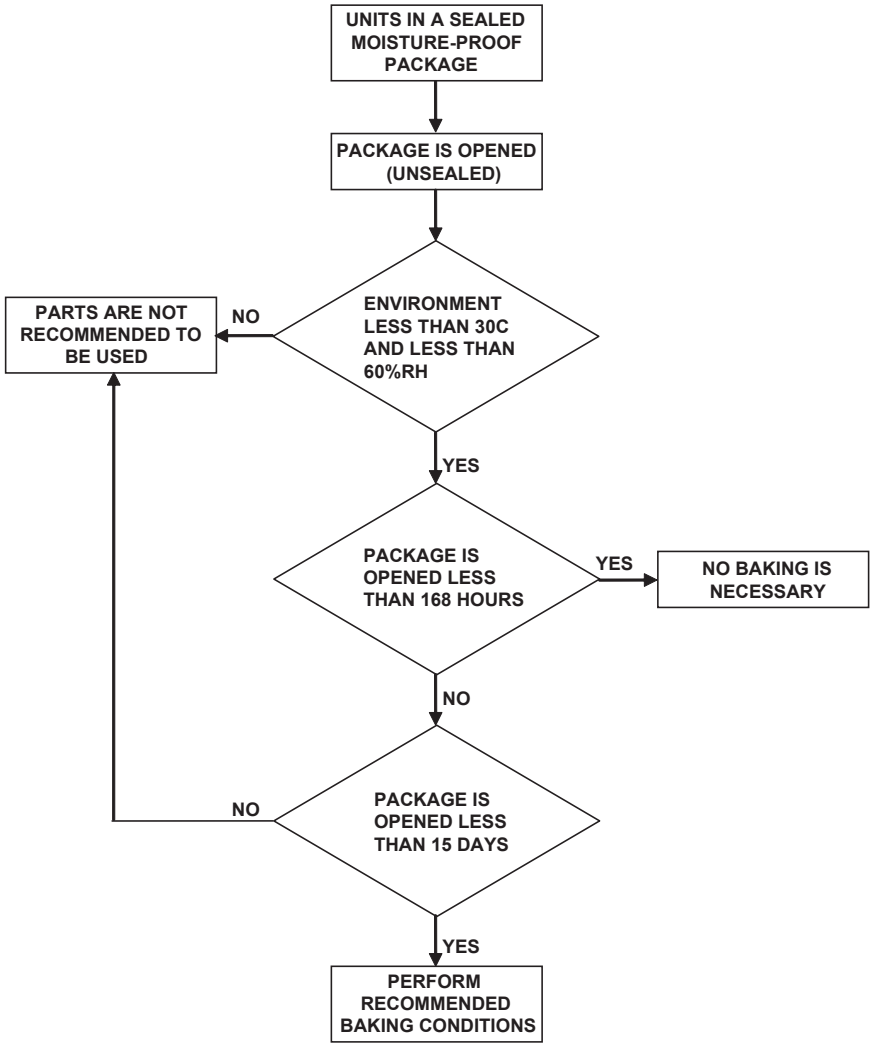


Figure 4. Baking Conditions Chart

Baking Conditions

Package	Temp	Time
In bulk	125 °C	≥ 24hours

Baking should only be done once.

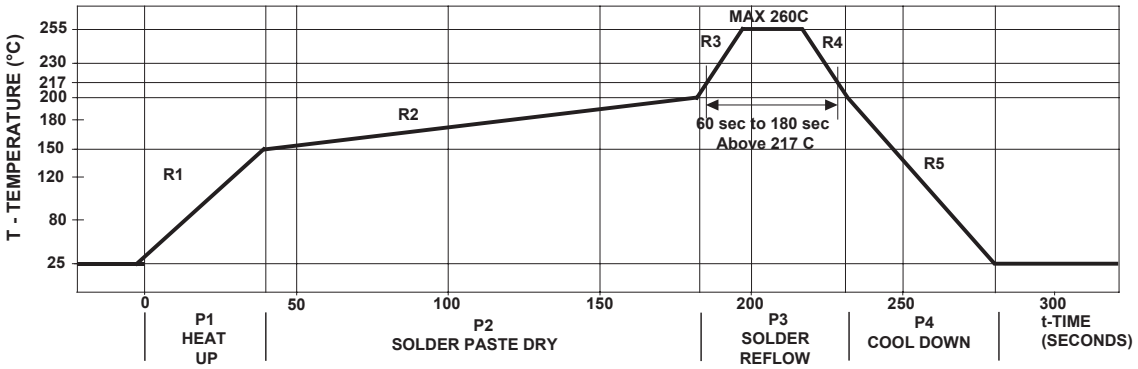
Recommended Storage Conditions

Storage Temperature	10°C to 30°C
Relative Humidity	below 60% RH

Time from unsealing to soldering

After removal from the bag, the parts should be soldered within 7 days if stored at the recommended storage conditions. If times longer than 7 days are needed, the parts must be stored in a dry box.

Recommended Reflow Profile



Process Zone	Symbol	ΔT	Maximum ΔT/Δtime or Duration
Heat Up	P1, R1	25°C to 150°C	3°C/s
Solder Paste Dry	P2, R2	150°C to 200°C	60s to 180s
Solder Reflow	P3, R3 P3, R4	200°C to 255°C 255°C to 200°C	3°C/s -6°C/s
Cool Down	P4, R5	200°C to 25°C	-6°C/s
Time maintained above 217°C		> 217°C	60s to 150s
Peak Temperature		260°C	
Time within 5°C of actual Peak Temperature		> 255°C	20s to 40s
Time 25°C to Peak Temperature		25°C to 260°C	8mins

The reflow profile is a straight-line representation of a nominal temperature profile for a convective reflow solder process. The temperature profile is divided into four process zones, each with different ΔT/Δtime temperature change rates or duration. The ΔT/Δtime rates or duration are detailed in the above table. The temperatures are measured at the component to printed circuit board connections.

In process zone P1, the PC board and ASDL-7021 pins are heated to a temperature of 150°C to activate the flux in the solder paste. The temperature ramp up rate, R1, is limited to 3°C per second to allow for even heating of both the PC board and ASDL-7021 pins.

Process zone P2 should be of sufficient time duration (100 to 180 seconds) to dry the solder paste. The temperature is raised to a level just below the liquidus point of the solder, usually 200°C (392°F).

Process zone P3 is the solder reflow zone. In zone P3, the temperature is quickly raised above the liquidus point of solder to 255°C (491°F) for optimum results. The dwell time above the liquidus point of solder should be between 20 and 40 seconds. It usually takes about 20 seconds to assure proper coalescing of the solder balls into liquid solder and the formation of good solder connections. Beyond a dwell time of 40 seconds, the intermetallic growth within the solder connections becomes excessive, resulting in the formation of weak and unreliable connections. The temperature is then rapidly reduced to a point below the solidus temperature of the solder, usually 200°C (392°F), to allow the solder within the connections to freeze solid.

Process zone P4 is the cool down after solder freeze. The cool down rate, R5, from the liquidus point of the solder to 25°C (77°F) should not exceed 6°C per second maximum. This limitation is necessary to allow the PC board and ASDL-7021 pins to change dimensions evenly, putting minimal stresses on the ASDL-7021.

Appendix A: General Application Guide for the ASDL-7021 Integrated FIR/VFIR IrDA Controller

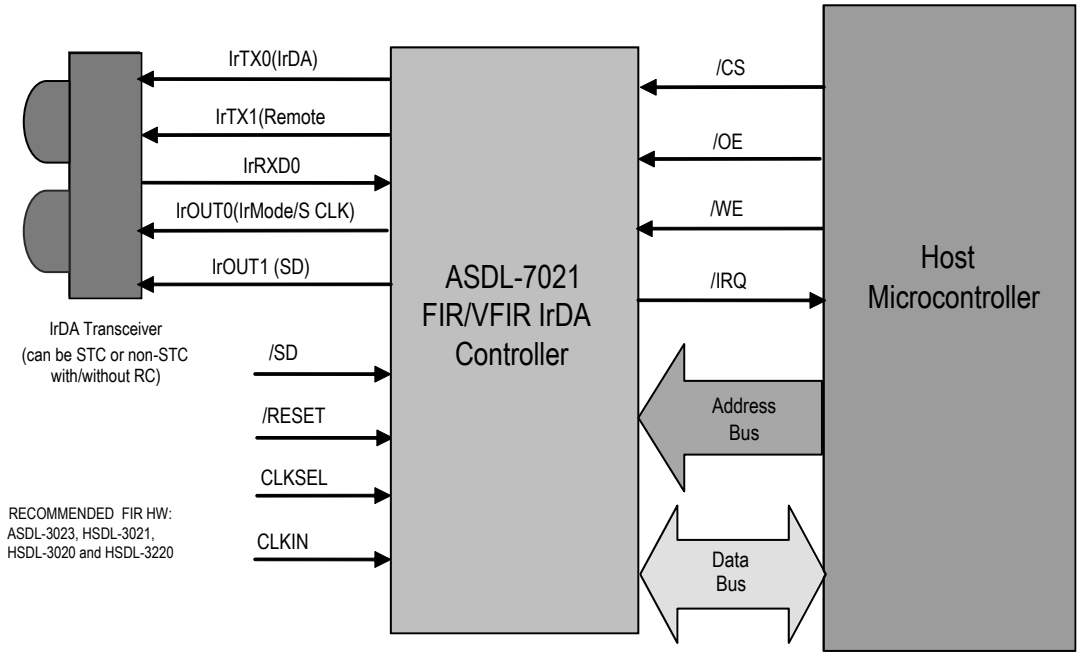


Figure A1. Block Diagram of ASDL-7021 interface with Recommended Transceiver and Host Microcontroller