STL3NK40

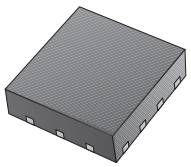
N-channel 400 V, 4.5 Ω, 2.3 A PowerFLAT™ (5x5) SuperMESH™ Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D (1)	Pw (1)
STL3NK40	400 V	< 5.5 Ω	2.3 A	75 W

1. The value is rated according to Rthj-f

- Extremely high dv/dt capability
- Improved ESD capability
- 100% avalanche rated
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability



PowerFLAT™(5x5)

Applications

- Switching application

Description

The new SuperMESH™ series of Power MOSFETs is the result of further design improvements on ST's well-established strip-based PowerMESH™ layout. In addition to significantly lower on-resistance, the device offers superior dv/dt capability to ensure optimal performance even in the most demanding applications. The SuperMESH™ devices further complement an already broad range of innovative high voltage MOSFETs, which includes the revolutionary MDmesh™ products.

Figure 1. Internal schematic diagram

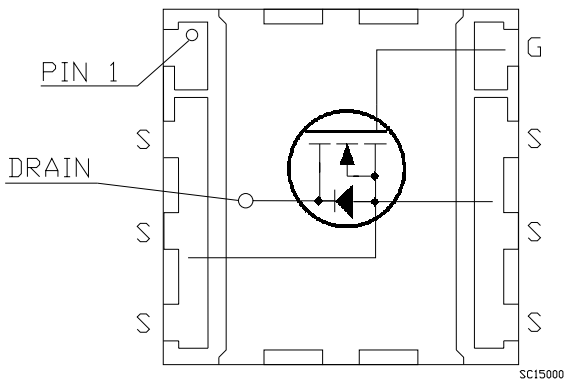


Table 1. Device summary

Order code	Marking	Package	Packaging
STL3NK40	3NK40	PowerFLAT™(5x5)	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	400	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 kΩ)	400	V
V_{GS}	Gate- source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25 ° C (steady state) Drain current (continuous) at T_C = 100°C	0.43 0.27	A A
I_{DM} (1)	Drain current (pulsed)	1.72	A
P_{TOT} (1)	Total dissipation at T_C = 25 °C (steady state)	2.5	W
P_{TOT} (2)	Total dissipation at T_C = 25 °C (steady state)	75	W
	Derating factor	0.02	W/°C
dv/dt (3)	Peak diode recovery voltage slope	4.5	V/ns
T_{stg} T_j	Storage temperature Max. operating junction temperature	-55 to 150	°C

1. When mounted on FR-4 Board of 1 inch², 2 oz Cu (t < 100 s)
2. The value is rated according to Rthj-f
3. I_{SD} < 0.43 A, di/dt< 200 A/µs, V_{DD} < 320 V

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
Rthj-f	Thermal resistance junction-foot (drain)	1.66	°C/W
Rthj-pcb(1)	Thermal resistance junction-pcb	50	°C/W

1. When mounted on FR-4 Board of 1 inch², 2 oz Cu (t < 100 s)

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	0.43	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	60	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	400			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0) V_{DS} = max rating V_{DS} = max rating, T_C = 125 °C				1 50	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			± 10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	0.8	1.6	2	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 0.22 A		4.5	5.5	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 10 V, I_D = 0.43 A	-	1.2		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	128 16 4	200 30 6	pF pF pF
R_G	Gate input resistance	f= 1 MHz Gate DC Bias = 0 Test signal level = 20 mV open drain	-	12		Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 320 V, I_D = 1.4 A, V_{GS} = 10 V *(see Figure 10)*	-	8.7 0.9 3.8	13	nC nC nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 200 V, I_D = 0.7 A,		3		ns
t_r	Rise time	R_G = 4.7 Ω, V_{GS} = 10 V	-	4	-	ns
$t_{d(off)}$	Turn-off-delay time	*(see Figure 14)*		18		ns
t_f	Fall time			16		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		0.43	A
I_{SDM} (1)	Source-drain current (pulsed)				1.72	A
V_{SD} (2)	Forward on voltage	I_{SD} = 0.43 A, V_{GS} = 0	-		1.2	V
t_{rr}	Reverse recovery time	I_{SD} = 1.4 A, di/dt = 100 A/µs		166		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 20 V	-	300		nC
I_{RRM}	Reverse recovery current	*(see Figure 19)*		3.6		A
t_{rr}	Reverse recovery time	I_{SD} = 1.4 A, di/dt = 100 A/µs		176		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 20 V, T_j = 150 °C	-	340		nC
I_{RRM}	Reverse recovery current	*(see Figure 19)*		3.8		A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

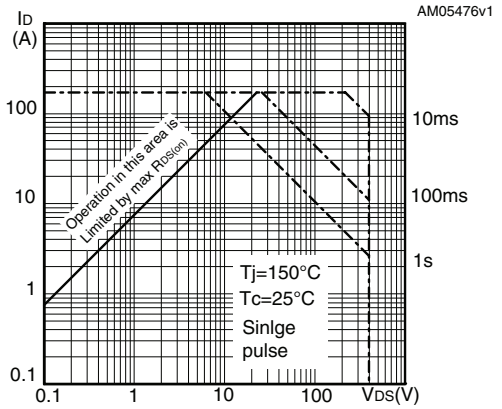


Figure 3. Thermal impedance

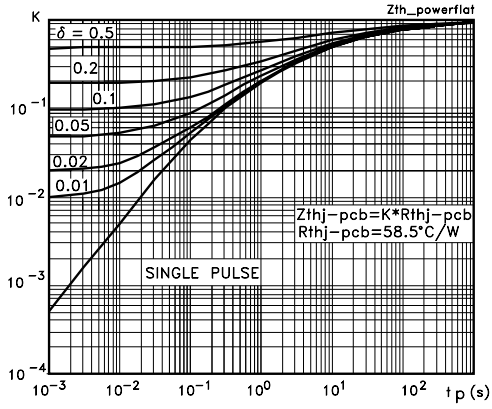


Figure 4. Saturation characteristics

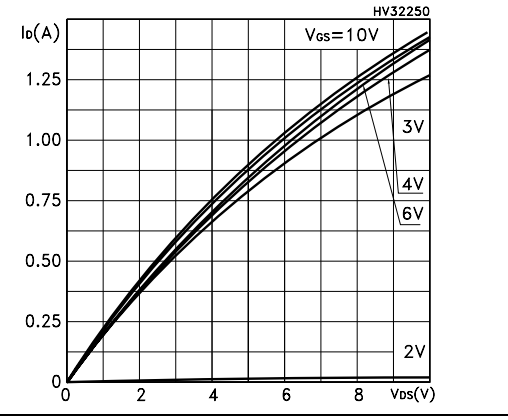


Figure 5. Transfer characteristics

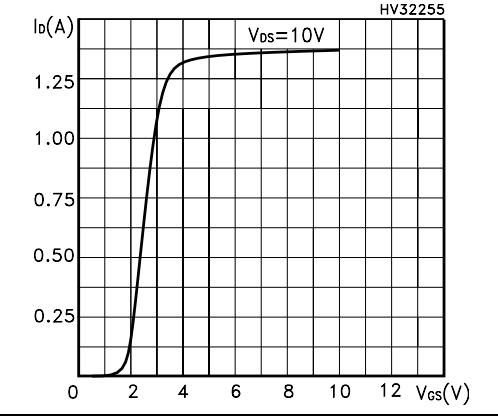


Figure 6. Output characteristics

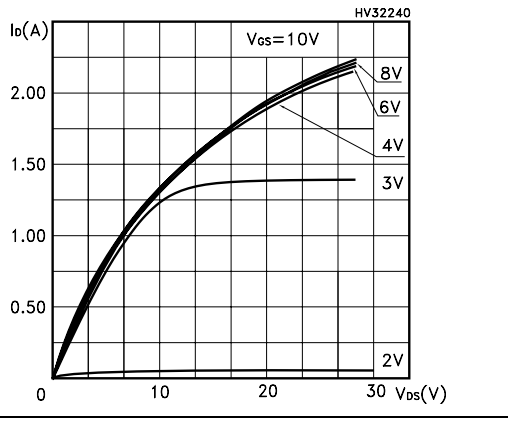


Figure 7. Static drain-source on-resistance

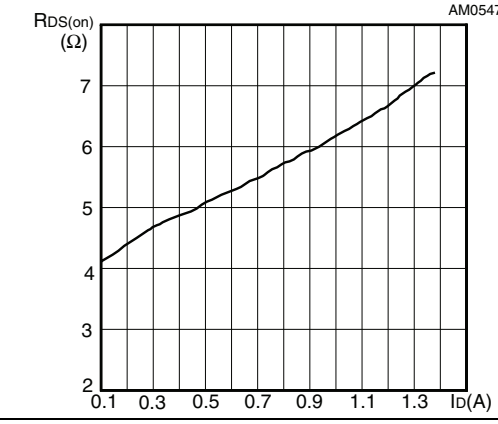


Figure 8. Gate charge vs gate-source voltage

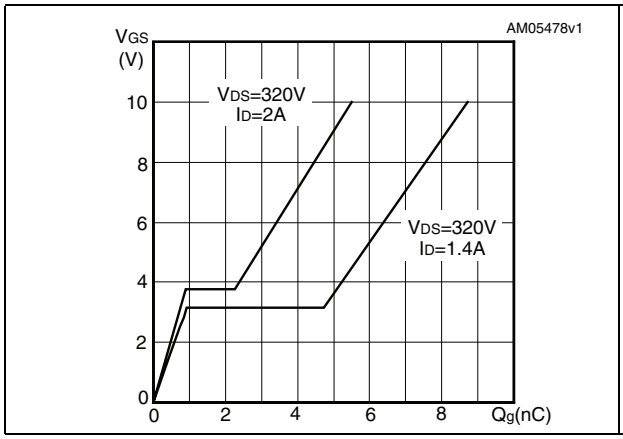


Figure 9. Capacitance variations

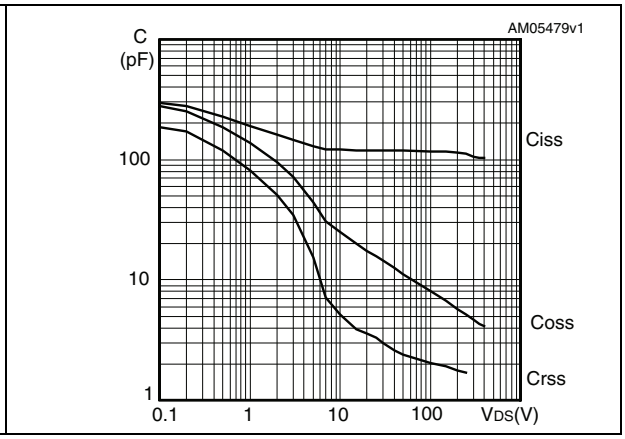


Figure 10. Transconductance

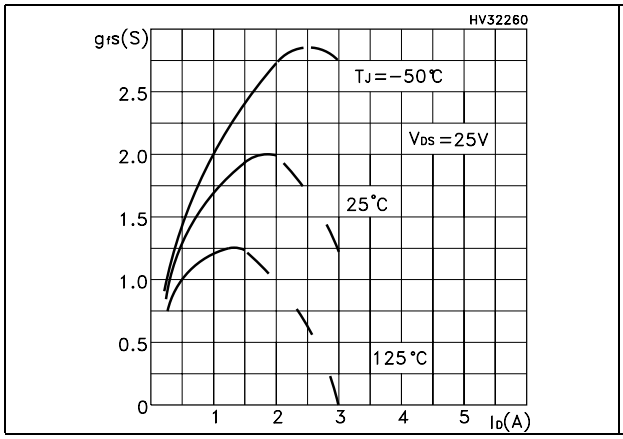


Figure 11. Normalized B_{VDSS} vs temperature

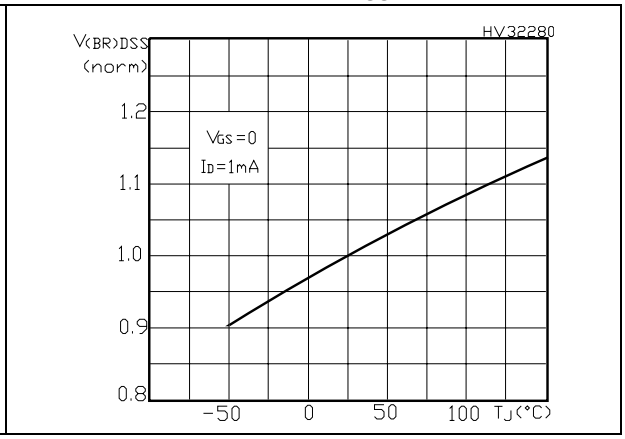


Figure 12. Normalized gate threshold voltage vs temperature

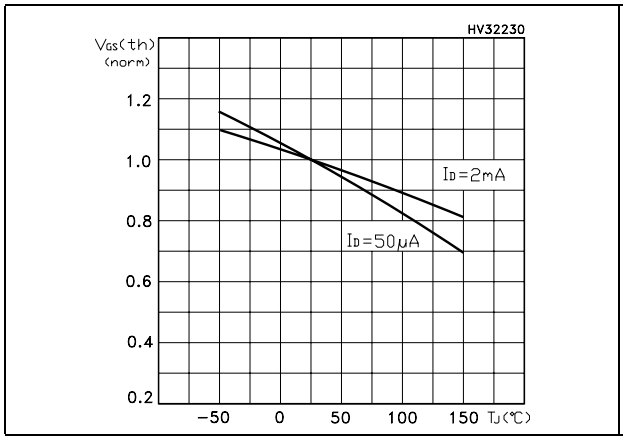
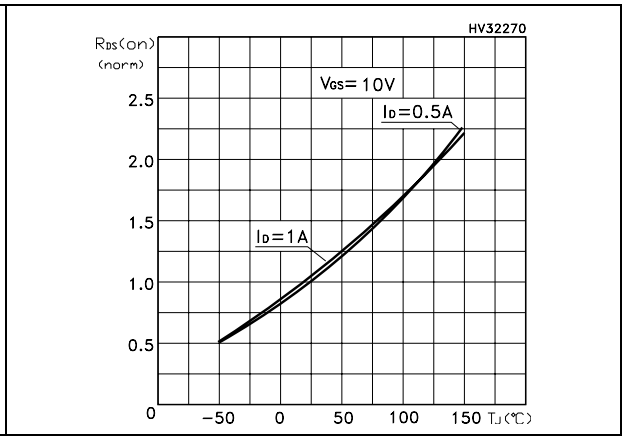


Figure 13. Normalized on-resistance vs temperature



3 Test circuits

Figure 14. Switching times test circuit for resistive load

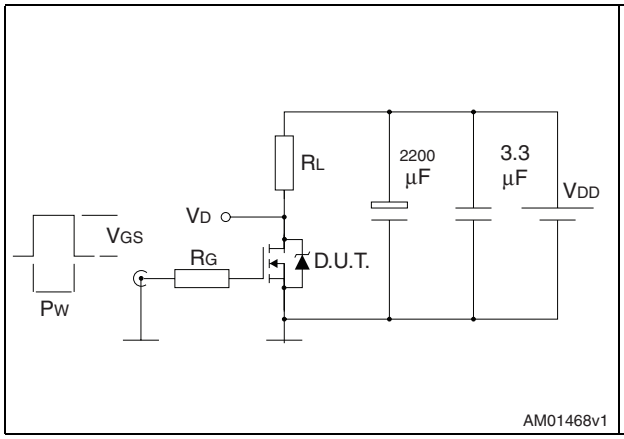


Figure 15. Gate charge test circuit

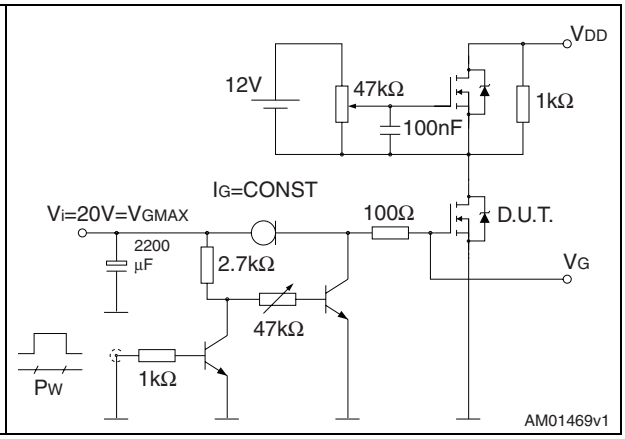


Figure 16. Test circuit for inductive load switching and diode recovery times

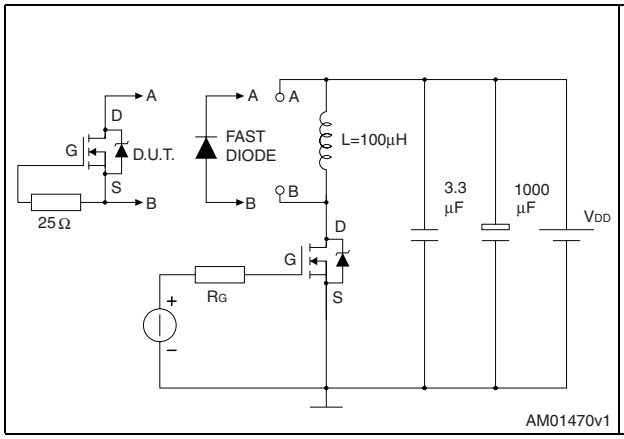


Figure 17. Unclamped inductive load test circuit

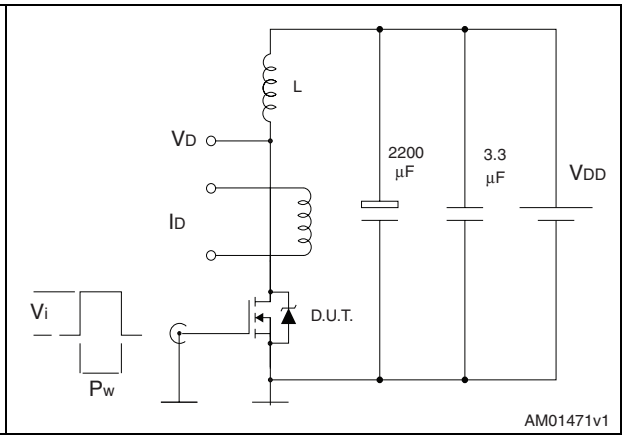


Figure 18. Unclamped inductive waveform

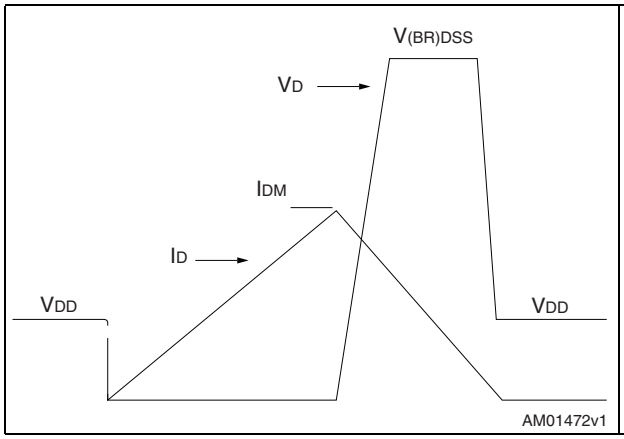
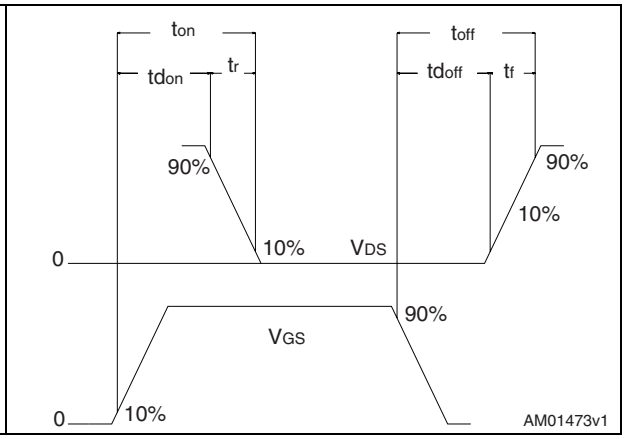


Figure 19. Switching time waveform

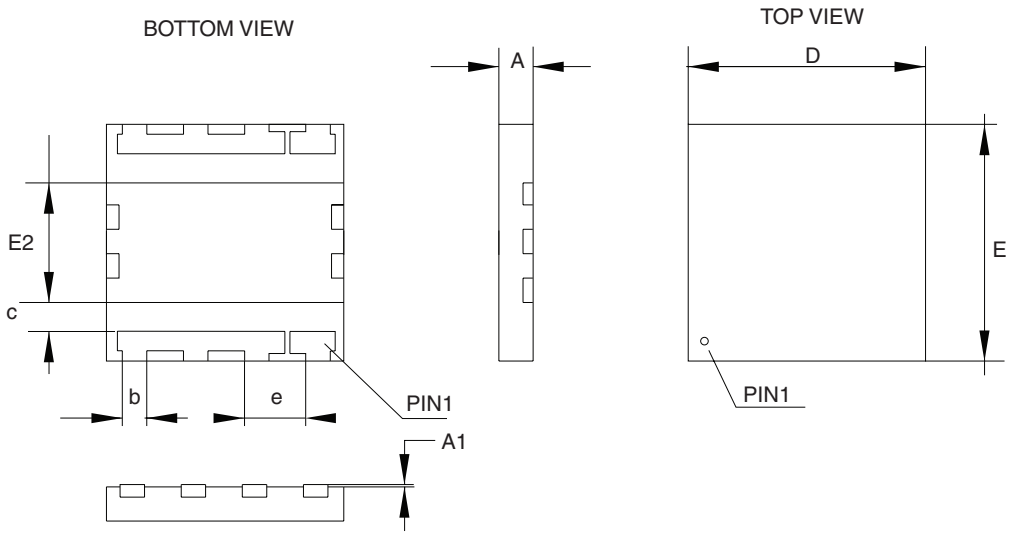


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

PowerFLAT ™(5x5) mechanical data

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1		0.02	0.05		0.0007	0.002
A3		0.24			0.009	
b	0.43	0.51	0.58	0.016	0.020	0.022
c	0.64	0.71	0.79	0.025	0.027	0.031
D		5.00			0.19	
E		5.00			0.19	
E2	2.49	2.57	2.64	0.01	0.10	0.103
e		1.27			0.05	



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
18-Sep-2009	1	First release

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