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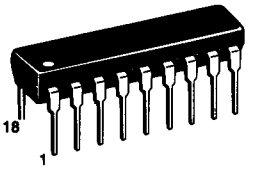
MC144143

Advance Information

Closed-Caption Decoder
CMOS

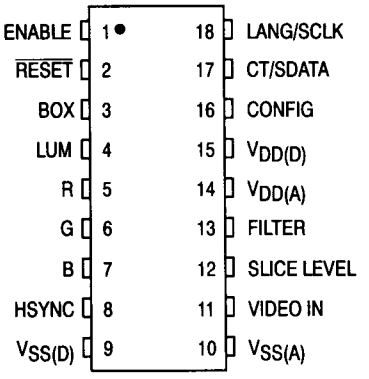


P SUFFIX
PLASTIC DIP
CASE 707

ORDERING INFORMATION

MC144143P	Plastic DIP

PIN ASSIGNMENT



The MC144143 is a line-21 closed-caption decoder for use in television receivers or set-top decoders conforming to the NTSC standard. Capability for processing and displaying all of the latest standard line-21 closed-caption format transmissions is included. The device requires a closed-caption encoded composite video signal, a horizontal sync signal, and an external keyer to produce captioned video. RGB outputs are provided, along with a luminance and a box signal, allowing simple interface to both color and black-and-white TV receivers.

Display storage is accomplished with an on-chip RAM. A modified ASCII character set, which includes several non-English characters, is decoded by an on-chip ROM. An on-screen character appears as a white or colored dot matrix on a black background.

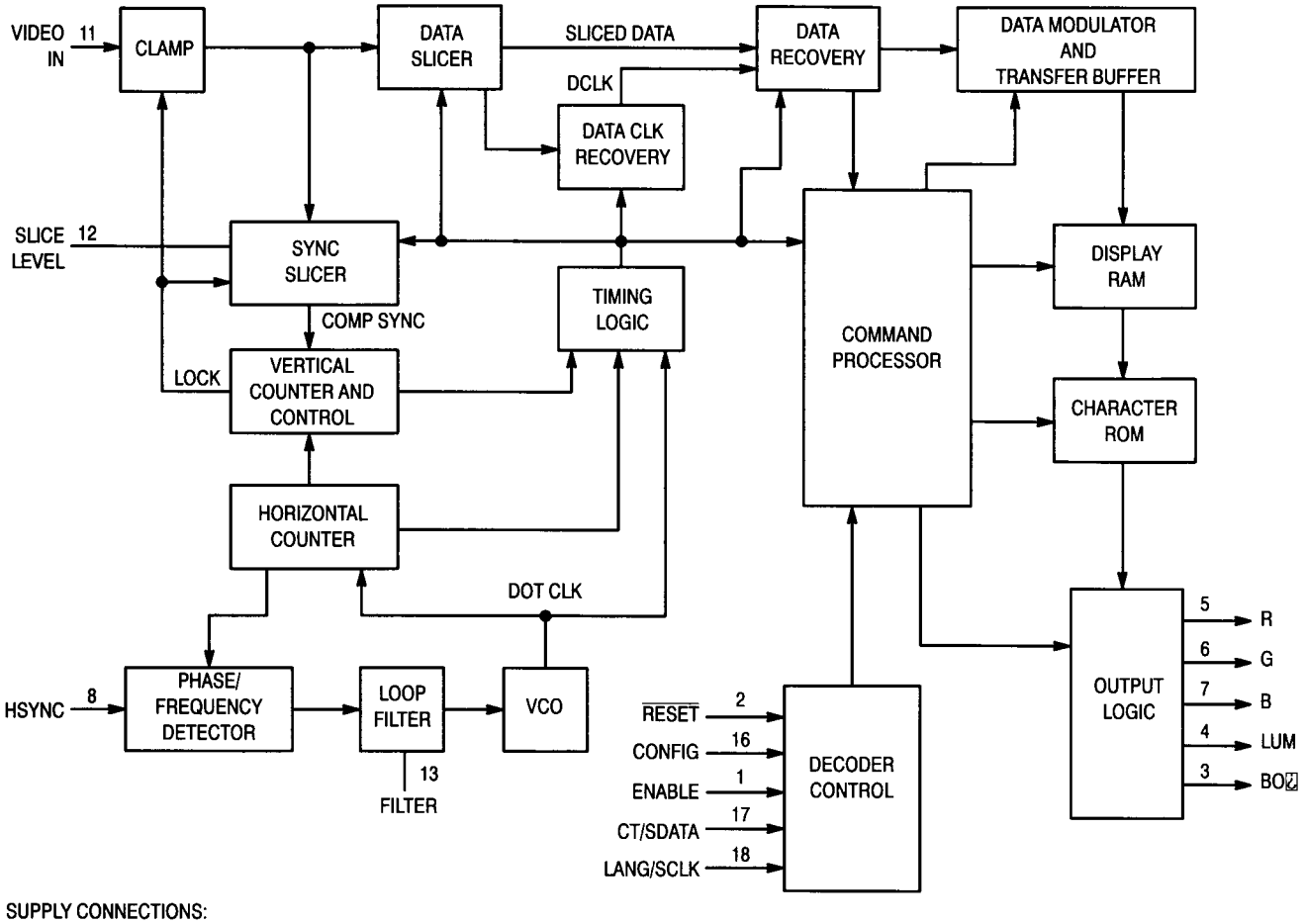
Captions (video-related information) can be up to four rows appearing anywhere on the screen and can be displayed in two modes: rollup or pop-on. With rollup captions, the row scrolls up and new information appears at the bottom row each time a carriage return is received. Pop-on captions work with two memories. One memory is displayed while the other is used to accumulate new data. A special command causes the information to be exchanged in the two memories, thus causing the entire caption to appear at once.

When text (non-video related information) is displayed, the rows contain a maximum of 32 characters over a black box which overwrites the screen. Eight rows of characters are displayed in the text mode.

An on-chip processor controls the manipulation of data for storage and display. Also controlled are the loading, addressing, and clearing of the display RAM. The processor transfers the data received to the RAM during scan lines 21 through 42. The operation of the display RAM, character ROM, and output logic circuits are controlled during scan lines 43 through 237. Several functions of the MC144143 are controlled via a port which may be configured to be serial or parallel.

- Conforms to FCC Report and Order as Amended by the Petition for Reconsideration on Gen. Doc. 91-1.
- Supports Four Different Data Channels, Time Multiplexed within the Line-21 Data Stream: Captions Utilizing Languages 1 and 2 plus Text Utilizing Languages 1 and 2
- Output Logic Provides Hardware Underline Control and Italics Slant Generation
- Single Supply, Operating Voltage Range: 4.75 to 5.25 V
- Supply Current: 20 mA (Preliminary)
- Operating Temperature Range: 0 to 70°C
- Composite Video Input Range: 0.7 to 1.4 V p-p
- Horizontal Input Polarity: Either Positive or Negative
- Internal Timing and Sync Signals Derived from On-Chip VCO

This document contains information on a new product. Specifications and information herein are subject to change without notice.



SUPPLY CONNECTIONS:
PIN 14 = $V_{DD(A)}$ = V+ FOR ANALOG SECTION
PIN 15 = $V_{DD(D)}$ = V+ FOR DIGITAL SECTION
PIN 10 = $V_{SS(A)}$ = GND FOR ANALOG SECTION
PIN 9 = $V_{SS(D)}$ = GND FOR DIGITAL SECTION

Figure 1. Block Diagram

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS* (Voltages referenced to $V_{SS(A)}$ and $V_{SS(D)}$)

Symbol	Parameter	Value	Unit
$V_{DD(A)}$	Analog DC Supply Voltage	– 0.5 to 6.0	V
$V_{DD(D)}$	Digital DC Supply Voltage	– 0.5 to 6.0	V
V_{in}	DC Input Voltage, Analog Section	– 0.5 to $V_{DD(A)}$ + 0.5	V
V_{in}	DC Input Voltage, Digital Section	– 0.5 to $V_{DD(D)}$ + 0.5	V
V_{out}	DC Output Voltage, Digital Section	– 0.5 to $V_{DD(D)}$ + 0.5	V
I_{in}	DC Input Current, per Pin	± 10	mA
I_{out}	DC Output Current, per Pin	± 20	mA
I_{DD}	DC Supply Current	± 30	mA
P_D	Power Dissipation, per Package	300	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

* Maximum ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than the maximum-rated voltages to this high-impedance circuit.

DC ELECTRICAL CHARACTERISTICS

($V_{DD(A)} = V_{DD(D)}$ = 4.75 to 5.25 V, T_A = 0 to 70°C, Voltages Referenced to $V_{SS(D)}$ Unless Otherwise Indicated)

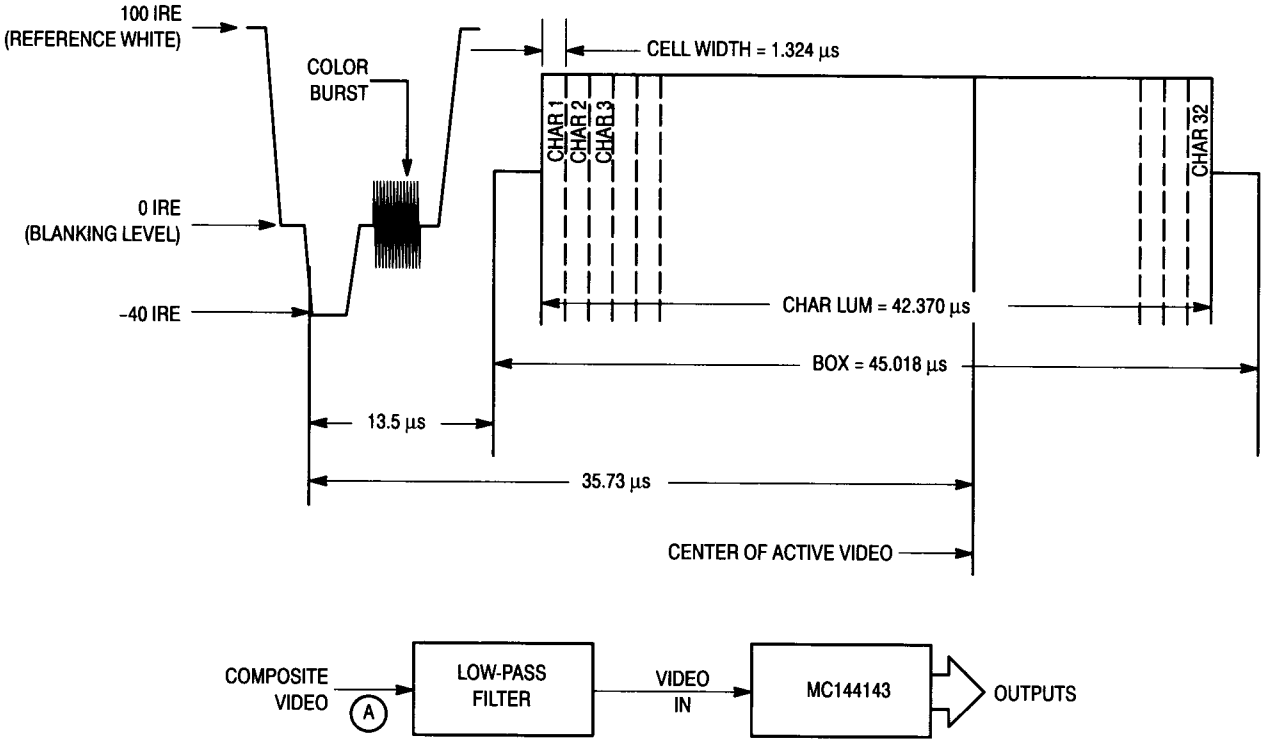
Symbol	Parameter	Test Condition	Guaranteed Limit	Unit
V_{IH}	Minimum High-Level Input Voltage (HSync, Enable, CT/SData, Lang/SClk, Config, $\overline{Reset}$)		0.7 x $V_{DD(D)}$	V
V_{IL}	Maximum Low-Level Input Voltage (HSync, Enable, CT/SData, Lang/SClk, Config, $\overline{Reset}$)		0.2 x $V_{DD(D)}$	V
V_{OH}	Minimum High-Level Output Voltage (Box, Lum, R, G, B)	I_{out} = – 0.75 mA	$V_{DD(D)}$ – 0.4	V
V_{OL}	Maximum Low-Level Output Voltage (Box, Lum, R, G, B)	I_{out} = 1.0 mA	0.4	V
I_{in}	Maximum Input Leakage Current (HSync, Enable, CT/SData, Lang/SClk, Config, $\overline{Reset}$)	$V_{in} = V_{SS(D)}$ or $V_{DD(D)}$	± 3.0	µA
I_{DD}	Maximum Power Supply Current		*	mA

* The estimated value is 20 mA; this is not guaranteed.

VIDEO AC CHARACTERISTICS ($V_{DD(A)}$ = $V_{DD(D)}$ = 4.75 to 5.25 V, T_A = 0 to 70°C)

Symbol	Parameter	Guaranteed Limit	Unit
V_{in}	Input Sensitivity, Video In	1.0 V p-p ± 3 dB	
BW	Bandwidth, Video In	600	kHz
SN	Signal-to-Random-Noise Ratio (CCIR Weighted), Video In (≤ 1 Error per Row)	25	dB
	Code Level at 1 V p-p, Video In (Note 1)	50 ± 10	IRE
	Maximum Frequency Tolerance, HSync (Nominal Frequency = 15,734.263 Hz)	± 3	%
t	Clock Run-In Start (Notes 1 and 2)	10.5 ± 0.5	µs

NOTES:
1. Line 21 must be in the proper relative position to the leading edge of the vertical sync pulse.
2. Measured from the midpoint of the leading edge of HSync to the midpoint on the rising edge of the first clock run-in cycle.



NOTES:
1. Timing parameters derived from the *NAB Engineering Handbook*, 7th Edition, page 5.4-75.
2. Dot period = 82.76 ns.
3. An assumption is made that the delay through the low-pass filter is 220 ns. Therefore, the timing of the output signals is normally set so that the start of the leading box preceding the first displayable character cell occurs at 13.4 to 13.7 µs after the midpoint of the leading edge of the horizontal sync pulse at Point A. The 13.4 to 13.7 µs value may be altered via a mask option; contact your Motorola representative.

Figure 2. Timing of Output Signals Relative to Composite Video at Point A

SERIAL INTERFACE AC CHARACTERISTICS ($V_{DD(A)}$ = $V_{DD(D)}$ = 4.75 to 5.25 V, T_A = 0 to 70°C)

Symbol	Parameter	Guaranteed Limit	Unit
f_{clk}	Maximum Serial Data Clock Frequency (Also, refer to t_w) (Figure 3)	10	MHz
t_{su}	Minimum Setup Time, CT/SData to Lang/SClk (Figure 4)	75	ns
t_h	Minimum Hold Time, Lang/SClk to CT/SData (Figure 4)	25	ns
t_{su}	Minimum Setup Time, Enable to Lang/SClk (Figure 5)	175	ns
t_{su}	Minimum Setup Time, CT/SData to Enable (Figure 7)	100	ns
t_h	Minimum Hold Time, Enable to CT/SData (Figure 7)	100	ns
t_{rec}	Minimum Recovery Time, Enable to Lang/SClk (Figure 5)	100	ns
t_w	Minimum Pulse Width, Lang/SClk (Figure 3)	50	ns
C_{in}	Maximum Input Capacitance — CT/SData, Lang/SClk, Enable	10	pF

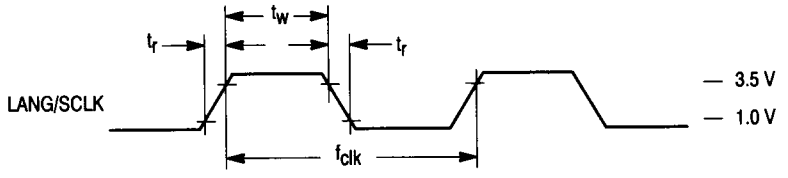


Figure 3.

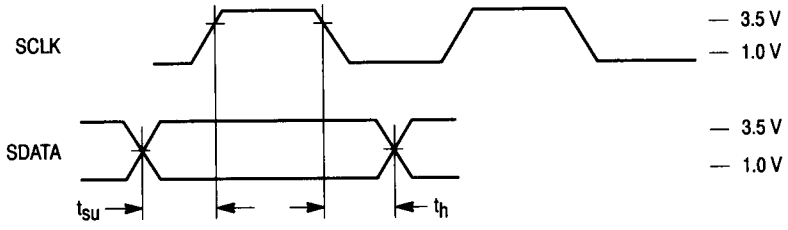


Figure 4.

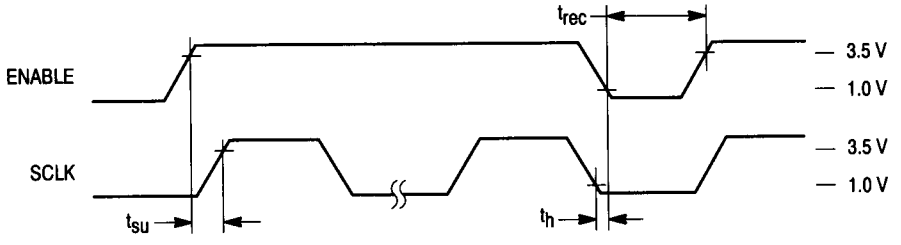


Figure 5.

THE LINE-21 CLOSED-CAPTIONING SYSTEM

The line-21 closed-captioning system provides for the transmission of caption information and other text material as an encoded composite data signal during the unblanked portion of line 21, field 1 of the standard NTSC video signal. In addition, a framing code is transmitted during the first half of line 21, field 2.

The encoded composite video signal for line 21, fields 1 and 2 is shown in Figure 6. The video signal conforms to the Standard Synchronizing Waveform for Color Transmission given in Sub-part E, Part 73 of the FCC Rules and Regulations.

Data Transmission Format

The composite data signal contained within the active portion of line 21 consists of a 7-cycle sine-wave clock run-in burst, a start bit, and 16 bits of data. These 16 bits consist of two 8-bit alphanumeric characters formulated according to the USA Standard Code for Information Interchange (USASCII;x3.4-1967) with odd parity. The clock rate is 0.5035 MHz which is 32 H. The clock burst and data packet are 50 IRE units peak-to-peak and are filtered to a "2T" response. Data is sent with the least significant bit (bit b1) being sent first and the most significant bit (bit b8, the parity bit) being sent last.

Multiplexed Data Channels

The line-21 closed-caption system defines four different data channels which can be time multiplexed within the Line 21 data stream. They are Captions — Language 1 (C1), Captions — Language 2 (C2), Text — Language 1 (T1) and Text — Language 2 (T2). Both languages may be English in either case.

Text (optional) is defined as non-video related information, so its display can fill the screen. In a full-screen text-mode display, a black box 8 rows high by 34 columns wide covers the screen. Text appears starting at the top with a maximum of 32 characters per row. When all 8 rows have been used, the display scrolls up as additional information is received. The MC144143 provides a reduced height text display mode showing 8 rows of text.

Captions are video-related information, so they are not permitted to overwrite the screen. Captions may be displayed anywhere on the screen. Up to four rows may be displayed at one time. All the rows in each caption appear at once, so this mode is called pop-on captions.

A secondary caption display, called *rollup captions*, is also provided. In this mode, caption information is displayed in any consecutive two, three, or four rows. Data appears in the base row and scrolls up as new information is received. The data scrolls off the top row selected, as in the *text* mode. Rollup captions are usually used for captioning unscripted and fast turn around programming, such as talk shows and news.

DATA FORMAT

The four data channels are transmitted in line 21 as a time multiplexed data stream. The start of a particular channel's data stream is identified by the occurrence of one of its unique command codes. Once a unique command code is received, all subsequent data is considered to belong to that data channel until a unique command code is received for another data channel.

The 7-bit ASCII table defines two types of information: printing and non-printing. Printable data are data bytes having values between x0100000 ($20) and x1111111 ($7F), where x represents the parity bit. Data bytes having values between x0000000 ($00) and x0011111 ($1F) are called non-printing characters, because they have no displayable character font in the standard ASCII table.

Displayable Character Set

The specifications define a modified ASCII table character set where eight of the alpha-numeric characters have been changed to provide some non-English characters. Also, 15 additional characters are defined by special character commands. The changes in the ASCII table characters are shown in Table 1.

Table 1. Modifications to the ASCII Characters

Hex Code	ASCII Character	Line-21 Character
2A	*	á
5C	\	é
5E	^	í
5F	_	ó
60	`	ú
7B	{	ç
7D	}	Ñ
7E	~	ñ

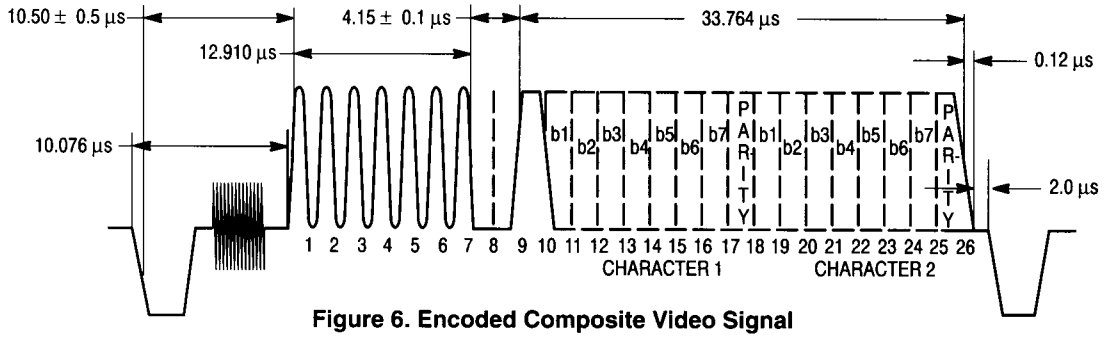


Figure 6. Encoded Composite Video Signal

Fifteen additional displayable characters are sent by transmitting a two-byte code. The sixteenth code provides a transparent space. The byte pair has a non-printing character followed by a printing character, where the non-printing character is $11 for Language 1 and $19 for Language 2. The printing character determines the special character font that is displayed according to Table 2.

Commands and Special Information

Data channel commands and special information are transmitted as two-byte pairs consisting of a non-printing character followed by a printing character. The two bytes of the pair must be transmitted in the same field, and the pair is transmitted twice in successive frames. This redundancy provides some immunity to noise errors for control information.

Throughout the line-21 system, bit 4 of the non-printing character identifies the language. Bit b4 = 0 signifies Language 1 commands and b4 = 1 signifies Language 2. The non-printing characters used in the line-21 system are $10 through $17 for Language 1 and $18 through $1F for Language 2.

Data Channel Commands

All the data channel command codes use the non-printing character $14 for Language 1 and $1C for Language 2. The printing character determines the particular command function. The commands are shown in Tables 3 through 6. The printing character is given by its hexadecimal value.

Data Location and Attribute Codes

Additional codes are used for positioning the data on the screen and for controlling the character attributes. There are two location attributes, row and column (tab or indent) position, and three character attributes, color, italics, and underline. All attribute information is contained in the preamble codes (precodes) and midrow codes (midcodes).

The precodes identify the display row and character attributes for the caption data that follows. These attributes hold for the entire line unless changed by a midcode or indent code. All the non-printing characters, $10 through $17 for Language 1 and $18 through $1F for Language 2 are used. The code pair assignment for the location and character attributes are given in Table 7.

The midcodes are used to change the character attributes in the middle of a caption row. The midcode occupies a space in the display. The characters following the midcode are displayed with the assigned attributes. The attributes hold until the end of the row, unless changed by another midcode. The indent codes listed in Table 6 actually perform in the same manner as a midcode.

The midcodes use the non-printing characters $11 and $19, respectively, for the two Languages. The printing character of the two-byte pair contains the character attributes as shown in Table 8. The printing character is given by its hexadecimal value.

Table 2. Additions to the ASCII Characters

Print	Character
30	®
31	°
32	1/2
33	¿
34	™
35	¢
36	£
37	"1/8 note" music symbol
38	à
39	"Transparent Space"
3A	è
3B	â
3C	ê
3D	î
3E	ô
3F	û

Table 3. Data Channel Commands — Captions (C1 or C2)

Print	Function
20	Resume Caption Loading (Off Screen)
25	Resume 2-Line Rollup
26	Resume 3-Line Rollup
27	Resume 4-Line Rollup
29	Resume Direct Loading (On Screen)
2C	Erase Displayed Memory
2E	Erase Non-Displayed Memory
2F	Show Caption (Flip Memories)

Table 4. Data Channel Commands — Text (T1 or T2)

Print	Function
2A	Start Text
2B	Resume Text

Table 5. Data Channel Commands — Captions or Text

Print	Function
21	Backspace
28	Flash On/Off
2D	New Line (Carriage Return)

Table 6. Data Channel Two-Byte Commands — Captions or Text

Command	Function
14 24	Delete to End of Row
17 21	Tab Offset 1 Column
17 22	Tab Offset 2 Columns
17 23	Tab Offset 3 Columns

Table 7. Code Pair Assignments for Location and Attributes

Non-print	11	11	12	12	15	15	16	16	17	17	10	13	13	14	14
CAPTION ROW	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ATTRIBUTE															
Monochrome	40	60	40	60	40	60	40	60	40	60	40	40	60	40	60
Mono Underline	41	61	41	61	41	61	41	61	41	61	41	41	61	41	61
Green	42	62	42	62	42	62	42	62	42	62	42	42	62	42	62
Green Underline	43	63	43	63	43	63	43	63	43	63	43	43	63	43	63
Blue	44	64	44	64	44	64	44	64	44	64	44	44	64	44	64
Blue Underline	45	65	45	65	45	65	45	65	45	65	45	45	65	45	65
Cyan	46	66	46	66	46	66	46	66	46	66	46	46	66	46	66
Cyan Underline	47	67	47	67	47	67	47	67	47	67	47	47	67	47	67
Red	48	68	48	68	48	68	48	68	48	68	48	48	68	48	68
Red Underline	49	69	49	69	49	69	49	69	49	69	49	49	69	49	69
Yellow	4A	6A	4A	6A	4A	6A	4A	6A	4A	6A	4A	4A	6A	4A	6A
Yellow Underline	4B	6B	4B	6B	4B	6B	4B	6B	4B	6B	4B	4B	6B	4B	6B
Magenta	4C	6C	4C	6C	4C	6C	4C	6C	4C	6C	4C	4C	6C	4C	6C
Magenta Underline	4D	6D	4D	6D	4D	6D	4D	6D	4D	6D	4D	4D	6D	4D	6D
Italics (mono)	4E	6E	4E	6E	4E	6E	4E	6E	4E	6E	4E	4E	6E	4E	6E
Italics Underline	4F	6F	4F	6F	4F	6F	4F	6F	4F	6F	4F	4F	6F	4F	6F
Indent 0 (mono)	50	70	50	70	50	70	50	70	50	70	50	50	70	50	70
Indent 0 Underline	51	71	51	71	51	71	51	71	51	71	51	51	71	51	71
Indent 4	52	72	52	72	52	72	52	72	52	72	52	52	72	52	72
Indent 4 Underline	53	73	53	73	53	73	53	73	53	73	53	53	73	53	73
Indent 8	54	74	54	74	54	74	54	74	54	74	54	54	74	54	74
Indent 8 Underline	55	75	55	75	55	75	55	75	55	75	55	55	75	55	75
Indent 12	56	76	56	76	56	76	56	76	56	76	56	56	76	56	76
Indent 12 Underline	57	77	57	77	57	77	57	77	57	77	57	57	77	57	77
Indent 16	58	78	58	78	58	78	58	78	58	78	58	58	78	58	78
Indent 16 Underline	59	79	59	79	59	79	59	79	59	79	59	59	79	59	79
Indent 20	5A	7A	5A	7A	5A	7A	5A	7A	5A	7A	5A	5A	7A	5A	7A
Indent 20 Underline	5B	7B	5B	7B	5B	7B	5B	7B	5B	7B	5B	5B	7B	5B	7B
Indent 24	5C	7C	5C	7C	5C	7C	5C	7C	5C	7C	5C	5C	7C	5C	7C
Indent 24 Underline	5D	7D	5D	7D	5D	7D	5D	7D	5D	7D	5D	5D	7D	5D	7D
Indent 28	5E	7E	5E	7E	5E	7E	5E	7E	5E	7E	5E	5E	7E	5E	7E
Indent 28 Underline	5F	7F	5F	7F	5F	7F	5F	7F	5F	7F	5F	5F	7F	5F	7F

Table 8. Midcode Assignment

Print	Character Attribute
20	Monochrome
21	Monochrome Underlined
22	Green
23	Green Underlined
24	Blue
25	Blue Underlined
26	Cyan
27	Cyan Underlined
28	Red
29	Red Underlined
2A	Yellow
2B	Yellow Underlined
2C	Magenta
2D	Magenta Underlined
2E	Italics
2F	Italics Underlined

OPERATING CHARACTERISTICS

DISPLAY FORMAT

Characters are displayed as white or colored, dot-matrix characters on a black background. The characters are described by a 6-by-9 dot pattern within a character cell which is 8 dots wide by 13 dots high. This provides a one-dot border of black around each character and provision for one row for underline, offset by a row of black, between the character and the bottom edge of the cell. Character luminance has normally been set at 90 IRE units and the surrounding black box at 10 IRE units.

The Character ROM contains a 12–18 ***dot-matrix*** pattern of each character. Each ***dot*** from the character ROM represents a single picture element or 'pixel' and each picture 'dot' is made up of a square of four pixels. Pixels 1 and 2 are generated during field one and pixels 3 and 4 during field two. Alternate rows and columns are read out of each field to produce an interleaved and rounded character. A display row contains a maximum of 32 characters plus a leading and trailing blank box, each a character cell in width, making the overall width of a display row 34 x 8 = 272 dots. Successive display rows are butted together, so that the total display is 195 dots high.

The black box (34 character cells wide by 195 dots high) results in a box size of 45.018 µs in width by 195 TV scan lines in height. A scan line is two adjacent picture lines. The first line is generated during field 1 and the second line is generated during field 2. When centered in the video display, this box starts 13.5 µs after the leading edge of H in scan line 43 and extends to scan line 237. This places the display approximately within the safe title area for NTSC receivers. Character width is 42.37 µs and is approximately centered on the screen, resulting in a leading and trailing 1.32 µs black border.

Text Mode Display

When text mode, in either language, has been selected (and valid Line 21 code has been detected in the incoming video), an 8-row by 34-character black box appears. Received text characters are displayed as they are received starting in the top row. Successive carriage returns (new line command) move the display down successive rows until 8 display rows have been used. Thereafter, the text scrolls up as new characters are added to the bottom row.

If the data for the selected channel is interrupted by a command for another channel, data processing stops but the display remains. When a *resume text* command is received, data processing resumes and the new characters are added starting at the position that the display row/column pointer was in at the interruption of data processing. If a *start text* command is received, the display is cleared and new characters are displayed starting in the top row, column 1 (left side).

When scrolling, the display shifts one scan line per frame until a complete row has been scrolled. If a carriage return is received before scrolling is complete, the display immediately completes the "scroll" by jumping up the remaining scan lines and starts displaying the new text.

There are never any transparent boxes in the text display.

Caption Mode Display

When caption mode, in either language, has been selected, the screen is transparent (display box disappears). Caption data can appear in any of the 15 display rows, but a single caption may consist of no more than 4 rows. If more than four rows are received, the last four are displayed. The form of the caption display depends on the caption mode indicated by the transmitted caption command, pop-on, paint-on, or rollup.

Pop-on captions work with two caption memories. One of them is always being displayed while the other is being used to accumulate new caption data. A new caption is popped-on by swapping the two memories (the show caption command). When the on-screen memory is erased, the screen is blank (transparent) and the memory defaults to the row/column pointer at row 1, column 1 and monochrome non-underlined.

When caption mode is selected, the decoder processes any data following the resume caption loading (RCL) command (or the show caption command). Normally, this command is followed by a precode to indicate the row, column, and character attributes to be used with the following data. If no precode is received, the data is added to the location last indicated by the row/column pointer prior to the receipt of the RCL command with the character attributes previously assigned.

Paint-on caption mode is essentially equivalent to the pop-on mode except that the data received after the resume direct loading (RDL) command is written to the on-screen memory rather than the off-screen memory. All the rules for precodes, midcodes, etc. are otherwise the same.

Rollup caption mode presents a text-like display that is limited to 2, 3, or 4 rows depending on the resume rollup (RRn) command used. The precode following the RRn command is used to indicate the base row for the rollup display. The base row is the bottom row for the rollup display. In this case, the black box does not appear until characters are being displayed and the box is only wide enough to provide a leading and trailing box in each line. The new data appears in the bottom row, and as each carriage return is received, the row scrolls up and the new data is added to the bottom. When the number of rows indicated by the resume command has been reached, the data in the top row scrolls off as new data is added to the bottom.

The tab (indent) precode permits placing captions starting at four character boundaries. The tab offset command provides the means for adjusting the starting position for a caption at any column position.

Display Erase and Autoblanking

The display is erased in the text mode by the *start text* command (but the box is maintained) and in the caption mode by the *erase displayed memory* command. The non-displayed memory can be erased by the *erase non-displayed memory* command.

Four other events can also cause the display to be erased. First, changing the data channel to be processed by switching between captions and text or between languages 1 and 2 clears the memory and hence the display. Second, if the autoblanking circuit is activated by the loss of valid code, then the display is turned off and the memory cleared. Third, the memory and display are cleared when loss of vertical lock is

detected, which normally occurs on a change of channel. Last, in the caption mode only, if no valid caption command in the selected language is received for a 16-second period, the on-screen memory is erased.

The autoblanking circuit maintains the status of the presence of valid data. The decoder is held in the decoder off (TV) state until valid data is continuously detected for a period of 0.5 second. Once the valid data decision has been made, and assuming that the user has enabled the outputs, the normal display for the data channel selected is presented.

The autoblanking circuit does not activate again until valid data has been lost for 1.5 seconds. Any valid data received during the 1.5 second period resets the counter so that autoblanking activates only on continuous loss of data for 1.5 seconds.

Decoder Control Interface

The device allows either of two control modes: parallel or serial. The parallel mode permits the control of the decoder functions by means of simple switch selections on the three control inputs. In the serial control mode, these three pins are configured to allow a serial stream. The decoder's functions are controlled by clocking in a data word via this serial port.

VIDEO INPUT SIGNAL PROCESSING

The composite video input is ac coupled to the IC where the sync tip is internally clamped to a fixed reference voltage. Initially, the signal is clamped using a simple clamp, but improved impulse noise performance is achieved once the internal sync circuits lock to the incoming signal. Noise rejection is obtained by making the clamp operative only during the sync tip. The clamped composite video signal is fed to both the data slicer and sync slicer blocks. An external capacitor stores the slice level.

The data slicer generates a clean CMOS-level data signal by slicing the signal at its midpoint. The slice level is established on an adaptive basis during line 21 of the odd field. The resultant value is stored until the next odd field line 21 begins. A high level of noise immunity is achieved by using this process.

The data clock recovery circuit produces a 32 H clock signal Data Clock (DClk) that is locked in phase to the sliced clock run-in burst obtained from the data slicer. The dot clock is locked in phase with HSync but the DClk phase is not determined until the occurrence of line 21 data. When line 21 code appears, DClk phase lock is achieved during the clock run-in burst and used to reclock the sliced data. Once phase lock is established, it is maintained until a change in video signal occurs.

TIMING AND SYNCHRONIZING CIRCUITS

All internal timing and synchronizing signals are derived from the on board 12.083 MHz VCO. Its output is the Dot Clk signal used to drive the horizontal and vertical counter chains and for display timing.

The horizontal counter is a divide-by-768 circuit with intermediate outputs needed to generate the timing logic signals used in data recovery and data output (display). It produces pulse signals at H, 2 H, 32 H and 48 H rates as well as the horizontal square wave, Q768, that is used to phase lock the VCO.

The vertical counter and control circuits produce a noise free vertical pulse by dividing the horizontal signal in a 525 counter. The internal synchronizing signals are phased up with the incoming video by comparing the internally generated vertical pulse to an input vertical pulse derived from the comp sync signal provided by the sync slicer. When proper phasing has been established, this circuit outputs the lock signal which is used to provide additional noise immunity to the slicing circuits.

The locked state is established only after several successive fields have occurred in which these two vertical pulses remain in sync. Once locked, the internal timing flywheels until such time as the two vertical pulses lose coincidence for a number of consecutive fields. Until lock is established, the decoder operates on a pulse-by-pulse basis.

The internal sync circuits lock to all 525 line signals having a vertical sync pulse that meets all of the following conditions: (1) the pulse is at least 2.5 H long, (2) the pulse starts at the proper 2 H boundary for its field, and (3) if equalizing pulse serrations are present, they must be less than 0.125 H in width.

DATA RECOVERY

The data recovery circuits perform the initial processing of the data in line 21. The sliced data is reclocked using Clk and the reclocked data stream is checked for the presence of valid data. When valid data is present, the two bytes are clocked into the serial/parallel register and output in parallel form.

This block checks the bytes for valid (odd) parity, and determines whether the recovered byte pair is a repeat of the previously received byte pair. That information is used with the redundancy flag in the command processor to determine whether the command should be executed or not.

COMMAND PROCESSOR

The command processor controls the manipulation of the data for storage and display. This processor decodes the three control inputs to determine the display status desired and the data channel selected. This information is then used to perform its most important function, the control of the loading, addressing, and clearing of the display RAM.

During data recovery time (TV lines 21–42), the command processor transfers only the data received for the data channel selected to the RAM for storage and display. In those cases such as special characters, midcodes, parity errors etc. where the data stored or action to be taken is different from the specific bytes received, the command processor converts the input data to the appropriate form.

During the display time (lines 43–237), the command processor controls the operations of the display RAM, character ROM, and output logic circuits.

MEMORY AND DISPLAY CIRCUITS

These circuits operate together to generate the output color signals R, G, B and the monochrome signals Luminance and Box. The character ROM contains the dot pattern for all the characters, but not the underline characteristic. The output logic provides the hardware underline control circuits and the italics slant generator. The smooth scroll display control is also performed in the output logic block.

DECODER CONTROL CIRCUIT

The control circuit block converts the signals provided at the three control pins into internal control signals required to

establish the operating mode of the device. The Config pin determines whether the port in is parallel or serial mode.

In parallel mode (pin 16 Config pin = high), the three control pins 1, 17, 18 perform the decoder control functions of Decoder On/Off, Caption/Text select and Lang1/Lang2 select respectively.

In serial mode (pin 16 Config pin = low), the control pins 1, 17, 18 perform the functions Enable, Serial Data, and Serial Clock. Each control word consists of 8 data bits, D0–D7, and a status bit A0. In the serial mode, two registers are accessible for software control of the decoder. These are the Control register and the Shift register. The bit definitions for these registers are given in Table 9.

Table 9. Input Data Bit Assignment for Serial Mode

Bit	Control Register	Shift Register
D0	Must Be Low	Must Be Low
D1	Output Enable	Language Select: Low = 2, High = 1
D2	Must Be Low	CT Select: Low = Text, High = Captions
D3	Must Be Low	F1/F2 Select: Low = Field 1, High = Field 2
D4	Must Be Low	Must Be Low
D5	Must Be Low	Must Be Low
D6	Reset Processor	Must Be Low
D7	Chip Reset	Must Be Low
A0	Must Be Low	Flag (serial status)

NOTE: Operation of Field 2 (even field of line 21) is the same as Field 1 (odd field of line 21)

The Control register is used to enable the outputs (Decoder On/Off) and to reset the MC144143. To write to the Control register, A0 and all serial data bits marked low must be set to 0. To reset the MC144143, clock in the data with Bits D6 and D7 set to 1. Then clock in the data with D6 and D7 set to 0. To enable the outputs, clock in data with Bit D1 set to 1, and all other bits set to 0. To disable the outputs, clock in data with all bits set to 0.

The Shift register is used to control the Data Channel and field to be processed by the decoder. To write to the Shift register, A0 must be set to 0, and all serial data bits marked low must be set to 0. The D1 and D2 bits are then used to control the Language 1 or 2 and Captions or text selection. The D3 bit controls the field selection. All other bits must be set to 0. Bit D1=1 sets the language select bit to Language 2. Bit D2=1 enables the outputs to recover Captions and D2=0 enables Text recovery. Bit D3=0 sets the field selection to Field 1, which is normal operation. Bit D3=1 sets operation to Field 2 and the MC144143 will process any valid Line-21 data that has been encoded into Field 2.

PIN DESCRIPTIONS

INPUTS

Video In (PIn 11)

Composite NTSC Video Input. This pin should be driven by an emitter follower through a 0.1 µF capacitor. The signal must be band limited to 600 kHz; a single-pole, low-pass filter may be used, as shown in Figure 8. The input level must be a nominal value of 1 V p-p. The polarity is sync tips negative.

HSync (Pin 8)

Horizontal Sync Input. This signal pulls the on-chip dot-clock VCO within the proper range. The circuit uses the frequency of HSync, not the phase. Therefore, any polarity may be used. This signal must be at CMOS voltage levels, and is usually derived from the H flyback pulse. The MC144143 requires that the HSync signal be continuous.

$\overline{\text{Reset}}$ (Pin 2)

Active-Low Master Reset. When this pin is taken to a low CMOS logic level (0), the device is reset when in the parallel mode (Config = high). Pin 2 may be tied high when in the serial mode (Config = low) if reset is to be performed through the serial port. To assure a valid reset, care should be taken to make sure reset does not occur until the V_{DD} power supply has fully ramped up. If an RC reset circuit is used, the time constant of RC should be made greater than the time for V_{DD} to ramp up.

Config (Pin 16)

Configure Input for the Control Port. When this input is at a high CMOS logic level (1), the port is configured in the parallel mode and control must be provided in parallel. When low, control must be provided as a serial stream.

Enable (Pin 1)

Parallel Mode: Decoder Display Control Input. When this pin is at a high CMOS logic level (1), the outputs are enabled. When this pin is at a low CMOS logic level (0), the R, G, B, Luminance, and Box outputs are disabled, but incoming data is still processed. The disabled output state is an inactive (low) level.

Serial Mode: Active-High Enable Input. This pin controls the serial port. When the Enable pin is low, the serial interface is disabled and the SData pin is in the high-impedance state. On the low-to-high transition of Enable, the state of the flag is output on the bidirectional SData pin. The Enable pin must remain high for the duration of the data transfer. After the data stream is sent, this pin must be returned to the low logic level. See Figure 7.

CT/SData (Pin 17)

Parallel Mode: Captions or Text Data-Channel Selector Input. When this pin is at a high CMOS logic level (1), captions are processed. A low CMOS logic level (0) causes text to be processed.

Serial Mode: Serial Data Input/Output. See Figure 7. Note that on the low-to-high transition of Enable, the bidirectional SData pin is an output. Then, on the first high-to-low transition of SClk, the SData pin becomes an input. The serial input data stream consists of eight data bits (D0 through D7) and one address bit (A0). Bit A0 determines whether the eight data bits remain in the shift register or whether the bits are transferred into a control register. If A0 is low, the contents of the input shift register are transferred to a control register when the Enable pin is brought low. If A0 is high, the bits remain in the shift register, and a flag is set. This flag indicates to the command processor that the shift register should be serviced. After servicing is performed, the command processor clears the flag. Reference Table 9.

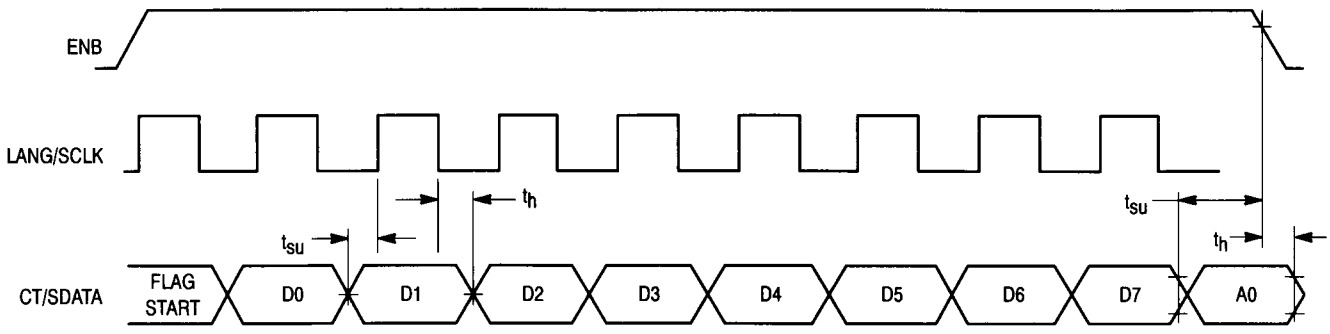


Figure 7. Timing Diagram for Serial Mode (Config = Low)

Lang/SClk (Pin 18)

Parallel Mode: Language Data-Channel Selector Input. When this pin is at a high CMOS logic level (1), language 1 is processed. A low CMOS logic level (0) causes language 2 to be processed.

Serial Mode: Serial Clock Input. Nine clock cycles are required for each serial transfer. Data is shifted in on the low-to-high transition of SClk. See Figure 7.

OUTPUTS

Box (Pin 3)

Black Box Keying Output. This digital output is at CMOS levels and is active high. The black box keying signal for the captions/text display area is used for both color and monochrome (black and white) television.

Lum (Pin 4)

Character Video Luminance Output. This digital output is at CMOS levels and is active high. This signal determines the character brightness and is used for monochrome (black and white) television, only. If unused, this pin must be floated.

R, G, B (Pins 5, 6, 7)

Red, Green, and Blue Video Outputs. These digital outputs are at CMOS logic levels and are active high. These character video signals are for color television only. If unused, these pins must be floated.

EXTERNAL COMPONENTS

Slice Level (Pin 12)

Sink Slice Level. A 0.1 µF capacitor must be tied between this pin and analog ground, $V_{SS(A)}$. The capacitor is used to store the sync slice level voltage.

Filter (Pin 13)

Loop Filter. A low-pass filter consisting of a series resistor-capacitor of 5 kΩ and 0.082 µF must be tied between this pin and analog ground $V_{SS(A)}$. This filter must be shunted with a 2200 pF capacitor. This network is used to integrate the output of the on-chip phase/frequency detector which feeds the on-chip VCO. The filter schematic is shown in Figure 8.

POWER SUPPLY

$V_{DD(A)}$ (Pin 14)

Most Positive Supply Potential for the analog section of the device. The voltage on this pin may range from + 4.75 to + 5.25 V with respect to the V_{SS} pins. For optimum performance, $V_{DD(A)}$ should be bypassed to $V_{SS(A)}$ using a low-inductance capacitor mounted very close to these pins.

$V_{DD(D)}$ (Pin 15)

Most Positive Supply Potential for the digital portion of the device. The voltage on this pin may range from + 4.75 to + 5.25 V with respect to the V_{SS} pins. For optimum performance, $V_{DD(D)}$ should be bypassed to $V_{SS(D)}$ using a low-inductance capacitor mounted very close to these pins.

$V_{SS(A)}$ (Pin 10)

Most Negative Supply Potential for the analog section of the device. This pin must be tied to ground.

$V_{SS(D)}$ (Pin 9)

Most Negative Supply Potential for the digital section of the device. This pin must be tied to ground.

APPLICATIONS INFORMATION

PCB DESIGN

To maximize the performance of the MC144143, noise should be kept to a minimum. Good printed circuit board design will enhance the operation of the MC144143. Separate analog and digital grounds will reduce noise and decoding errors. In addition, separate filters on $V_{DD(A)}$ and $V_{DD(D)}$ will also help to minimize noise and decoding errors. Sufficient decoupling and short leads will also improve performance.

When designing mixed analog/digital printed circuit boards, separate ground planes for digital ground and analog ground should be employed. Large switching currents generated by digital circuits will be amplified by analog circuitry and can quickly make a circuit unusable. Digital oscillators can become a source of EMI (electromagnetic interference) problems. Care should be taken to ensure analog ground does not inadvertently become part of the digital ground. The analog and digital grounds should be connected together at only one point. This should be the $V_{DD(A)}$ and $V_{DD(D)}$ pins on the MC144143 if possible. Additionally, when interconnecting several printed circuit boards together, care must be taken to ensure cabling does not interconnect digital and analog grounds together to produce a path for digital switching currents through analog ground.

When using any device that combines digital and analog circuitry, such as the MC144143, ground planes are desirable. Loosely interconnected traces and/or random areas of ground strewn around the printed circuit board are inadequate for high performance circuitry. While distribution of $V_{DD(A)}$ and $V_{DD(D)}$ can be done by bussing, to do so with the ground system is disastrous. Stray ground inductance can increase radiation and make EMI suppression very difficult.

A 1-inch long conductor is an 18 nH inductor. The cross sectional area of the conductor affects the exact value of the inductance, but for most PCB traces this is approximately correct. If the ground system is composed of traces or clumps of ground loosely interconnected, it will be inductive. The amount of inductance will be proportional to the length of the conductors making up the ground. This inductance cannot be decoupled away. It must be designed out.

A CMOS device exhibits a characteristic input capacitance of about 10 pF. If this gate is driven by a digital signal that switches 2.5 V in a period of 5 ns, the equation for the average current flowing during the switching time will be:

$$I_{AV} = Cdv/dt.$$

A voltage change of 2.5 V in 5 ns requires an average current of 5 mA. If we assume a linear ramp starting from zero, the total change in current will be 10 mA. The change in current per nanosecond per gate can be found by dividing the change in current by the time

$$10 \text{ mA}/5 \text{ ns} = 2 \text{ mA/ns}.$$

For a device with outputs driving one gate for each output,

$$di/dt = 16 \bullet 2 \text{ mA/ns} = 32 \text{ mA/ns}.$$

If the above 1-inch wire is in this current path, then the voltage dropped across it can be found from the formula

$$v = Ldi/dt = 18 \text{ nH} \bullet 32 \text{ mA/ns} = 0.576 \text{ V}.$$

If the inductor is in the ground system, it is in the signal path. The voltage generated by the switching currents through this inductor will be added to the signal. At best it will be superimposed on the analog signal as unwanted noise. At worst, it can render the entire circuit unusable. Even the digital signal path is not immune to this type of signal. It can false trigger clock circuits causing timing errors, confuse comparator type circuits, and cause digital signals to be misinterpreted as wrong values.

When laying out the PCB, use electrolytic capacitors of sufficient size at the power input to the printed circuit board. Adding low ESR (effective series resistance) decoupling capacitors of about 0.1 μF capacitance between $V_{DD(A)}$ and ground and $V_{DD(D)}$ and ground at the device power pins will help reduce noise in general, and also reduce EMI and ESD (electrostatic discharge) susceptibility. Implementation of a good ground plane ground system can all but eliminate the type of noise described above.

To summarize, use sufficient electrolytic capacitor filtering, make separate ground planes for analog ground and digital ground, tie these grounds together at one and only one point, keep the ground planes as continuous and unbroken as possible, use low ESR capacitors of about 0.1 μF capacitance on $V_{DD(A)}$ and $V_{DD(D)}$ at each device, and keep all leads as short as possible.

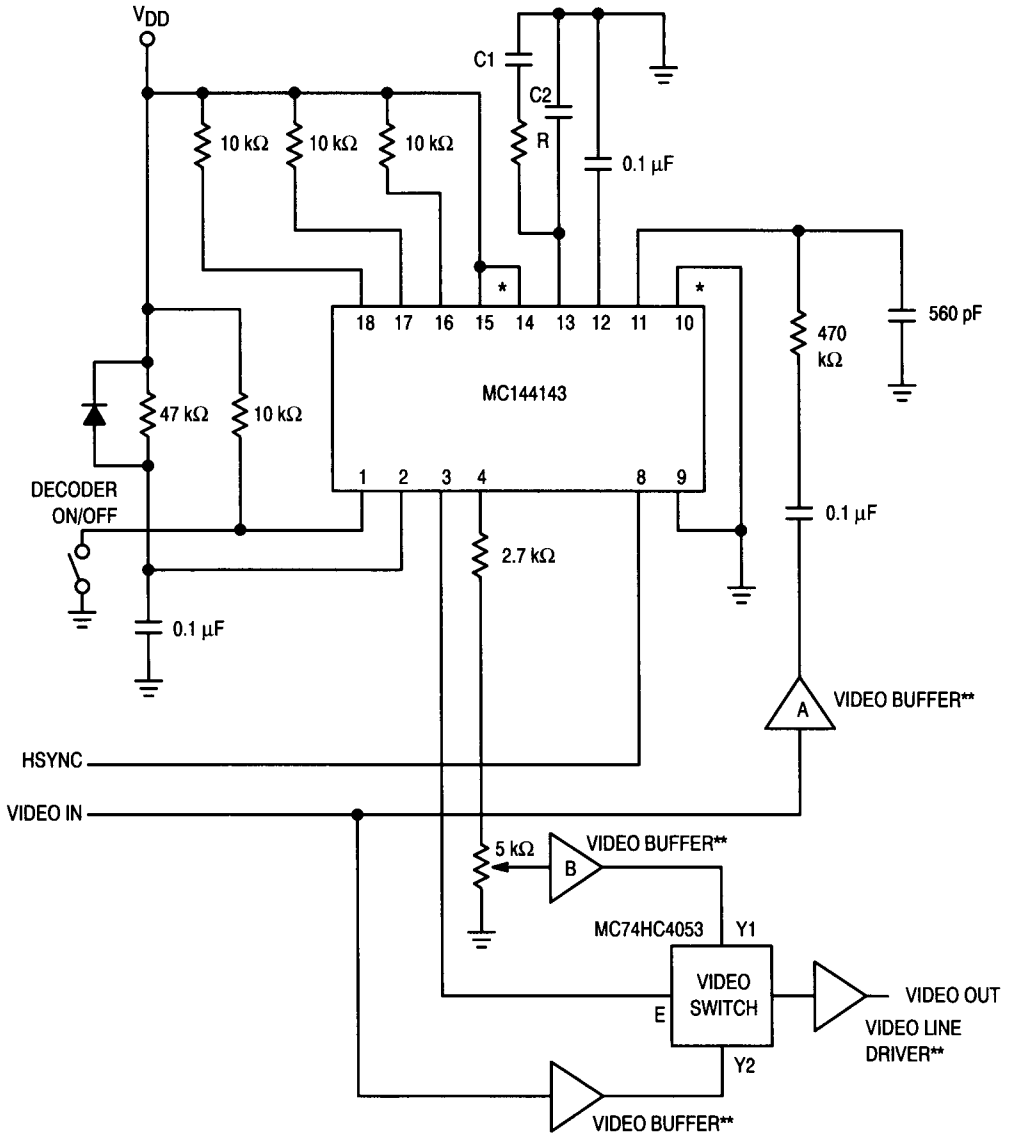
APPLICATIONS CIRCUIT

Figure 8 shows a typical decoder circuit using a parallel configuration of the input port. The video output is monochromatic using the Luminance pin as an output. Video switching control is obtained from the Box pin output. Similar techniques can be employed when using the RGB outputs.

The Video Buffers shown can be of any typical design. A gain of one is needed with sufficiently low impedance to drive the video input to the MC144143 and the video switch. The input impedance for the video switch is dependent on the design of the Video Line Driver and the input impedance for the MC144143 should be considered as 470 ohms. In either case an MC14576B or MC14577B can be used to construct the buffer, or if proper low impedance design is employed, a discrete transistor buffer amplifier can be used. When using ac coupling, dc restoration is necessary for the video buffers. This can be a simple RC network or a more complicated implementation depending on the needs of the application.

An MC14576B or MC14577B is recommended for the Video Line Driver. These devices are low impedance operational amplifiers capable of driving 150 ohms, giving them the capability of driving a doubly terminated 75 ohm transmission line.

The video switch is a fast CMOS analog switch capable of switching on a per pixel basis. An MC74HC4053 or MC74HC4066 can be used for video switching. If a single-pole, single-throw switch such as the MC74HC4066 is used, then an inverter is necessary for constructing the double-throw operation necessary for the video switch. This can be a common CMOS inverter. If a single-pole, double-throw analog switch such as the MC74HC4053 is used, an inverter is unnecessary.

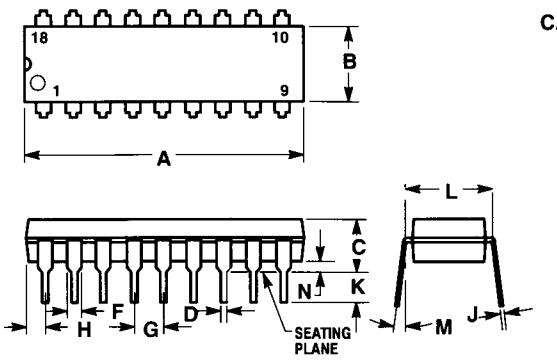


* Decouple V_{DD} to V_{SS} with 0.1 µF low ESR capacitors between pins 14 – 15 and 9 – 10 keeping leads as short as possible.
** MC14576B or MC14577B.

Figure 8. Typical Decoder Circuit

PACKAGE DIMENSIONS

P SUFFIX
PLASTIC
CASE 707-02



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTE: Introduction of this device in a surface-mount package is dependent on market demand.