DE-SERIES MOSFETS

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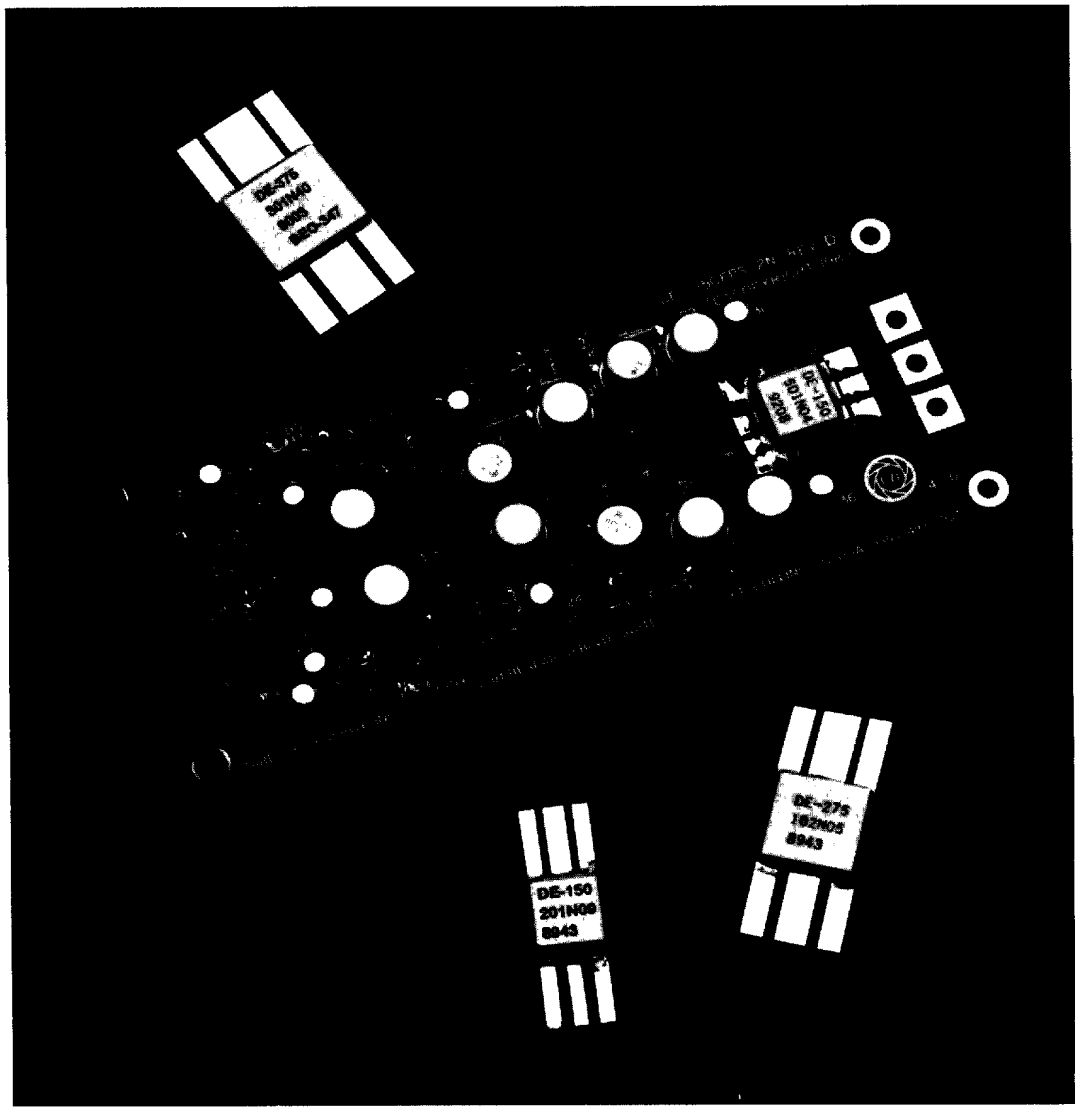
INTRODUCTION TO THE DE-SERIES

The DE-Series Fast Power™ MOSFETS are a new class of power components designed for high speed, high frequency, high power applications. DEI's Fast Power™ technology features a low inductance, low profile package which provides exceptional switching speeds and power handling capabilities.

The DE-Series offers five times the speed and twice the thermal dissipation, with one quarter the volume and one eighth the weight, of comparable conventional power MOSFET devices.

From its inception, power MOS has held great promise because of its potential speed. The particle transit time, source to drain, in any cell of the silicon die is typically on the order of 200ps (1). But conventional MOSFET packages are not suitable for high speed applications. The topology and materials of these packages are highly inductive, the thermal performance poor, and the mounting configuration at variance with low impedance circuit layout. And in the interim, die chemistry has been altered to stablize operation because of these shortcomings (2).

- **Speed and Frequency**
  Turn-on/turn-off time 4 to 8ns
  Frequency DC to > 15MHz
- **Voltage and Current**
  Vmax 100V to 1000V
  Imax (avg) 5A to 35A
  Imax (peak) < 40A to > 280A
- **Power**
  Dissipation 80W to 600W
  Switching < 100W to > 200kW
- **Other Features**
  Non-magnetic (no ferrous materials)
  Electrically isolated case



E-M SYMMETRY - Electrical Advantages of the DE-Series Fast Power™ MOSFET

DEI developed E-M Symmetry to address the need for a low inductance device for those applications which are handicapped by conventional MOSFET package design. The package design is best described as a distributed coplanar circuit (3).

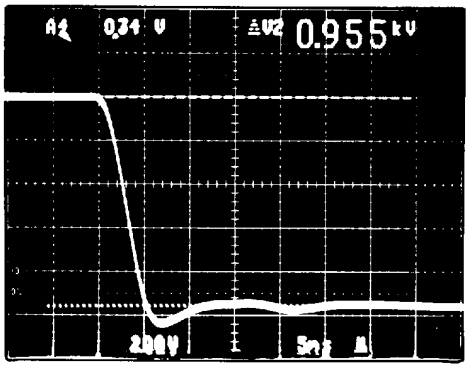


FIGURE 1. Voltage waveform

V_f = 700V (10-90%)
T_f = 3.5ns
R_L = 50 ohms

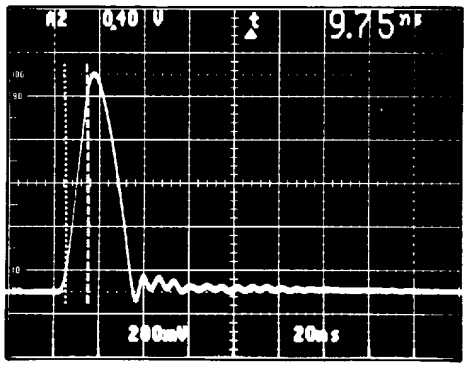


FIGURE 2. Current waveform

I_D = 100A
T_r = 9.75ns
R_L = 1 ohm

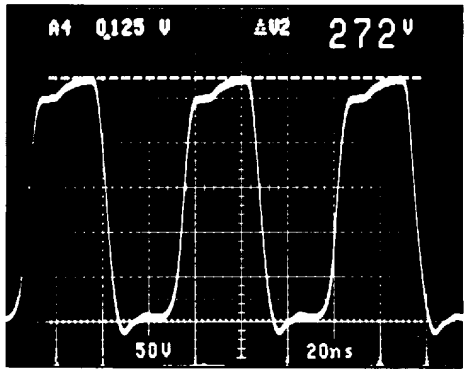


FIGURE 3. Frequency waveform

V_{DS} = 272V
f = 15MHz
P_O = 1200W

The DE-Series utilizes this coplanar structure from the external circuit, through the packaging, to the input of the power MOSFET, then continues as an identical coplanar structure, from the output of the power MOSFET die, through the package, to the contact of the external circuit. This topology provides several benefits: the distribution of the E and B fields are symmetric and uniform, the currents flow in sheets, and the voltage gradient changes are smooth and continuous. There is a mechanical benefit as well - a coplanar structure allows a practical method

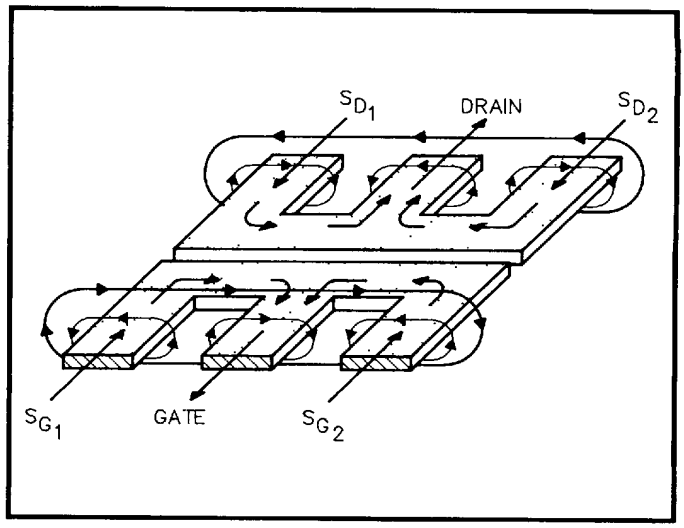


FIGURE 4. Coplanar DE-Series structure

for connecting the package leads to the external circuit that usually exist in a planar form.

Referring to **Figure 4,** the DE-Series device forms a coplanar waveguide, the ground plane of the coplanar waveguide lies on either side of the signal track (Gate or Drain) and corresponds to S_{G_1} and S_{G_2} on the gate side of the DE-Series, and likewise to S_{D_1} and S_{D_2} on the drain side.

Such that,

$I_G = I_{S_{G_1}} + I_{S_{G_2}}$ and $I_{S_{G_1}} = I_{S_{G_2}}$

and

$I_D = I_{S_{D_1}} + I_{S_{D_2}}$ and $I_{S_{D_1}} = I_{S_{D_2}}$

This symmetry provides cancellation of magnetic field vectors in all directions simultaneously, during the turn-on and turn-off transitions, effectively reducing the inductance theoretically to near zero.

To enhance switching speed further, the V_{LS} negative feedback term found in conventional three lead devices has been eliminated by integrating a differential Kelvin lead with the E-M symmetry of the input leads. Thus, the gate drive floats on the V_{LS} term, and the drain, source currents flowing in S_{D_1} and S_{D_2} are prevented by topology from flowing in S_{G_1} and S_{G_2}. Some manufacturers of conventional MOSFETs have invoked the Kelvin lead with no reduction in package inductance, which may have serious effects on device performance and reliability (4).

The combination of E-M Symmetry and the differential Kelvin allows the DE-Series to operate at voltage slew rates of $>$ 200KV/μs as shown in **Figure 1,** current slew rates of $>$ 10KA/μs as shown in **Figure 2,** and at frequencies $>$ 15MHz as shown in **Figure 3.**

Thermal-mechanical Advantages of the DE-Series Fast Power™ MOSFET

For high power applications, the DE-Series incorporates several key design features to provide excellent thermal dissipation and high power handling capability while offering a less cumbersome mounting technique than conventional devices. The first of these is illustrated in **Figure 5.**

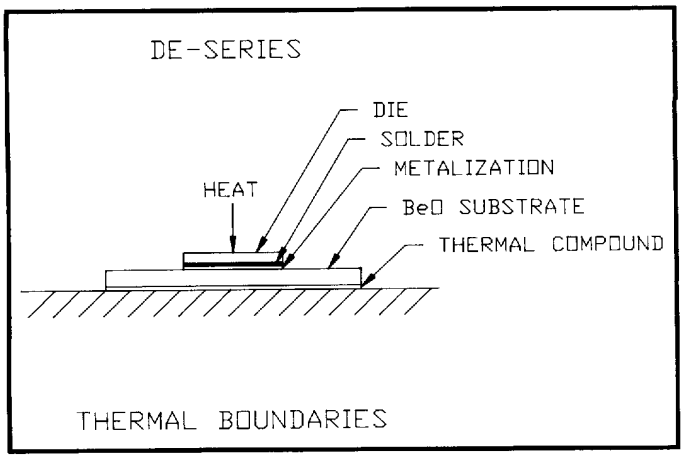


FIGURE 5. Cross-section view of DE-Series device

Here we see a cross-sectioned view of a DE-Series device and the thermal path from the die surface to the heat sink. By minimizing layer thickness, selecting materials with low thermal impedances and with coefficients of thermal expansion near silicon, a multi-layer configuration is assembled that not only provides low thermal impedance and low die stress but also allows for electrically isolated elements, i.e., gate drain and source.

Second, the package design must be capable of maintaining intimate contact between the heat extraction surface of the package and the heat sink, and also allow the device to expand in x, y, and z. **Figure 6** illustrates how this is accomplished in the DE Series.

The following descriptions refer to **Figure 6:**

(A) A silicone rubber pad provides local compliance for small variations in package and PCB.

(B) The leads are bent up and soldered to the bottom side of the PCB. This allows the device to be removed from the heat sink with the PCB. The leads of the DE-Series are made of 99.9 percent pure copper with the grain structure running in the direction of the lead length, producing an extremely soft lead. This, along with the stress relief bend, provides excellent lead compliance and offers low stress to the package seals.

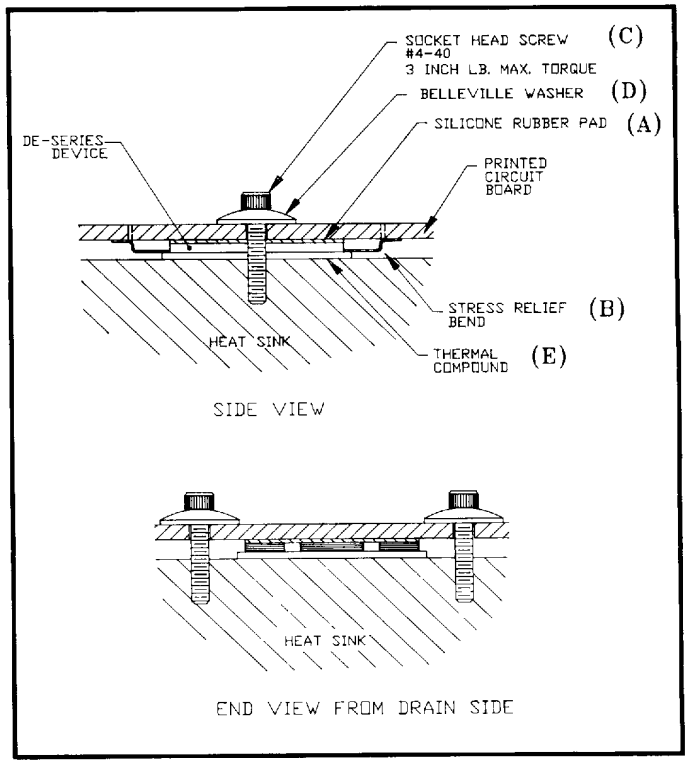


FIGURE 6. DE-Series heat sink mount

(C) Two screws pass through the PCB on either side of the device, and place it in compression.

(D) Belleville washers provide vertical compliance and maintain an even pressure on the device. This allows vertical (z) expansion.

(E) The heat sink side of the BeO substrate of the DE-Series has been ground flat to within ± .500 mil per inch/inch and thermal compound is applied for optimal thermal contact with the heat sink.

Thus the DE package design allows the device to maintain excellent thermal contact with the heat sink, yet expand in x, y and z while minimizing the mechanical stresses. This package design and mounting configuration give the DE-Series a factor of 2 in power handling capability over conventional devices while also providing for isolated elements.

REFERENCES

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George J. Krausse
DEI

■ GATE DRIVE CIRCUITRY

As either frequency or switching speed increases, circuit layout and tightly packed components become key elements of high speed circuit topology. Therefore in order to fully utilize the inherent speed of the DE-Series, the drive circuitry must be arranged with great care.

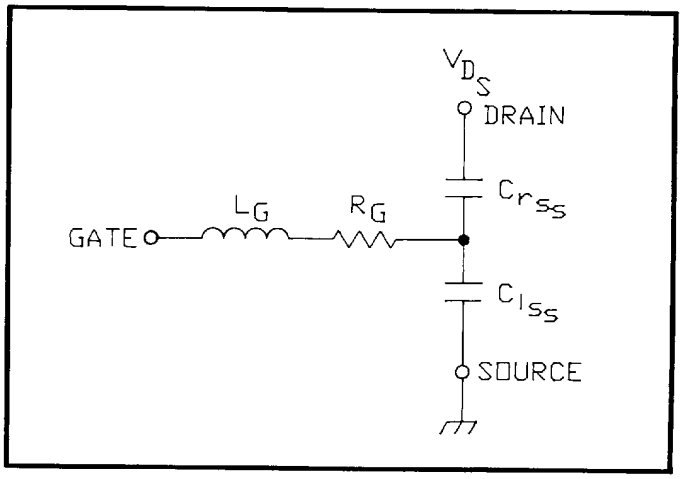


FIGURE 7. Gate input circuit model

The input of the DE-Series devices will appear very capacitive with small inductive and resistive terms as shown in **Figure 7.** This can represent a substantial load for the gate driver. To explore this, let us look at several key parameters which will help define gate drive requirements. The first parameter is peak gate current. This is given by

1.

$$I_G = C_{iss}\frac{dv_G}{dt} + C_{rss}\frac{dv_{DG}}{dt}$$

The first term is the current required by the gate capacitance. The second term accounts for the additional current required by the reverse-transfer capacitance during the drain fall time, often referred to as the Miller effect or Miller capacitance.

Given: DE-375 102N11
C_{iss} = 3900PF
C_{rss} = 85PF
Let: V_{DS} = 900V
V_{GS} = 15V
d_t = 5ns

Then:

$$I_G = \frac{3.9E\text{-}9(15)}{5E\text{-}9} + \frac{85E\text{-}12(900)}{5E\text{-}9}$$

I_G = 11.7A + 15.3A = 27A

From this two important factors are apparent. First, the total peak gate drive current can be very large. Second, for high voltage devices, the reverse-transfer capacitance current requirement can be larger than the gate capacitance current requirement.

For gate driver design it is also useful to calculate the required driver impedance. This is given by

2. $Z_{GD} = \frac{V_G}{I_G}$

If we use the values for V_G and I_G from the previous calculations for the DE-375/102N11 we have

$$Z_G = \frac{15V}{27A} = .56 \text{ ohms}$$

This implies that the driver output impedance must be very low in order to achieve the drive requirements.

Another interesting parameter is output loop inductance of the driver. This is given by

3. $L_{GD} = \frac{V_G\, d_t}{d_i}$

From the preceding:

$V_G = 15V$

$d_t = 5ns$

$d_i = 27A$

Then:

$L_{GD} = \frac{15V(5E\text{-}9)}{27} = 2.78nH$ (approximately 3nH)

This requires a very tight output current loop, careful circuit design and component selection.

Looking at the instantaneous peak power and average power requirements, the peak power is given by

4. $P_{oPK} = I_G \cdot V_G$

Given: $I_G = 27A$

$V_G = 15V$

Then: $P_{oPK} = 27A \cdot 15V = 405$ Watts

The average power is given by

5. $P_{AVE} = C_{iSS}(V_G)^2 f$

Given: $C_{iSS} = 3.9nF$

$V_G = 15V$

Let: $f = 10MHz$

Then: $P_{AVE} = 3.9E\text{-}9(15)2\ 10E6 = 8.77$ Watts

It is interesting to note that most of this 8.77 watts will be dissipated in the R_G term of the MOSFET. In fact this power loss could be large enough to damage a device if it were not attached to a heat sink.

Now parameters 1 through 5 can be combined to obtain a specification for the ideal gate driver as follows:

$V_G = 15V$

$T_r < 5ns$

$I_D > 27A$

$Z_{GD} < .56$ ohms

$L_{GD} < 3nH$

$P_{oPK} = 405$ Watts

$P_{oAve} = 9$ Watts

It is this group of specifications that DEI used as design goals for the high speed gate drive of **Figure 8.** It will drive the DE-150, 275 and 375 with pulse widths from DC to a minimum of about 50ns and frequencies up to about 1 MHz, and 3 MHz, with additional cooling for Q_1 and Q_2.

In **Figure 8,** U_1 provides TTL to 15V level conversion as well as the drive current for Q_1 and Q_2, which comprises a CMOS inverter. The drains of Q_1 and Q_2 drive the gate of the DE-Series device. For best performance the return image currents at S_{G_1} and S_{G_2} should be balanced so that

$$I_{S_{G_1}} = I_{S_{G_2}}.$$

This is done by circuit topology.

In **Figure 8** note the physical location of C9, C12, C13, C14, and C11, C15, C16, and C17. These capacitors are the by-pass capacitors for Q_1, which provides the on drive current.

Their physical location is such that the return image current for S_{G_1} is through C9, C12, C13, and C14. And the return image current for S_{G_2} is through C11, C15, C16, and C17. Thus, E-M symmetry is invoked in the input gate drive circuit. When the input drive circuit ground is decoupled from the power ground of S_{D_1} and S_{D_2}, such that no drain current flows in either S_{G_1} or S_{G_2}, then the differential Kelvin aspect of the DE-Series is operating as well as E-M symmetry, and the turn-on time is minimized.

This drive circuitry is available through Directed Energy, Inc. as the FPS1N Fast Power Switch. It is designed for applications using laser diodes, micro-channel plates, E-beam cathodes, electro-static deflectors, hard tube grids and acoustic transducers.

With an FPS1N/102N05 configured as a pull down switch for a 50 ohm load resistor, a $<5ns$ voltage fall time is obtained, as illustrated in **Figure 1.** Using the same FPS1N board, except configured as a high current switch with a DE-275/201N30, we obtained a current pulse of 100A in 9.7ns for a current slew rate of $> 10kA/\mu s$, as shown in **Figure 2.**

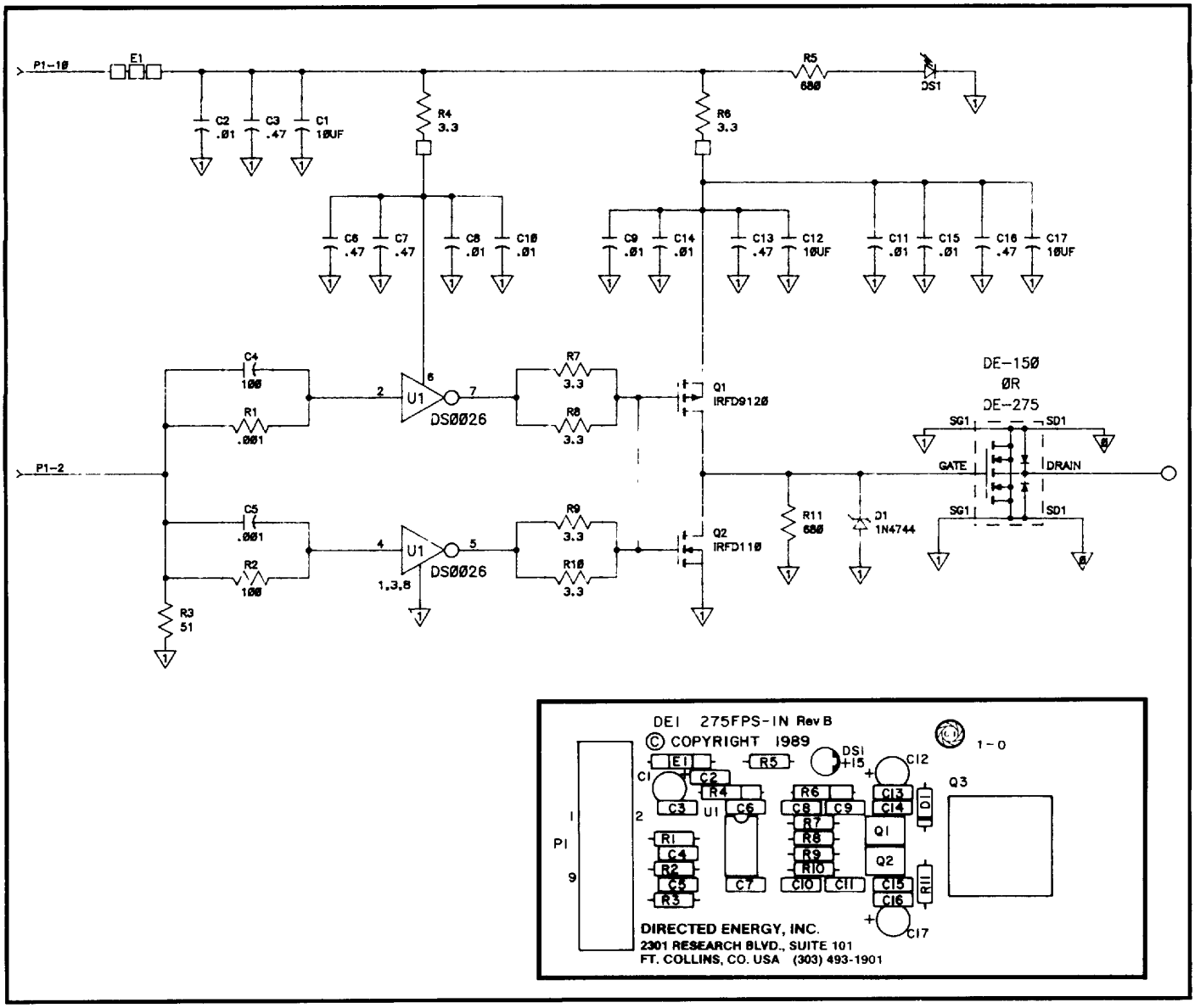


FIGURE 8. FPS-1N gate drive circuit diagram and component silk screen.

For additional general information on gate drive characteristics and requirements, see the following:

1. Gate Drive Characteristics and Requirements for Power Hexfets. Chapter 8, Hexfet. *Power Mosfet.* Designer's Manual. 9/87 International Rectifier. Application Note 937A.
2. Chapter 5. High Speed Gate Drive Circuits. *Mospower Applications Handbook.* 1984 Siliconix Inc.
3. Chapter 8. Gate Drive Circuits. *Power Mosfets Theory and Applications.* Duncan A. Grant. Wiley Interscience 1989.

A new class of power components designed for high speed, high frequency, high power applications.

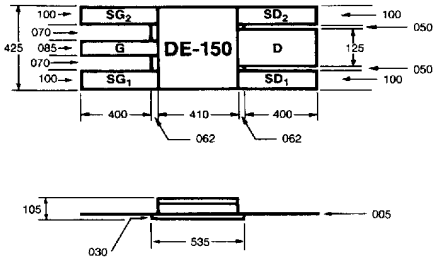
Features

- Fast rise times
- High voltages and currents
- Excellent power handling capabilities
- Multi-megahertz PRFs

Applications

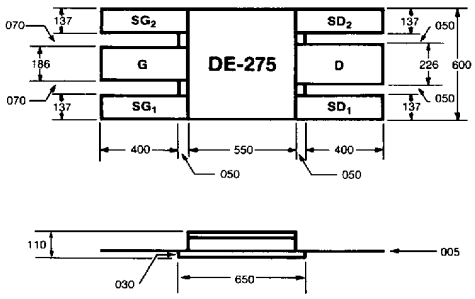
- Driving tube grids, laser diodes, MCPs, Pockels cells, Q-switches, and acoustic transducers
- HF power conversion
- Switch mode RF

THE DE-150 SERIES



PART NO.	V_{DS} (V)	I_D (A)	I_{DM} (A)	$R_{DS(ON)}$ (ohms)	T_r (ns)	P_D (W)	C_{ISS} (pF)	C_{OSS} (pF)	C_{RSS} (pF)
501N04-00	500	4.5	36	1.5	5	80	600	50	5
201N09-00	200	9.0	72	0.40	5	80	800	450	50
101N09-00	100	9.0	72	0.16	5	80	600	160	15

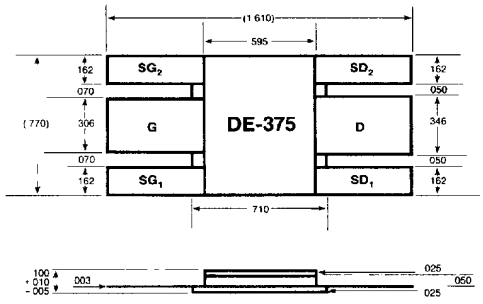
THE DE-275 SERIES



*Requires special order

PART NO.	V_{DS} (V)	I_D (A)	I_{DM} (A)	$R_{DS(ON)}$ (ohms)	T_r (ns)	P_D (W)	C_{ISS} (pF)	C_{OSS} (pF)	C_{RSS} (pF)
102N05-00	1000	5.0	40	2.60	5	150	2500	75	15
801N06-00	800	6.0	48	2.20	5	150	2500	75	15
501N12-00	500	12.0	96	0.50	5	150	2500	150	25
201N25-00	200	25.0	240	0.08	5	150	2500	250	50
201P11-00*	-200	-11.0	-80	0.50	5	150	1300	450	250
101N30-00	100	30.0	240	0.05	5	150	2500	1500	500
101P12-00*	-100	-12.0	-60	0.30	5	150	700	450	200

THE DE-375 SERIES



PART NO.	V_{DS} (V)	I_D (A)	I_{DM} (A)	$R_{DS(ON)}$ (ohms)	T_r (ns)	P_D (W)	C_{ISS} (pF)	C_{OSS} (pF)	C_{RSS} (pF)
102N11-00	1000	11.0	88	1.20	7	200	3700	100	20
501N21-00	500	21.0	168	0.25	7	200	4300	150	50
301N35-00	300	35.0	320	0.10	7	200	3900	280	85

Inquire about ***DEI's*** FPS high speed gate drive modules which are available for each series of devices.