STANDARD
MICROSYSTEMS
CORPORATION

CLK19W304

CK66 Frequency Clock Generator For LX/EX Chipsets

FEATURES

- Supports Pentium™, Pentium™ Pro, Pentium™ II, AMD and Cyrix CPUs with I^2C
- 4 CPU Clocks
- 12 SDRAM Clocks for 3 DIMMs
- 7 PCI Synchronous Clocks
- One IOAPIC Clock for Multiprocessor Support
- Optional Single or Mixed Supply: (Vdd = Vddq3 = Vddq2 = Vddq2b = 3.3V) or (Vdd = Vddq3 = 3.3V, Vddq2 = Vdq2b = 2.5V)
- < 250ps Skew Among CPU and SDRAM Clocks
- < 250ps Skew Among PCI Clocks
- Smooth Frequency Switch with Selections from 50 MHz to 83.3 MHz clocks
- I^2C 2-Wire Serial Interface and I^2C Read Back
- Spread Spectrum Function to Reduce EMI
- Programmable Registers to Enable/Stop Each Output and Select Modes (Mode as Tri-state or Normal)
- MODE Pin for Power Management
- 48 MHz for USB
- 24 MHz for Super I/O
- 48 Pin SSOP Package

GENERAL DESCRIPTION

The CLK19W304 is a Main board Clock Synthesizer which provides all clocks required for high-speed RISC or CISC microprocessors such as Intel PentiumPro, PentiumII, AMD or Cyrix. Eight different frequencies of CPU and PCI clocks are externally selectable with smooth transitions.

The CLK19W304 also provides an I^2C serial bus interface to program the registers to enable or disable each clock output and choose the 0.5% or 1.5% center type spread spectrum.

The CLK19W304 accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V power supply. High drive PCI and SDRAM CLOCK outputs typically provide greater than 1 V /ns slew rate into 30 pF loads. CPU CLOCK outputs typically provide better than 1 V /ns slew rate into 20 pF loads while maintaining 50± 5% duty cycle. The fixed frequency outputs: REF, 24MHz, and 48 MHz provide better than 0.5V /ns slew rate.

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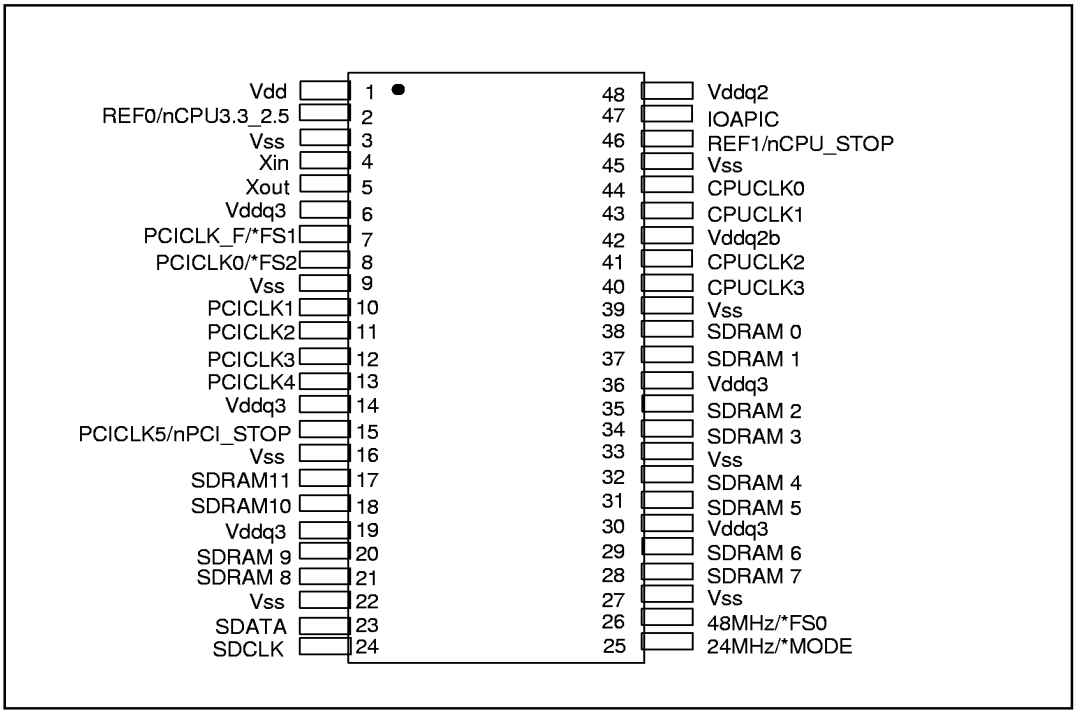
PIN CONFIGURATION



PIN DESCRIPTION

IN - Input
OUT - Output
I/O - Bi-directional Pin
n - Active Low
• - Internal 250kΩ pull-up

Crystal I/O

SYMBOL	PIN	I/O	FUNCTION
Xin	4	IN	Crystal input with internal loading capacitors and feedback resistors.
Xout	5	OUT	Crystal output at 14.318MHz nominally.

CPU, SDRAM, PCI Clock Outputs

SYMBOL	PIN	I/O	FUNCTION
CPUCLK [0:3]	40,41,43,44	OUT	Low skew (< 250ps) clock outputs for host frequencies such as CPU, Chipset and Cache. Vddq2 is the supply voltage for these outputs.
IOAPIC	47	OUT	High drive buffered output of the crystal, and is powered by VDDq2.
SDRAM [0:11]	17,18,20,21, 28,29,31,32, 34,35,37,38	O	SDRAM clock outputs which have the same frequency as CPU clocks.
PCICLK_F/ *FS1	7	I/O	Latched input for FS1 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks. Free running PCI clock during normal operation.
PCICLK 0 / *FS2	8	I/O	Latched input for FS2 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks. PCI clock during normal operation.
PCICLK [1:4]	10,11,12,13	OUT	Low skew (< 250ps) PCI clock outputs.
PCICLK5/ nPCI_STOP	15	I/O	Internal 250kΩ pull-up. If MODE = 1 (default), then this pin is a PCI5 clock output. If MODE = 0 , then this pin is nPCI_STOP and used in power management mode for synchronously stopping the all PCI clocks.

I²C Control Interface

SYMBOL	PIN	I/O	FUNCTION
SDATA	23	I/O	Serial data of I²C 2-wire control interface
SDCLK	24	IN	Serial clock of I²C 2-wire control interface

Fixed Frequency Outputs

SYMBOL	PIN	I/O	FUNCTION
REF0 / nCPU3.3_2.5	2	I/O	Internal 250kΩ pull-up. Latched input for nCPU3.3_2.5 at initial power up. Reference clock during normal operation. Latched high - Vddq2 = Vddq2b = 2.5V Latched low - Vddq2 = Vddq2b = 3.3V
REF1 / nCPU_STOP	46	I/O	Internal 250kΩ pull-up. If MODE =1 (default), then this pin is a REF1 buffered output of the crystal. If MODE = 0 , then this pin is nCPU_STOP input used in power management mode for synchronously stopping the all CPU clocks.
24MHz / *MODE	25	I/O	Internal 250kΩ pull-up. Latched input for MODE at initial power up. 24MHz output for super I/O during normal operation.
48MHz / *FS0	26	I/O	Internal 250kΩ pull-up. Latched input for FS0 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks. 48MHz output for USB during normal operation.

Power Pins

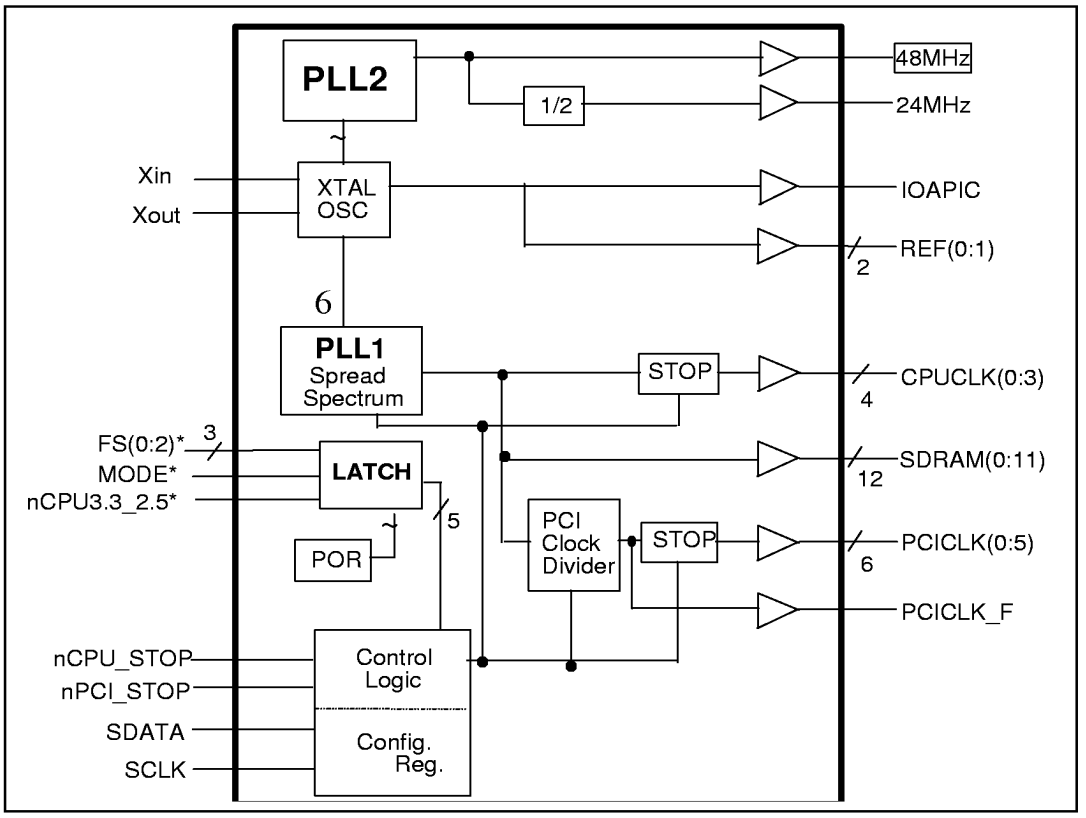
SYMBOL	PIN	FUNCTION
Vdd	1	Power supply for Ref [0:1] crystal and core logic.
Vddq2	42	Power supply for CPUCLK[0:3], either 2.5V or 3.3V.
Vddq2b	48	Power supply for IOAPIC output, either 2.5V or 3.3V.
Vddq3	6,14,19,30, 36	Power supply for SDRAM, PCICLK and 48/24MHz outputs.
Vss	3,9,16,22,27, 33,39,45	Circuit Ground.

FREQUENCY SELECTION

FS2	FS1	FS0	CPU,SDRAM (MHz)	PCI (MHz)	REF,IOAPIC (MHz)
0	0	0	50	25	14.318
0	0	1	75	32	14.318
0	1	0	83.3	41.65	14.318
0	1	1	68.5	34.25	14.318
1	0	0	83.3	33.3	14.318
1	0	1	75	37.5	14.318
1	1	0	60	30	14.318
1	1	1	66.8	33.4	14.318

nCPU 3.3_2.5 BUFFER SELECTION

nCPU 3.3_2.5 (PIN 2) INPUT LEVEL	CPU & IOAPIC OPERATE AT
1	VDD = 2.5V
0	VDD = 3.3V



CLK19W304 BLOCK DIAGRAM

FUNCTION DESCRIPTION

POWER MANAGEMENT FUNCTIONS

All clocks can be individually enabled or disabled via the 2-wire control interface. On power up, external circuitry should allow 3 ms for the VCO's to stabilize prior to enabling clock outputs to assure correct pulse widths. When MODE=0, pins 15 and 46 are inputs (nPCI_STOP), (nCPU_STOP), when MODE=1, these functions are not available. A particular clock could be enabled as both the 2-wire serial control interface and one of these pins indicate that it should be enable. The CLK19W304 may be disabled in the low state according to the following table in order to reduce power consumption. All clocks are stopped in the low state, but maintain a valid high period on transitions from running to stop. The CPU and PCI clocks transform between running and stop by waiting for one positive edge on PCICLK_F followed by negative edge on the clock of interest, after which high levels of the output are either enabled or disabled.

nCPU_STOP	nPCI_STOP	CPU	PCI	OTHER CLKs	XTAL & VCOs
0	0	LOW	LOW	RUNNING	RUNNING
0	1	LOW	RUNNING	RUNNING	RUNNING
1	0	RUNNING	LOW	RUNNING	RUNNING
1	1	RUNNING	RUNNING	RUNNING	RUNNING

2-WIRE I^2C CONTROL INTERFACE

The clock generator is a slave I2C component which can be "read back" the data stored in the latches for verification. All proceeding bytes must be sent to change one of the control bytes. The 2-wire control interface allows each clock output individually enabled or disabled. On power up, the CLK19W304 initializes with default register settings, and then it's optional to use the 2-wire control interface.

The SDATA signal only changes when the SDCLK signal is low, and is stable when SDCLK is high during normal data transfer. There are only two exceptions. One is a high-to-low transition on SDATA while SDCLK is high used to indicate the beginning of a data transfer cycle. The other is a low-to-high transition on SDATA while SDCLK is high used to indicate the end of a data transfer cycle. Data is always sent as complete 8-bit bytes followed by an acknowledge generated.

Byte writing starts with a "start" condition followed by 7-bit slave address and a write command bit [1101 0010], command code checking [0000 0000], and byte count checking. After successful reception of each byte, an "acknowledge" (low) on the SDATA wire will be generated by the clock chip. Controller can start to write to internal I^2C registers after the string of data. The sequence order is as follows:

Bytes sequence order for I^2C controller:

Clock Address A(6:0) & R/W	**Ack**	**8 bits dummy Command code**	**Ack**	**8 bits dummy Byte count**	**Ack**	**Byte0,1,2... until Stop**

Set R/W to 1 when "read back", the data sequence is as follows:

Clock Address A(6:0) & R/W	**Ack**	**Byte 0**	**Ack**	**Byte 1**	**Ack**	**Byte2, 3, 4... until Stop**

SERIAL CONTROL REGISTERS

The Pin column lists the affected pin number and the @PowerUp column gives the state at true power up. Registers are set to the values shown only on true power up. "Command Code" byte and "Byte Count" byte must be sent following the acknowledge of the Address Byte. Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledge. After that, the below described sequence (Register 0, Register 1, Register 2,) will be valid and acknowledged.

Register 0: CPU Frequency Select Register (1 = enable, 0 = Stopped)

BIT	@POWERUP	PIN	DESCRIPTION
7	0	-	0 = ±1.5% Spread Spectrum Modulation 1 = ±0.5% Spread Spectrum Modulation
6	0	-	SSEL2 (Frequency table selection by software via I^2C)
5	0	-	SSEL1 (Frequency table selection by software via I^2C)
4	0	-	SSEL0 (Frequency table selection by software via I^2C)
3	0	-	0 = Selection by hardware 1 = Selection by software I^2C - Bit 6:4
2	0	-	0 = Spread Spectrum center spread type 1 = Spread Spectrum down spread type
1	0	-	0 = Normal 1 = Spread Spectrum enabled
0	0	-	0 = Running 1 = Tristate all outputs

Frequency table selection by software via I^2C

SSEL2	SSEL1	SSEL0	CPU,SDRAM (MHz)	PCI (MHz)	REF,IOAPIC (MHz)
0	0	0	50	25	14.318
0	0	1	75	32	14.318
0	1	0	83.3	41.65	14.318
0	1	1	68.5	34.25	14.318
1	0	0	83.3	33.3	14.318
1	0	1	75	37.5	14.318
1	1	0	60	30	14.318
1	1	1	66.8	33.4	14.318

FUNCTION TABLE

FUNCTION	OUTPUTS				
Description	CPU	PCI	SDRAM	REF	IOAPIC
Tri-State	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Normal	see table	see table	CPU	14.318	14.318

Register 1 : CPU , 48/24 MHz Clock Register (1 = enable, 0 = Stopped)

BIT	@POWERUP	PIN	DESCRIPTION
7	1	-	Reserved
6	1	-	Reserved
5	1	-	Reserved
4	1	-	Reserved
3	1	40	CPUCLK3 (Active / Inactive)
2	1	41	CPUCLK2 (Active / Inactive)
1	1	43	CPUCLK1 (Active / Inactive)
0	1	44	CPUCLK0 (Active / Inactive)

Register 2: PCI Clock Register (1 = enable, 0 = Stopped)

BIT	@POWERUP	PIN	DESCRIPTION
7	X	-	Reserved
6	1	7	PCICLK_F (Active / Inactive)
5	1	15	PCICLK5 (Active / Inactive)
4	1	13	PCICLK4 (Active / Inactive)
3	1	12	PCICLK3 (Active / Inactive)
2	1	11	PCICLK2 (Active / Inactive)
1	1	10	PCICLk1 (Active / Inactive)
0	1	8	PCICLK0 (Active / Inactive)

Register 3: SDRAM Clock Register (1 = enable, 0 = Stopped)

BIT	@POWERUP	PIN	DESCRIPTION
7	1	28	SDRAM7 (Active / Inactive)
6	1	29	SDRAM6 (Active / Inactive)
5	1	31	SDRAM5 (Active / Inactive)
4	1	32	SDRAM4 (Active / Inactive)
3	1	34	SDRAM3 (Active / Inactive)
2	1	35	SDRAM2 (Active / Inactive)
1	1	37	SDRAM1 (Active / Inactive)
0	1	38	SDRAM0 (Active / Inactive)

Register 4: Additional SDRAM Clock Register (1 = enable, 0 = Stopped)

BIT	@POWERUP	PIN	DESCRIPTION
7	X	-	Reserved
6	X	-	Reserved
5	X	-	Reserved
4	X	-	Reserved
3	1	17	SDRAM11 (Active / Inactive)
2	1	18	SDRAM10 (Active / Inactive)
1	1	20	SDRAM9 (Active / Inactive)
0	1	21	SDRAM8 (Active / Inactive)

Register 5: Peripheral Control (1 = enable, 0 = Stopped)

BIT	@POWERUP	PIN	DESCRIPTION
7	X	-	Reserved
6	X	-	Reserved
5	X	-	Reserved
4	1	47	IOAPIC (Active / Inactive)
3	X	-	Reserved
2	X	-	Reserved
1	1	46	REF1 (Active / Inactive)
0	1	2	REF0 (Active / Inactive)

Register 6: Reserved Register

BIT	@POWERUP	PIN	DESCRIPTION
7	X	-	Reserved
6	X	-	Reserved
5	X	-	Reserved
4	X	-	Reserved
3	X	-	Reserved
2	X	-	Reserved
1	X	-	Reserved
0	X	-	Reserved

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or Vdd).

SYMBOL	PARAMETER	RATING
Vdd , V_{IN}	Voltage on any pin with respect to GND	- 0.5 V to + 7.0 V
T_{STG}	Storage Temperature	- 65°C to + 150°C
T_B	Ambient Temperature	- 55°C to + 125°C
T_A	Operating Temperature	0°C to + 70°C

AC CHARACTERISTICS

Vdd = Vddq3 = 3.3V – 5 %, Vddq2 = Vddq2b = 2.375V~2.9V , T_A = 0 C to +70 C						
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**TEST CONDITIONS**
Output Duty Cycle		45	50	55	%	Measured at 1.5V
CPU/SDRAM to PCI Offset	t_{OFF}	1		4	ns	15 pF Load Measured at 1.5V
Skew (CPU-CPU), (PCI-PCI), (SDRAM-SDRAM)	t_{SKEW}			250	ps	15 pF Load Measured at 1.5V
CPU/SDRAM Cycle to Cycle Jitter	t_{CCJ}			±250	ps	
CPU/SDRAM Absolute Jitter	t_{JA}			500	ps	
Jitter Spectrum 20 dB Bandwidth from Center	BWJ			500	KHz	
Output Rise (0.4V ~ 2.0V) & Fall (2.0V ~0.4V) Time	t_{TLH} t_{THL}	0.4		1.6	ns	15 pF Load on CPU and PCI outputs
Overshoot/Undershoot Beyond Power Rails	Vover	0.7		1.5	V	22 Ω at source of 8 inch PCB run to 15 pF load
Ring Back Exclusion	VRBE	0.7		2.1	V	Ring Back must not enter this range.

DC CHARACTERISTICS

Vdd = Vddq3 = 3.3V – 5 %, Vddq2 = Vddq2b = 2.375V~2.9V , T_A = 0 C to +70 C						
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**TEST CONDITIONS**
Input Low Voltage	V_{IL}			0.8	V_{dc}	
Input High Voltage	V_{IH}	2.0			V_{dc}	
Input Low Current	I_{IL}			-66	µA	
Input High Current	I_{IH}			5	µA	
Output Low Voltage I_{OL} = 4 mA	V_{OL}			0.4	V_{dc}	All outputs
Output High Voltage I_{OH} = 4mA	V_{OH}	2.4			V_{dc}	All outputs using 3.3V power
Tri-State leakage Current	Ioz			10	µA	
Dynamic Supply Current for Vdd + Vddq3	I_{dd3}				mA	CPU = 66.6 MHz PCI = 33.3 MHz with load
Dynamic Supply Current for Vddq2 + Vddq2b	I_{dd2}				mA	Same as above
CPU Stop Current for Vdd + Vddq3	I_{CPUS3}				mA	Same as above
CPU Stop Current for Vddq2 + Vddq2b	I_{CPUS2}				mA	Same as above
PCI Stop Current for Vdd + Vddq3	I_{PD3}				mA	

BUFFER CHARACTERISTICS

TYPE 1 BUFFER FOR CPU (0:3)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITIONS
Pull-Up Current Min	$I_{OH(min)}$	-27			mA	Vout = 1.0 V
Pull-Up Current Max	$I_{OH(max)}$			-27	mA	Vout = 2.0V
Pull-Down Current Min	$I_{OL(min)}$	TBD			mA	Vout = 1.2 V
Pull-Down Current Max	$I_{OL(max)}$			27	mA	Vout = 0.3 V
Rise/Fall Time Min Between 0.4 V and 2.0 V	$T_{RF(min)}$	0.4			ns	10 pF Load
Rise/Fall Time Max Between 0.4 V and 2.0 V	$T_{RF(max)}$			1.6	ns	20 pF Load

TYPE 2 BUFFER FOR IOAPIC

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITIONS
Pull-Up Current Min	$I_{OH(min)}$				mA	Vout = 1.4 V
Pull-Up Current Max	$I_{OH(max)}$			-29	mA	Vout = 2.7V
Pull-Down Current Min	$I_{OL(min)}$				mA	Vout = 1.0 V
Pull-Down Current Max	$I_{OL(max)}$			28	mA	Vout = 0.2 V
Rise/Fall Time Min Between 0.7 V and 1.7 V	$T_{RF(min)}$	0.4			ns	10 pF Load
Rise/Fall Time Max Between 0.7 V and 1.7 V	$T_{RF(max)}$			1.8	ns	20 pF Load

TYPE 3 BUFFER FOR REF1, 24MHz, 48MHz

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITIONS
Pull-Up Current Min	$I_{OH(min)}$	-29			mA	Vout = 1.0 V
Pull-Up Current Max	$I_{OH(max)}$			-23	mA	Vout = 3.135V
Pull-Down Current Min	$I_{OL(min)}$	29			mA	Vout = 1.95 V
Pull-Down Current Max	$I_{OL(max)}$				mA	Vout = 0.4 V
Rise/Fall Time Min Between 0.8 V and 2.0 V	$T_{RF(min)}$	1.0			ns	10 pF Load
Rise/Fall Time Max Between 0.8 V and 2.0 V	$T_{RF(max)}$			4.0	ns	20 pF Load

TYPE 4 BUFFER FOR REF0 and SDRAM(0:11)

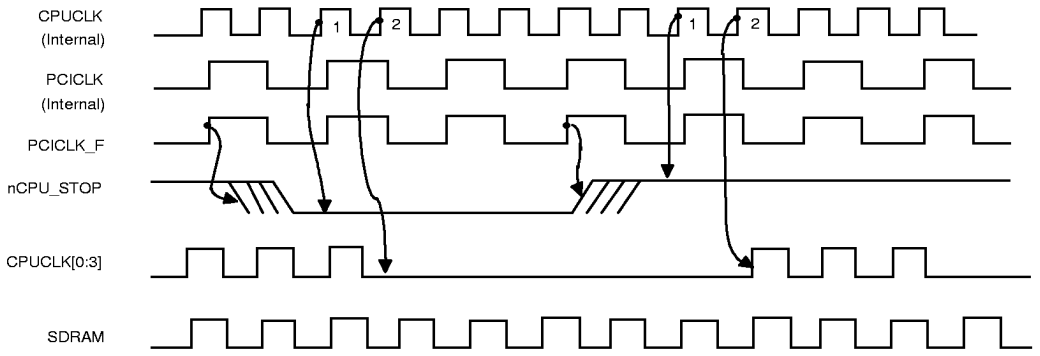
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITIONS
Pull-Up Current Min	$I_{OH(min)}$				mA	Vout = 1.65V
Pull-Up Current Max	$I_{OH(max)}$			-46	mA	Vout = 3.135V
Pull-Down Current Min	$I_{OL(min)}$				mA	Vout = 1.65 V
Pull-Down Current Max	$I_{OL(max)}$			53	mA	Vout = 0.4 V
Rise/Fall Time Min Between 0.8 V and 2.0 V	$T_{RF(min)}$	0.5			ns	20 pF Load
Rise/Fall Time Max Between 0.8 V and 2.0 V	$T_{RF(max)}$			1.3	ns	30 pF Load

TYPE 5 BUFFER FOR PCICLK(0:5,F)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITIONS
Pull-Up Current Min	$I_{OH(min)}$	-33			mA	Vout = 1.0 V
Pull-Up Current Max	$I_{OH(max)}$			-33	mA	Vout = 3.135 V
Pull-Down Current Min	$I_{OL(min)}$	30			mA	Vout = 1.95 V
Pull-Down Current Max	$I_{OL(max)}$			38	mA	Vout = 0.4 V
Rise/Fall Time Min Between 0.8 V and 2.0 V	$T_{RF(min)}$	0.5			ns	15 pF Load
Rise/Fall Time Max Between 0.8 V and 2.0 V	$T_{RF(max)}$			2.0	ns	30 pF Load

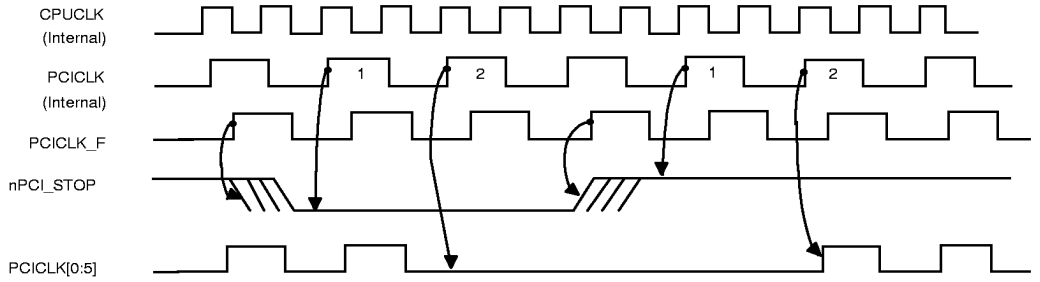
POWER MANAGEMENT TIMING

nCPU_STOP Timing Diagram (synchronous)



For synchronous Chipset, nCPU_STOP pin is a synchronous " active low " input pin used to stop the CPU clocks for low power operation. This pin is asserted synchronously by the external control logic at the rising edge of free running PCI clock(PCICLK_F). All other clocks will continue to run while the CPU clocks are stopped. The CPU clocks will always be stopped in a low state and resume output with full pulse width. In this case, CPU "clocks on latency" is less than 2 CPU clocks and "clocks off latency" is less then 2 CPU clocks.

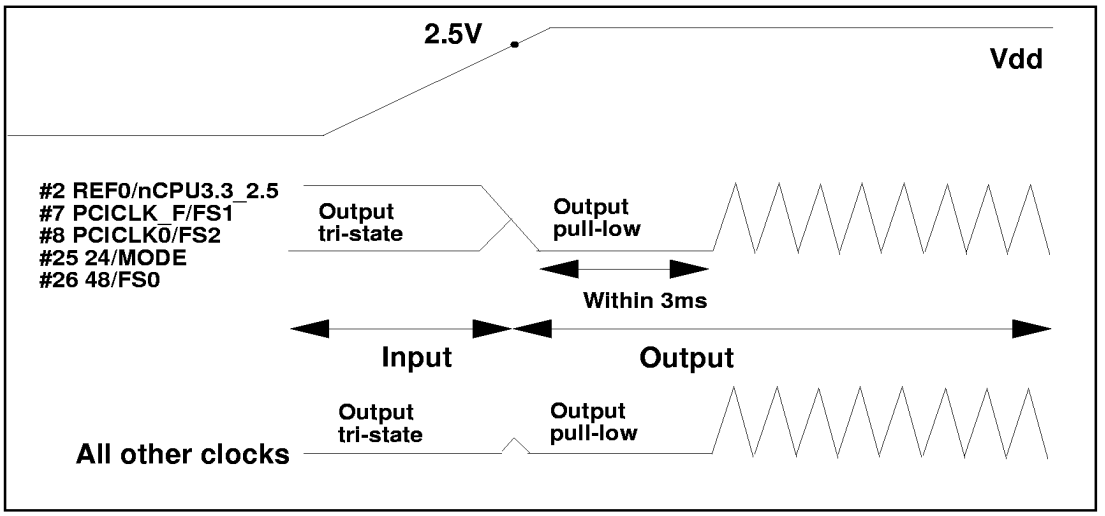
nPCI_STOP Timing Diagram (synchronous)



For synchronous Chipset, nPCI_STOP pin is a synchronous "active low" input pin used to stop the PCICLK [0:5] for low power operation. This pin is asserted synchronously by the external control logic at the rising edge of free running PCI clock(PCICLK_F). All other clocks will continue to run while the PCI clocks are stopped. The PCI clocks will always be stopped in a low state and resume output with full pulse width. In this case, PCI "clocks on latency" is less than 1 PCI clocks and "clocks off latency" is less then 1 PCI clocks.

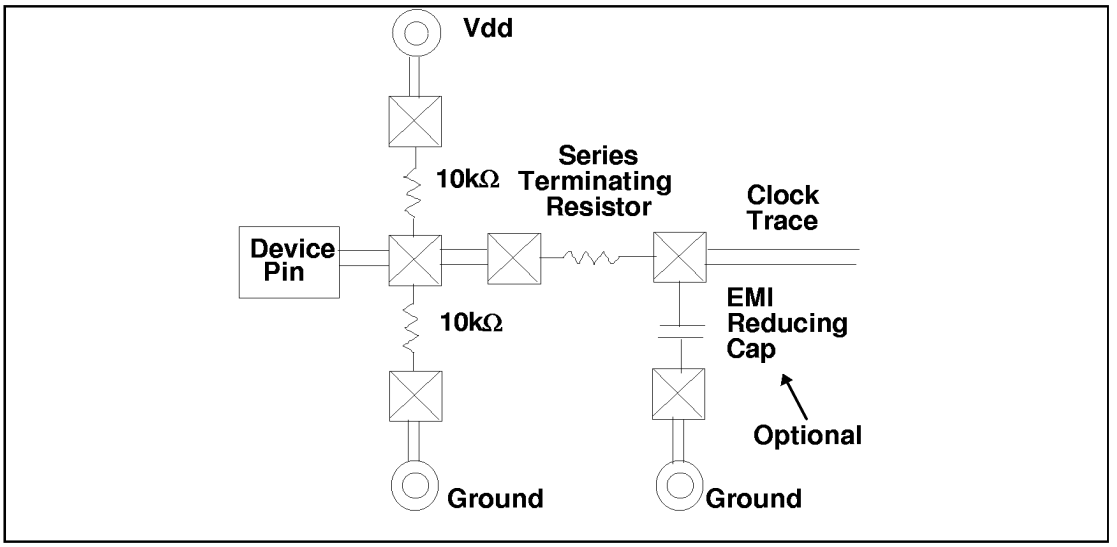
OPERATION OF DUAL FUNCTION PINS

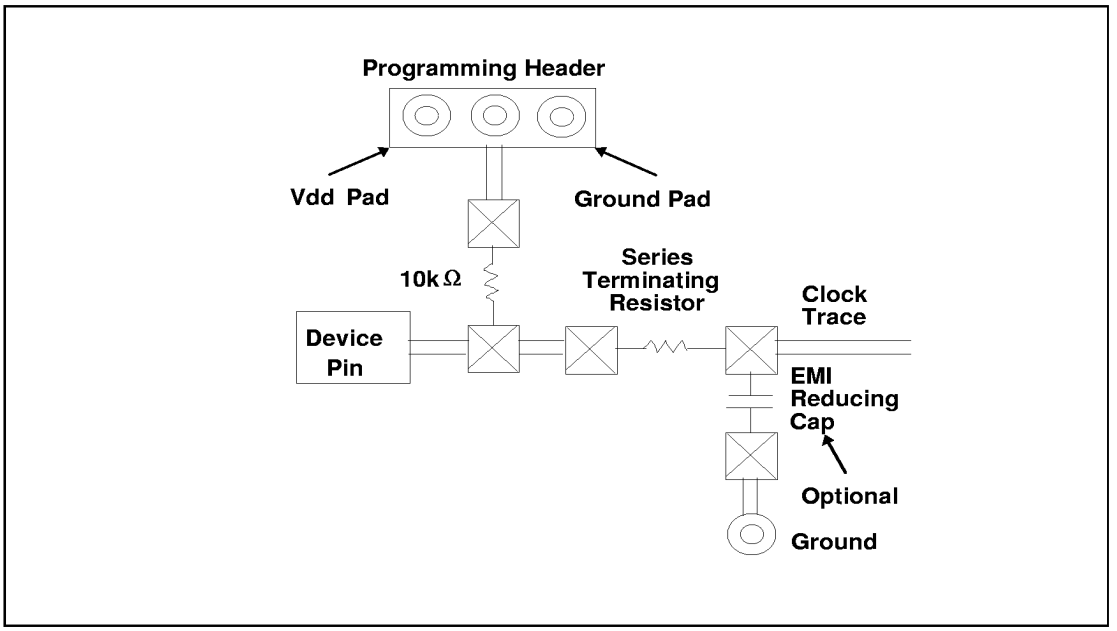
Pins 2, 7, 8, 25, and 26 are dual function pins and are used for selecting different functions in this device (see Pin description). During power up, these pins are in input mode (see Fig1), therefore, and are considered input select pins. When Vdd reaches 2.5V, the logic level that is present on these pins are latched into their appropriate internal registers. Once the correct information are properly latched, these pins will change into output pins and will be pulled low by default. At the end of the power up timer (within 3 ms) outputs starts to toggle at the specified frequency.



Each of these pins are a large pull-up resistor (250 kΩ @3.3V) inside. The default state will be logic 1, but the internal pull-up resistor may be too large when long traces or heavy load appear on these dual function pins. Under these conditions, an external 10 kΩ resistor is recommended to be connected to Vdd if logic 1 is expected. Otherwise, the direct connection to ground if a logic 0 is desired. The 10 kΩ resistor should be place before the serious terminating resistor. Note that these logic will only be latched at initial power on.

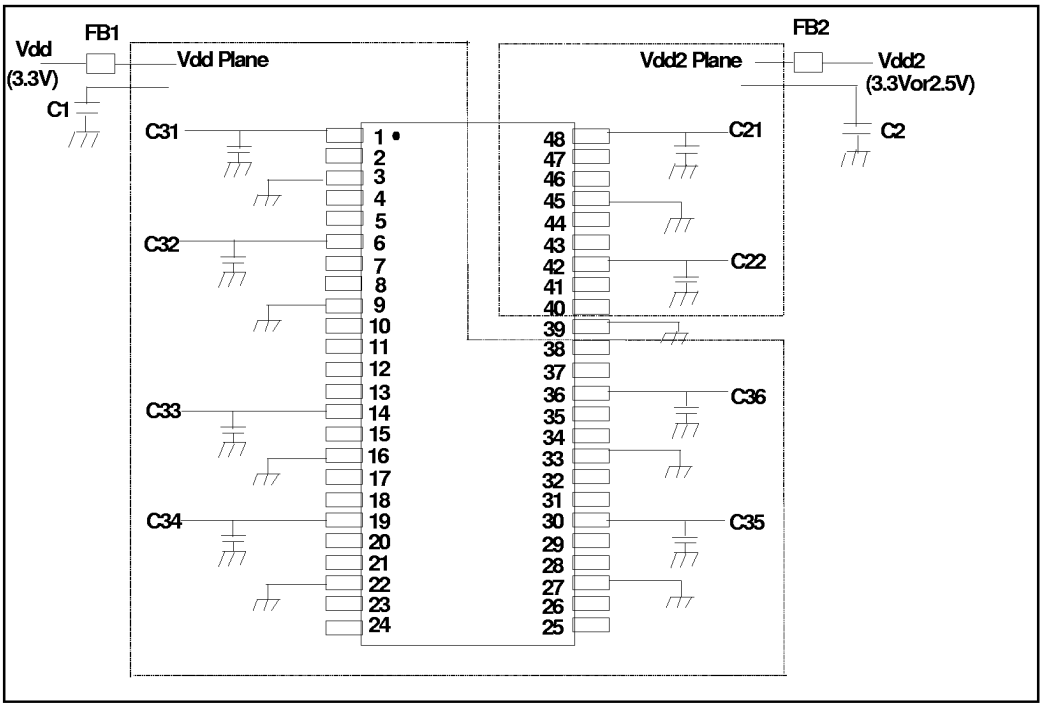
If optional EMI reducing capacitor are needed, they should be placed as close to the series terminating resistor as possible and after the series terminating resistor. These capacitor has typical values ranging from 4.7pF to 22pF.



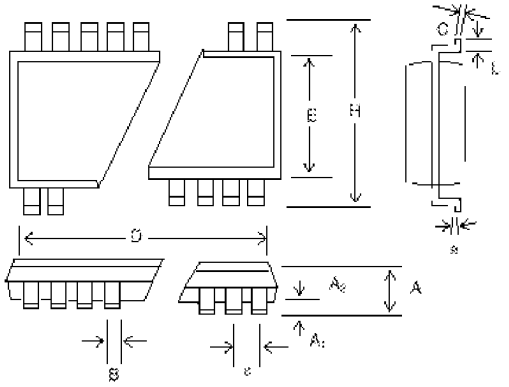


POWER SUPPLY SUGGESTION

1. A solid ground plane should be placed around the clock device. Ground connections should be tied to this main ground plane as short as possible. No cuts should be made in the ground plane around the device.
2. C21,C22,C31,C36 are decoupling capacitors (0.1£gF surface mount, low ESR, ceramic capacitors.) They should be placed as possible as the Vdd pin and the ground via.
3. C1 and C2 are supply filtering capacitors for low frequency power supply noise. A 22£gF (or 10£gF) tantalum capacitor is recommended.
4. Use of Ferrite Bead's (FB) are recommended to further reduce the power supply noise.
5. The power supply race to the Vdd pins must be thick enough so that voltage drops across the trace resistance is negligible.



PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.110	0	0	2.79
A_1	0.008	0.012	0.016	0.20	0.30	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.013	0.20	0.25	0.33
C	0.006	0.008	0.010	0.15	0.20	0.25
D	-	0.625	0.637	-	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.025 BSC			0.64 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.025	0.030	0.040	0.64	0.76	1.02
a	0°	5°	8°	0°	5°	8°

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