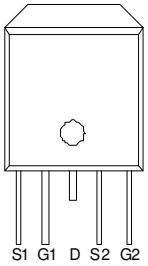
P & N-Channel 30-V (D-S) MOSFET

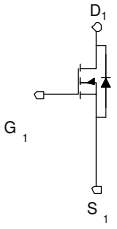
These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
30	39 @ V_{GS} = 4.5V	30
	29 @ V_{GS} = 10V	36
-30	29 @ V_{GS} = -4.5V	-36
	22 @ V_{GS} = -10V	39

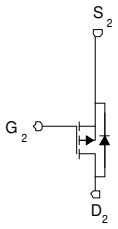
- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DPAK saves board space
- Fast switching speed
- High performance trench technology

Pb-free
RoHS COMPLIANT
HALOGEN FREE





N-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	N-Channel	P-Channel	Units
Drain-Source Voltage		V_{DS}	30	-30	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current[a]	T_A=25°C	I_D	36	-39	A
	T_A=70°C		30	-32	
Pulsed Drain Current[b]		I_{DM}	40	-40	
Continuous Source Current (Diode Conduction)[a]		I_S	30	-30	A
Power Dissipation[a]	T_A=25°C	P_D	50	50	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 175		°C

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient[a]	$R_{\theta JA}$	50	°C/W
Maximum Junction-to-Case	$R_{\theta JC}$	3.0	°C/W

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

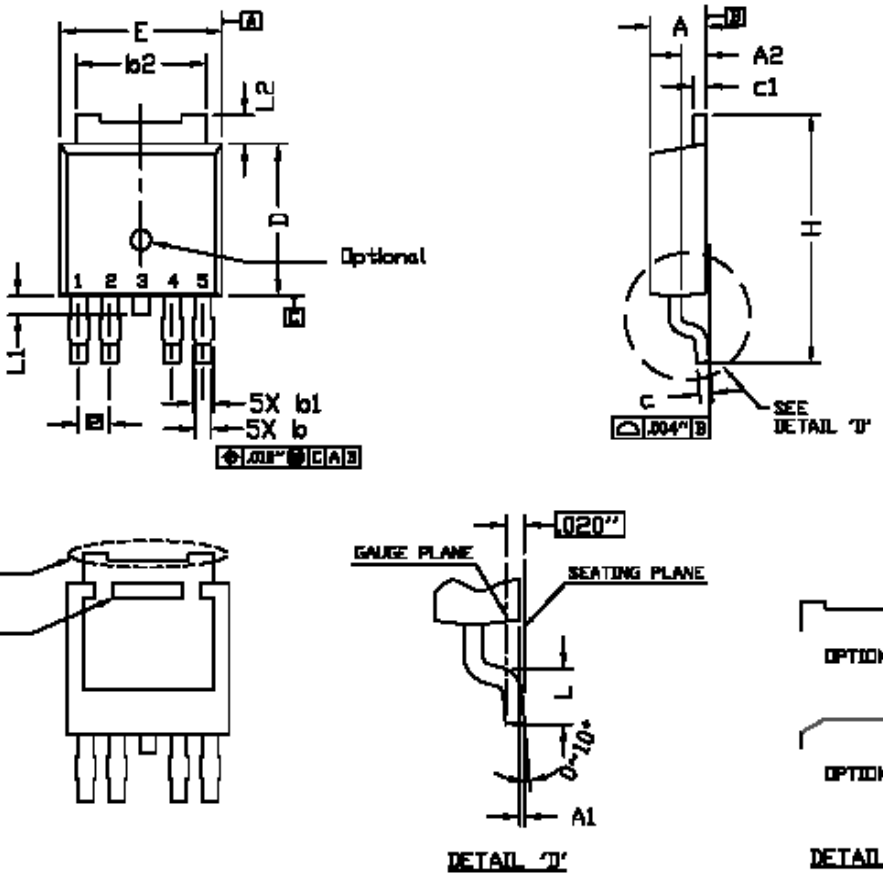
SPECIFICATIONS ($T_A = 25^oC$ UNLESS OTHERWISE NOTED)							
Parameter	**Symbol**	**Test Conditions**	**Limits**				**Unit**
			Ch	**Min**	**Typ**	**Max**	
Static							
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, $I_D = 250$ uA	N	0.6			V
		$V_{GS} = V_{DS}$, $I_D = -250$ uA	P	-0.6			
Gate-Body Leakage	I_{GSS}	$V_{GS} = -20$ V, $V_{DS} = 0$ V	P			±100	nA
		$V_{GS} = 20$ V, $V_{DS} = 0$ V	N			±100	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -24$ V, $V_{GS} = 0$ V	P			-1	uA
		$V_{DS} = 24$ V, $V_{GS} = 0$ V	N			1	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} = 5$ V, $V_{GS} = 10$ V	N	20			A
		$V_{DS} = -5$ V, $V_{GS} = -10$ V	P	-20			
Drain-Source On-Resistance[a]	$r_{DS(on)}$	VGS = 10 V, $I_D = 6.9$ A	N			29	mΩ
		VGS = 4.5 V, $I_D = 6$ A				39	
		VGS = -10 V, $I_D = -5.2$ A	P			22	
		VGS = -4.5 V, $I_D = -4.2$ A				29	
Forward Tranconductance[a]	g_{fs}	$V_{DS} = 15$ V, $I_D = 6.9$ A	N		25		S
		$V_{DS} = -15$ V, $I_D = -5.2$ A	P		10		
Dynamic							
Total Gate Charge	Q_g	N-Channel V_{DS}=15V, V_{GS}=10V, I_D=6.9A P-Channel V_{DS}=-15V, V_{GS}=-10V, I_D=-5.2A	N		6.0		nC
			P		10		
Gate-Source Charge	Q_{gs}		N		1.0		
			P		2.4		
Gate-Drain Charge	Q_{gd}		N		1.5		
			P		3.9		
Turn-On Delay Time	$t_{d(on)}$	N-Chaneel V_{DD}=15V, V_{GS}=10V, I_D=1A , R_{GEN}=6Ω, P-Channel V_{DD}=-15V, V_{GS}=-10V, I_D=-1A R_{GEN}=6Ω	N		7.4		nS
			P		7.6		
Rise Time	t_r		N		4		
			P		6.8		
Turn-Off Delay Time	$t_{d(off)}$		N		22.2		
			P		33.6		
Fall-Time	t_f		N		3.6		
			P		23.2		

Notes

a. Pulse test: PW <= 300us duty cycle <= 2%.

b. Guaranteed by design, not subject to production testing.

TO252_4L PACKAGE OUTLINE



SYMBOL	DIMENSION IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	2.184	2.286	2.388	0.086	0.090	0.094
A1	0.000	—	0.127	0.000	—	0.005
A2	0.889	—	1.143	0.035	—	0.045
b	0.508	—	0.711	0.020	—	0.028
b1	0.584	—	0.787	0.023	—	0.031
b2	4.953	—	5.461	0.195	—	0.215
c	0.457	0.508	0.610	0.018	0.020	0.024
c1	0.457	—	0.610	0.018	—	0.024
D	5.969	6.096	6.223	0.235	0.240	0.245
E	6.350	6.604	6.731	0.250	0.260	0.265
e	1.270 BSC.			0.050 BSC.		
H	9.398	—	10.414	0.370	—	0.410
L	1.270	—	2.032	0.050	—	0.080
L1	—	—	1.016	—	—	0.040
L2	0.889	—	1.270	0.035	—	0.050

NOTE
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS. MOLD FLASH SHOULD BE LESS THAN 6 MIL.
2. DIMENSION L IS MEASURED IN GAUGE PLANE.
3. TOLERANCE 0.10 mm UNLESS OTHERWISE SPECIFIED.
4. CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
5. REFER TO JEDEC TO-252 (AD).