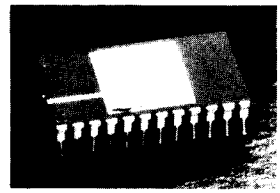
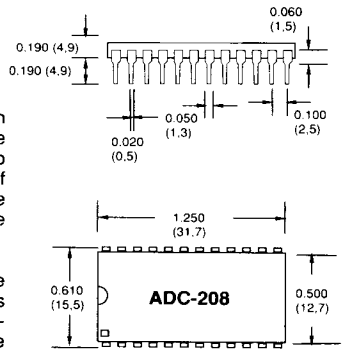
ADC-208
8-bit, 20 Msps Cmos Flash A/D

FEATURES

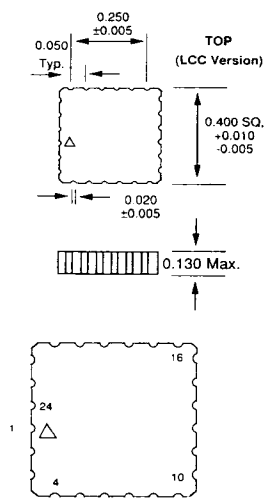
- **8-Bit flash A/D converter**
- **20 MHz sampling rate**
- **10 MHz full-power bandwidth**
- **Sample-hold not required**
- **Low power CMOS**
- **+5V dc operation**
- **1.2 Micron CMOS**
- **8-Bit latched three-state outputs with overflow bit**
- **Surface mount versions**
- **MIL-STD-883B versions**
- **No missing codes**



ADC-208 DIP



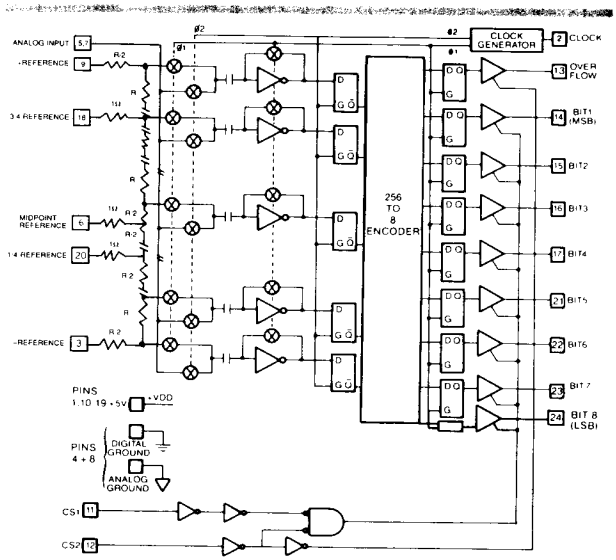
ADC-208 LCC



GENERAL DESCRIPTION

The ADC-208 utilizes an advanced VLSI 1.2 micron CMOS in providing 20 MHz sampling rates at 8-bits. The flexibility of the design architecture and process delivers effective bit rates to 30 MHz in the burst mode, one shot mode conversion times of 35 nanoseconds, low power modes to 150 mW, latch-up free operation without external components and operation over the full military temperature range.

The ADC-208 has 256 auto-zeroing comparators which are auto-balanced on every conversion to cancel out any offsets due to temperature and/or dynamic effects. These comparators sample the difference between the analog input and the reference voltages generated by the precision reference ladder network. Parallel output data and the overflow pin have Three-State outputs. The overflow pin allows cascading two devices for 9-bit operation.



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	VDD
2	CLOCK
3	-REFERENCE
4	ANA/DIG GND (VSS)
5	ANALOG INPUT
6	REFERENCE MID-POINT
7	ANALOG INPUT
8	ANA/DIG GND (VSS)
9	+REFERENCE
10	VDD
11	$\overline{CS1}$ (OUTPUT ENABLE)
12	CS2 (OVERFLOW ENABLE)
13	OVERFLOW BIT
14	BIT 1 (MSB)
15	BIT 2
16	BIT 3
17	BIT 4
18	REF 3/4 FS
19	VDD
20	REF 1/4 FS
21	BIT 5
22	BIT 6
23	BIT 7
24	BIT 8 (LSB)

ABSOLUTE MAXIMUM RATINGS

DESCRIPTION	LIMITS	UNITS
Power Supply Voltage (V_{DD} Pin 1,10,19)	-0.5 to +7.0	V dc
Digital Inputs	-0.5 to +5.5	V dc
Analog Input	-0.5 to +V_{DD} +0.5	V dc
Reference Inputs	-0.5 to +V_{DD} +0.5	V dc
Digital Outputs (short circuit protected to ground)	-0.5 to +5.5	V dc
Lead Temperature(10 sec)	+300 max.	°C
Storage Temperature	-65 to +150	°C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range +5V, ±0.25V power supplies, 15 MHz clock, +Reference = +5V, –Reference = Ground, unless otherwise noted.

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Single-Ended,Non-Isolated Input Range				
dc-20 MHz	0	–	+5.0	V
Analog Input Capacitance				
(static - Pin 5 to Pin 7)①	–	10	–	pF
(dynamic- Pin 5 to Pin 7)	–	64	–	pF
Ref. Ladder Resistance	–	300	–	Ohms
Ref. input (Note 1)	-0.5	–	V_{DD} +0.5	V dc
DIGITAL INPUTS				
Logic Levels				
Logic 1	3.2	–	–	V dc
Logic 0	–	–	0.8	V dc
Logic Loading				
Logic 1	–	+1	+5	µA
Logic 0	–	+1	+5	µA
Clock Low Pulse Width	15	25	–	nSec.
DIGITAL OUTPUTS				
Logic Levels				
Logic 1	–	4.5	5.0	V dc
Logic 0	–	–	0.4	V dc
Logic Loading				
Logic 1	4	–	–	mA
Logic 0	4	–	–	mA
Output Data Valid Delay from Rising Clock Edge				
99% probability	5	10	15	nSec.
100% probability				
+25 °C	5	10	25	nSec.
-55 °C to +125 °C	–	–	40	nSec
Coding	Straight Binary			
Resolution	8 Bits			
PERFORMANCE				
Sampling Rate.②	15	20	–	MSPS
Full Power Bandwidth	10	–	–	MHz
Diff. Linearity at +25 °C (See Tech, Note 4)				
Code Transitions	–	±0.5	±1.0	LSB
Center of Codes	–	±0.25	–	LSB
Diff. Lin. Over Temp.				
Code Transitions	–	±0.5	±1.0	LSB
Center of Codes	–	±0.25	–	LSB

PERFORMANCE	MIN.	TYP.	MAX.	UNITS
Int. Lin. at +25 °C (See Tech. Note 4) (Ref. adjusted)				
End-point	–	–	±1/2	LSB
Best-fit Line	–	–	±1/2	LSB
Int. Lin. Over Temp. (Ref. adjusted)				
Best-fit Line	–	±1/2	±1	LSB
Int. Lin. at +25 °C (Ref. unadjusted)				
End-point	–	±2	±2.5	LSB
Best-fit Line	–	±1.6	±1.9	LSB
Int. Lin. Over Temp. (Ref. unadjusted)				
End-point	–	±2.3	±2.6	LSB
Best-fit Line	–	±1.8	±2.0	LSB
Zero-Scale Offset (Code "0" to "1" transition)	–	±2.5	±4	LSB
Gain Error, +25 °C	–	±1	±1.75	LSB
Over temp.	–	±1.5	±2.5	LSB
Differential Gain③	–	2	–	%
Differential Phase③	–	1.1	–	degree
Aperture Delay	–	8	–	nSec.
Aperture Jitter	–	50	–	pSec.
Harmonic Distortion (8 MHz 2nd Order Harm.)	-40	-46	–	dB
Ref. Bandwidth (See Tech. Note 1)	–	10	–	MHz
Power Supply Rej.	–	0.02	0.05	%FSR/%/Vs
No Missing Codes	Over the operating temperature range			
POWER REQUIREMENTS				
Pwr. Supply Range (+V_{DD})	+3.5	+5.0	+5.5	V dc
Pwr. Supply Current				
+25 °C	–	+120	+145	mA
+125 °C	–	+100	+125	mA
-55 °C	–	+135	+160	mA
Pwr. Dissipation				
+25 °C	–	660	725	mW
+125 °C	–	550	690	mW
-55 °C	–	745	880	mW
PHYSICAL-ENVIRONMENTAL				
Oper. Temp. Range				
MC/LC Grade	0	–	+70	°C
MM/LM/883B	-55	–	+125	°C
Storage Temp. Range	-65	–	+150	°C
Package Types				
(DIP)	24-pin hermetic sealed, ceramic DIP			
(LCC)	24-pin hermetic sealed, ceramic LCC			

① Maximum input impedance is a function of clock frequency.
② At full power input and chip selects enabled.
③ For 10-step, 40 IRE NTSC ramp test.

TECHNICAL NOTES

1. The Reference ladder is floating with respect to V_{DD} and may be referenced anywhere within the specified limits. AC modulation of the reference voltage may also be utilized; contact DATEL for further information.

2. Clock Pulse Width - To improve performance when input signals may exceed Nyquist bandwidths, the clock duty cycle can be adjusted so that the low portion (sample mode) of the clock pulse is 15 nanoseconds wide. Reducing the sampling

Table 1. ADC-208 Output Coding

ANALOG INPUT	CODE	OVER FLOW	DATA 1234	BITS 5678	DECIMAL	HEX
0.00 V	Zero	0	0000	0000	0	00
+0.02 V	+1 LSB	0	0000	0001	1	01
+1.28 V	+1/4 FS	0	0100	0000	64	40
+2.54 V	+1/2 FS-1 LSB	0	0111	1111	127	7F
+2.56 V	+1/2 FS	0	1000	0000	128	80
+2.58 V	+1/2 FS+1 LSB	0	1000	0001	129	81
+3.84 V	+3/4 FS	0	1100	0000	192	C0
+5.10 V	+FS	0	1111	1111	255	FF
+5.12 V	Overflow	1	1111	1111	511*	1FF

* Note the overflow code does not clear the data bits.
Values shown here are for a +5.12Vdc reference. Scale other references proportionally
(+REF = +5.12V, -REF = GND, 1/4,1/2, and 3/4 Reference FS = No Connection)

time period minimizes the amount the input voltage slews and prevents the comparators from saturating.

3. The parallel output data and Overflow pin become available at the three-state buffer output when enabled. A full-scale input produces all "1"s on the data outputs. The OVERFLOW pin goes "high" when the analog input level exceeds + REF minus 1/2 LSB. Table 2 shows the truth table for the chip select enable signals.

4. DATEL uses the conservative definitions when specifying Integral Linearity (end-point) and Differential Linearity (code transition). The specifications using the less conservative definition have also been provided as a comparative specification for products specified this way.

5. The process that is used to fabricate the ADC-208 eliminates the latchup phenomena that has plagued CMOS devices in the past. The ADC-208 does not require external protection diodes.

CALIBRATION PROCEDURE

1. Connect the converter appropriately; a typical connection circuit is shown in Figure 2. Then apply an appropriate clock input. The ADC-208's reference input should be held to ±0.1% accuracy or better. Do not use the +5V power supply as a reference without precision regulation and high frequency decoupling capacitors.

2. Zero Adjustment
Apply a precision voltage reference source between the analog input (pins 5 & 7) and ground. Adjust the output of the reference source per Table 1 for the Unipolar Zero adjustment (+ 1/2 LSB). Adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 and 0000 0001. Ground -REFERENCE (pin 3) for operation without adjustment.

3. Full Scale Adjustment
Set the output of the voltage reference used in step 2 to the value shown in Table 1 for the Unipolar Gain Adjustment (+FS -1 1/2 LSB). Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1110 and 1111 1111. The + REFERENCE (pin 9) should be tied directly to a +5V reference for operation without adjustment.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 1.

5. Integral Nonlinearity Adjustments
Provision is made for optional adjustment of Integral Nonlinearity through access of the reference's 1/4, 1/2 & 3/4 Full Scale points. For example, at the half-scale major carry, set the input to 2.55V and adjust the reference until the code flickers equally between 127 and 128 for a 5.12V Full Scale input.

Table 2. Chip Select Truth Table

CS1	CS2	Bits 1-8	Overflow Bit
0	0	Tri-State Mode	Tri-State Mode
1	0	Tri-State Mode	Tri-State Mode
0	1	DATA Outputted	DATA Outputted
1	1	Tri-State Mode	DATA Outputted

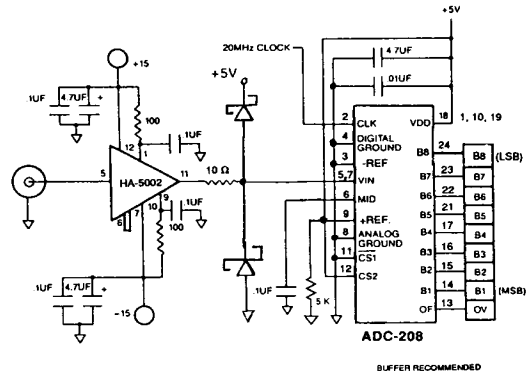
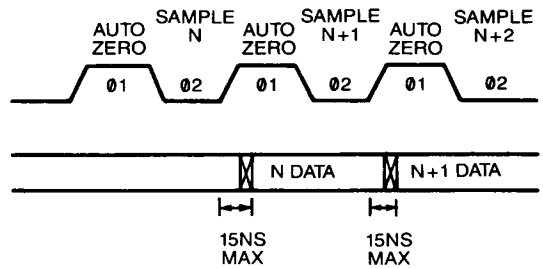


Figure 2. ADC-208 Typical Connections

NOTES:
Tie all V_{DD} pins (1,10, & 19) together. Tie both Analog Input pins (5 & 7) together. Connect both ANA/DIG GNDs (VSS pins 4 & 8) to one point, the ground plane beneath the converter.



Timing Diagram

LOW POWER MODES

Power Supply Aspect of Power Dissipation

Reduction of the V_{DD} power supply of the ADC-208 results in lower power dissipation. Refer to the curve of Figure 3 for power dissipation as a function of V_{DD}. The limiting factor is V_{DD} must be greater than the TTL or CMOS output levels. Interfacing to standard logic families presents little problem as the output drivers go to V_{DD} for a high state and to VSS for a low state.

BURST MODE

Applications can utilize an inherent system clock up to 30 MHz in the burst mode. The system clock can generate a one shot for a single conversion without requiring generation of a separate clock at a lower frequency.

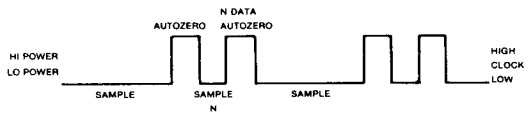


Figure 4. Burst Mode for Low Power

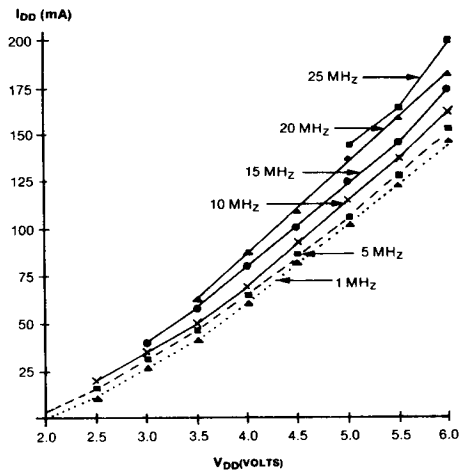


Figure 3. Power Dissipation Versus V_{DD}

Figure 5 shows power dissipation as a function of burst rate and repitition rate. Applications not requiring continuous conversions can give a double clock pulse, the clock returning low between conversions to reduce power dissipation. Power dissipation is essentially eliminated when the clock and signal input are turned off.

Figure 6 shows power dissipation as a function of the clock duty cycle. A conversion time of 35 nanoseconds can be obtained for a single conversion by leaving the clock in the Auto-zero mode. To initiate a conversion, the clock is put in the sample mode for 25 nanoseconds and then brought back high to the Auto-zero mode. Data is valid 15 nanoseconds after the clock goes high, eliminating the pipeline delay.

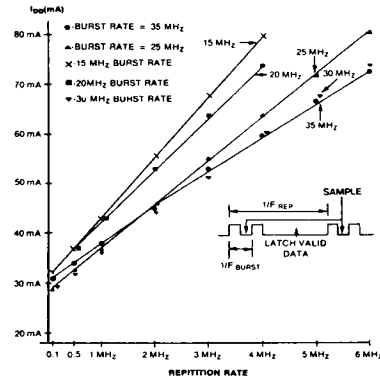


Figure 5. Power Dissipation vs. Burst Rate vs. Repetition Rate

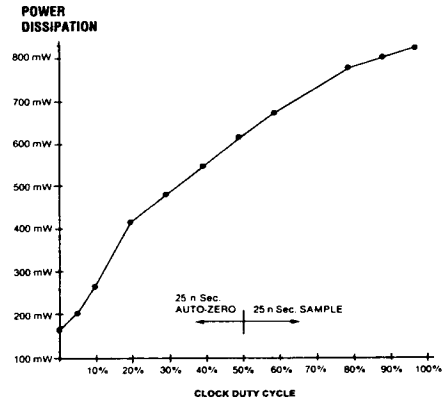


Figure 6. Power Dissipation vs. Duty Cycle for One-Shot Mode

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	PACKAGE
ADC-208MC	0 °C to +70 °C	24-pin DIP
ADC-208MM	-55 °C to +125 °C	24-pin DIP
ADC-208/883B	-55 °C to +125 °C	24-pin DIP
ADC-208LC	0 °C to +70 °C	24-pin LCC
ADC-208LM	-55 °C to +125 °C	24-pin LCC
ADC-208L/883B	-55 °C to +125 °C	24-pin LCC
ACCESSORIES		
ADC-B207/208	Evaluation Board (without ADC-208)	