MOSTEK

4096 X 1 BIT DYNAMIC RAM

MK4096 (P/N)-6/16/11

FEATURES

- ☐ Industry standard 16-pin DIP configuration (available in plastic (N) and ceramic (P) packages)
- ☐ All inputs are low capacitance and TTL compatible
- ☐ Input latches for address, chip select and data in
- ☐ Inputs protected against static charge
- ☐ Three-state TTL compatible output, latched and valid into next cycle
- ☐ Proven reliability with high performance

Part Number	Access Time	Cycle Time	Max Power*
MK 4096–6	250 ns	375 ns	450mW
MK 4096–16	300 ns	425 ns	385mW
MK 4096–11	350 ns	500 ns	320mW

*Standby power for all parts < 19mW

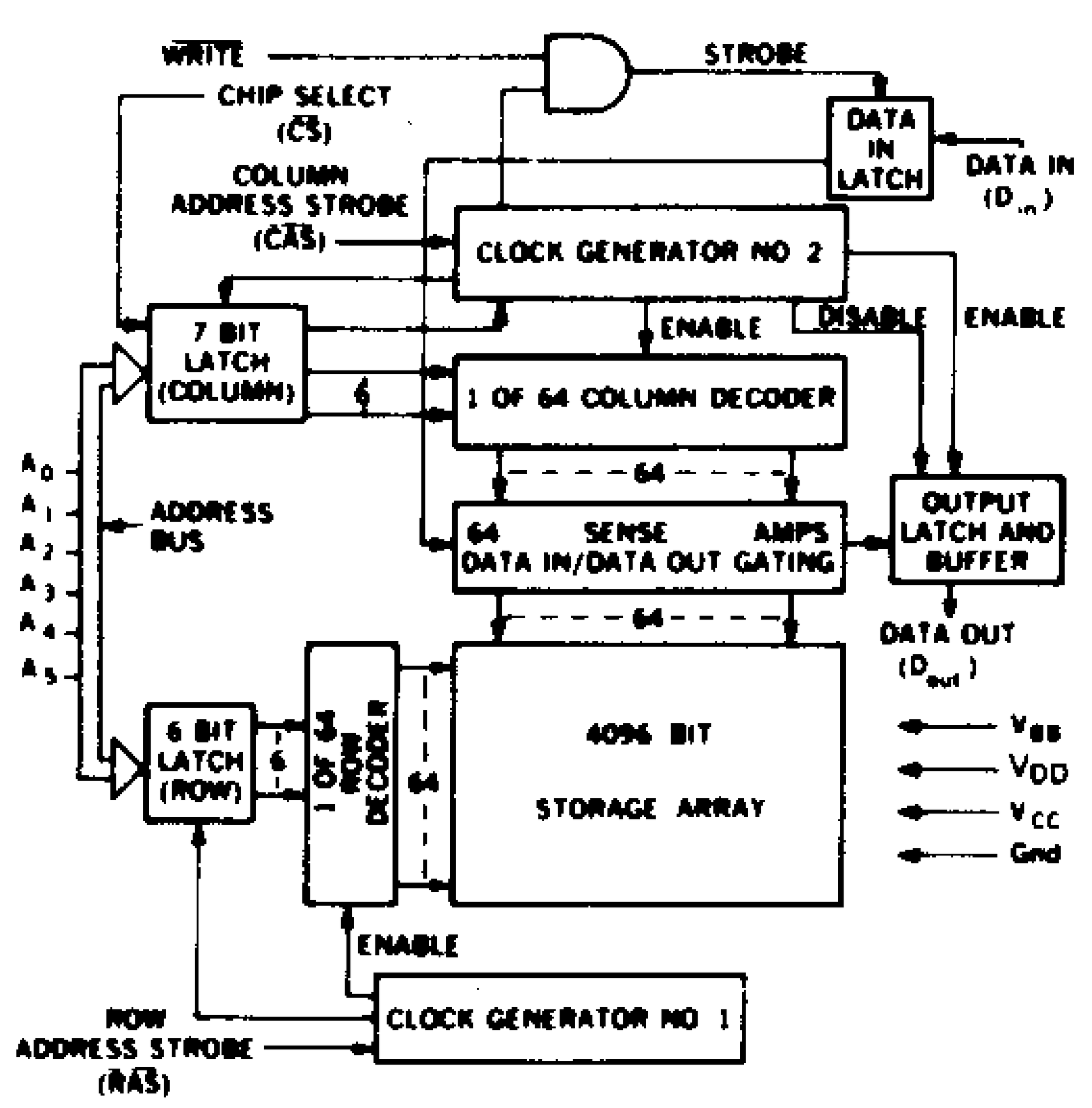
DESCRIPTION

The MK 4096 is the recognized industry standard 4096 word by 1 bit MOS Random Access Memory circuit packaged in a standard 16-pin DIP on 0.3 inch centers. This package configuration is made possible by a unique multiplexing and latching technique for the address inputs. The use of the 16-pin DIP for the MK 4096 provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

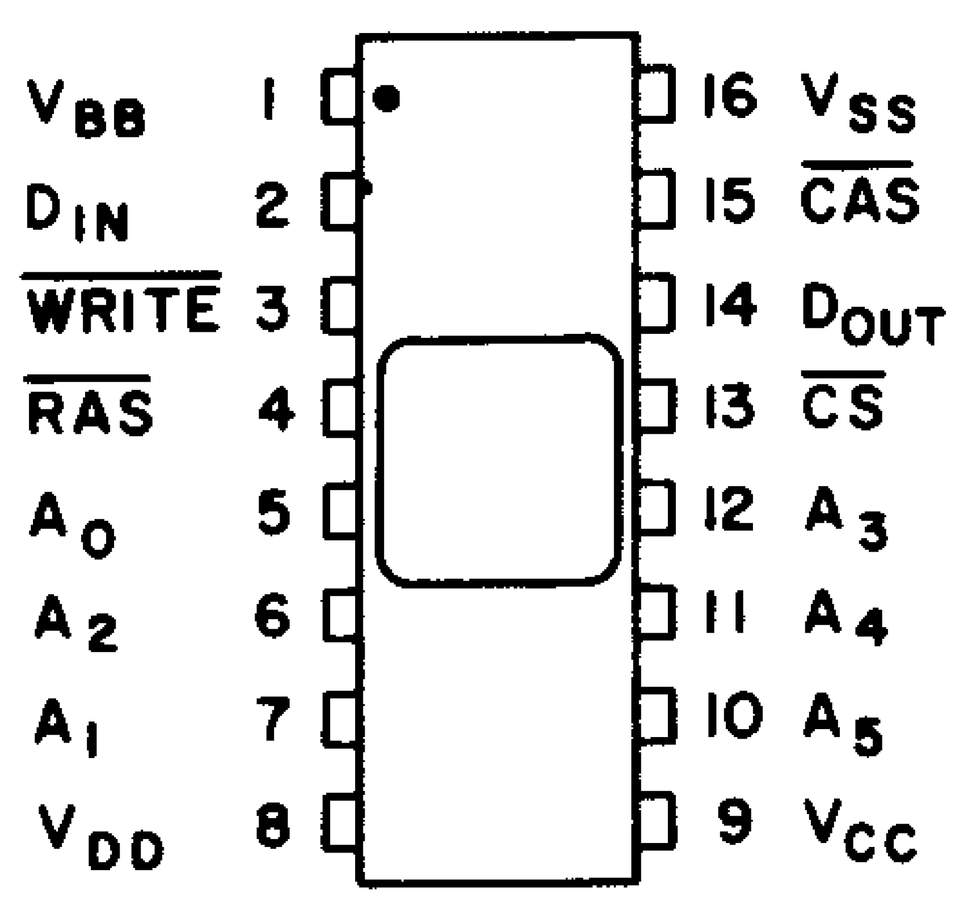
The MK 4096 is fabricated with MOSTEK's standard Self-Aligned, Poly-Interconnect, N-Channel (SPIN) process. The SPIN process allows the MK 4096 to be a highly manufacturable, state-of-the-art memory circuit that exhibits the reliability and performance standards necessary for today's (and tomorrow's) data processing applications. The MK 4096 employs a single transistor storage cell, utilizing a dynamic storage technique and dynamic control circuitry to achieve optimum performance with low power dissipation.

System oriented features incorporated within the MK 4096 include direct interfacing capability with TTL, 6 instead of 12 address lines to drive, on-chip registers which can eliminate the need for interface registers, input logic levels selected to optimize the noise immunity, and two chip select methods to allow the user to determine the speed/power characteristics of his memory system.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN NAMES

A_0 - A_5	ADDRESS INPUTS	D_{IN}	DATA IN
CAS	COLUMN ADDRESS STROBE	D_{OUT}	DATA OUT
CS	CHIP SELECT	V_{BB}	POWER (–5V)
RAS	ROW ADDRESS STROBE	V_{CC}	POWER (+5V)
WRITE	READ/WRITE INPUT	V_{DD}	POWER (+12V)
		V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} . . . . –0.5V to + 25V
($V_{SS}-V_{BB} \geq 4.5V$
Operating temperature T_A (Ambient) . . . . 0°C to + 70°C
Storage temperature (Ceramic) . . . . . . –65°C to + 150°C
Storage temperature (Plastic) . . . . –55°C to + 125°C
Power dissipation 1Watt
Data out current 50mA

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS (17)
($0°C \leq T_A \leq +70°C$)

	PARAMETER	MK 4096–6 MIN	MK 4096–6 MAX	MK 4096–16 MIN	MK 4096–16 MAX	MK 4096–11 MIN	MK 4096–11 MAX	UNITS	NOTES
V_{DD}	Supply Voltage	11.4	12.6	11.4	12.6	11.4	12.6	Volts	1
V_{CC}	Supply Voltage	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	Volts	1,2
V_{SS}	Supply Voltage	0	0	0	0	0	0	Volts	1
V_{BB}	Supply Voltage	–4.5	–5.5	–4.5	–5.5	–4.5	–5.5	Volts	1
V_{IHC}	Logic 1 Voltage – $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.7	7.0	2.7	7.0	3.0	7.0	Volts	1,3
V_{IH}	Logic 1 Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4	7.0	2.4	7.0	2.4	7.0	Volts	1,3
V_{IL}	Logic 0 Voltage, all inputs	–1.0	0.8	–1.0	0.8	–1.0	0.8	Volts	1,3

DC ELECTRICAL CHARACTERISTICS (17)
($0°C \leq T_A \leq 70°C$)(V_{DD} = 12.0V ± 5%; V_{CC} = 5.0V ± 10%; V_{SS} = 0V; V_{BB} = –5.0V ± 10%)

	PARAMETER	MK4096-6 MIN	MK4096-6 MAX	MK4096-16 MIN	MK4096-16 MAX	MK4096-11 MIN	MK4096-11 MAX	UNITS	NOTES
I_{DD1}	Average V_{DD} Power Supply Current		35		30		25	mA	4
I_{CC}	V_{CC} Power Supply Current							mA	5
I_{BB}	Average V_{BB} Power Supply Current		75		75		75	µA	
I_{DD2}	Standby V_{DD} Power Supply Current		1.5		1.5		1.5	mA	7
I_{DD3}	Average V_{DD} Supply Current during "$\overline{RAS}$-only" cycles		25		22		18	mA	4
$I_{I(L)}$	Input Leakage Current (any input)		5		5		5	µA	6
$I_{O(L)}$	Output Leakage Current		10		10		10	µA	7,8
V_{OH}	Output Logic 1 Voltage @ I_{OUT} = –5mA	2.4		2.4		2.4		Volts	2
V_{OL}	Output Logic 0 Voltage @ I_{OUT} = 2mA		0.4		0.4		0.4	Volts	

NOTES

1. All voltages referenced to V_{SS}. V_{BB} must be applied to and removed from the device within 5 seconds of V_{DD}.
2. Output voltage will swing from V_{SS} to V_{CC} if $V_{CC} \leq V_{DD}$ –4 volts. If $V_{CC} \geq V_{DD}$ –4 volts, the output will swing from V_{SS} to a voltage somewhat less than V_{DD}.
3. Device speed is not guaranteed at input voltages greater than TTL levels (0 to 5V).
4. Current is proportional to cycle rate; maximum current is measured at the fastest cycle rate.
5. I_{CC} depends upon output loading. The V_{CC} supply is connected to the output buffer only.
6. All device pins at 0 volts except V_{BB} which is at –5 volts and the pin under test which is at +10 volts.
7. Output is disabled (open-circuit) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1.
8. $0V \leq V_{OUT} \leq +10V$.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (10,15,17)
($0°C \leq T_A \leq 70°C$) (V_{DD} = 12.0V ± 5%, V_{CC} = 5.0V ± 10%, V_{SS} = 0V, V_{BB} = −5.0V ± 10%)

	PARAMETER	MK 4096-6 MIN	MK 4096-6 MAX	MK 4096-16 MIN	MK 4096-16 MAX	MK 4096-11 MIN	MK 4096-11 MAX	UNITS	NOTES
t_{RC}	Random Read or Write Cycle Time	375		425		500		nsec	11
t_{RAC}	Access time from Row Address Strobe		250		300		350		11,13
t_{CAC}	Access Time from Column Address Strobe		140		165		200		12,13
t_{OFF}	Output Buffer Turn-Off Delay	0	65	0	80	0	100		
t_{RP}	Row Address Strobe Precharge Time	115		125		150			
t_{RAS}	Row Address Strobe Pulse Width	250	10,000	300	10,000	350	10,000		
t_{RCL}	Row To Column Strobe Lead Time	60	110	80	135	100	150		14
t_{CAS}	Column Address Strobe Pulse Width	140		165		200			12
t_{AS}	Address Set-Up Time	0		0		0			
t_{AH}	Address Hold Time	60		80		100			
t_{CH}	Chip Select Hold Time	100		100		100			
t_T	Rise and Fall Times	3	50	3	50	3	50		15
t_{RCS}	Read Command Set-Up Time	0		0		0			
t_{RCH}	Read Command Hold Time	0		0		0			
t_{WCH}	Write Command Hold Time	110		130		150			
t_{WP}	Write Command Pulse Width	110		130		150			
t_{CRL}	Column to Row Strobe Lead Time	−40	+40	−50	+50	−50	+50		
t_{CWL}	Write Command to Column Strobe Lead Time	110		130		150			
t_{DS}	Data In Set-Up Time	0		0		0			16
t_{DH}	Data In Hold Time	110		130		150			16
t_{RFSH}	Refresh Period		2		2		2	msec	
t_{MOD}	Modify Time		10		10		10	µsec	
t_{DOH}	Data Out Hold Time	10		10		10		µsec	

NOTES Continued

9. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation: $C = \frac{I \Delta t}{\Delta V}$ with current equal to a constant 20mA.

10. A C measurements assume t_T = 5ns.

11. Assumes that $t_{RCL} + t_T \leq t_{RCL}$ (max).

12. Assumes that $t_{RCL} + t_T \geq t_{RCL}$ (max).

13. Measured with a load circuit equivalent to 1 TTL load and C_L = 100pF.

14. Operation within the t_{RCL} (max) limit insures that t_{RAC} (max) can be met. t_{RCL} (max) is specified as a reference point only; if t_{RCL} is greater than the specified t_{RCL} (max) limit, then access time is controlled exclusively by t_{CAC} and t_{RAS} . t_{RAC} and t_{RCL} will be longer by the amount $t_{RCL} + t_T$ exceeds t_{RCL} (max).

15. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

16. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

17. After the application of supply voltages or after extended periods of operation without clocks, the device must perform a minimum of one initialization cycle (any valid memory cycle containing both $\overline{RAS}$ and $\overline{CAS}$) prior to normal operation.

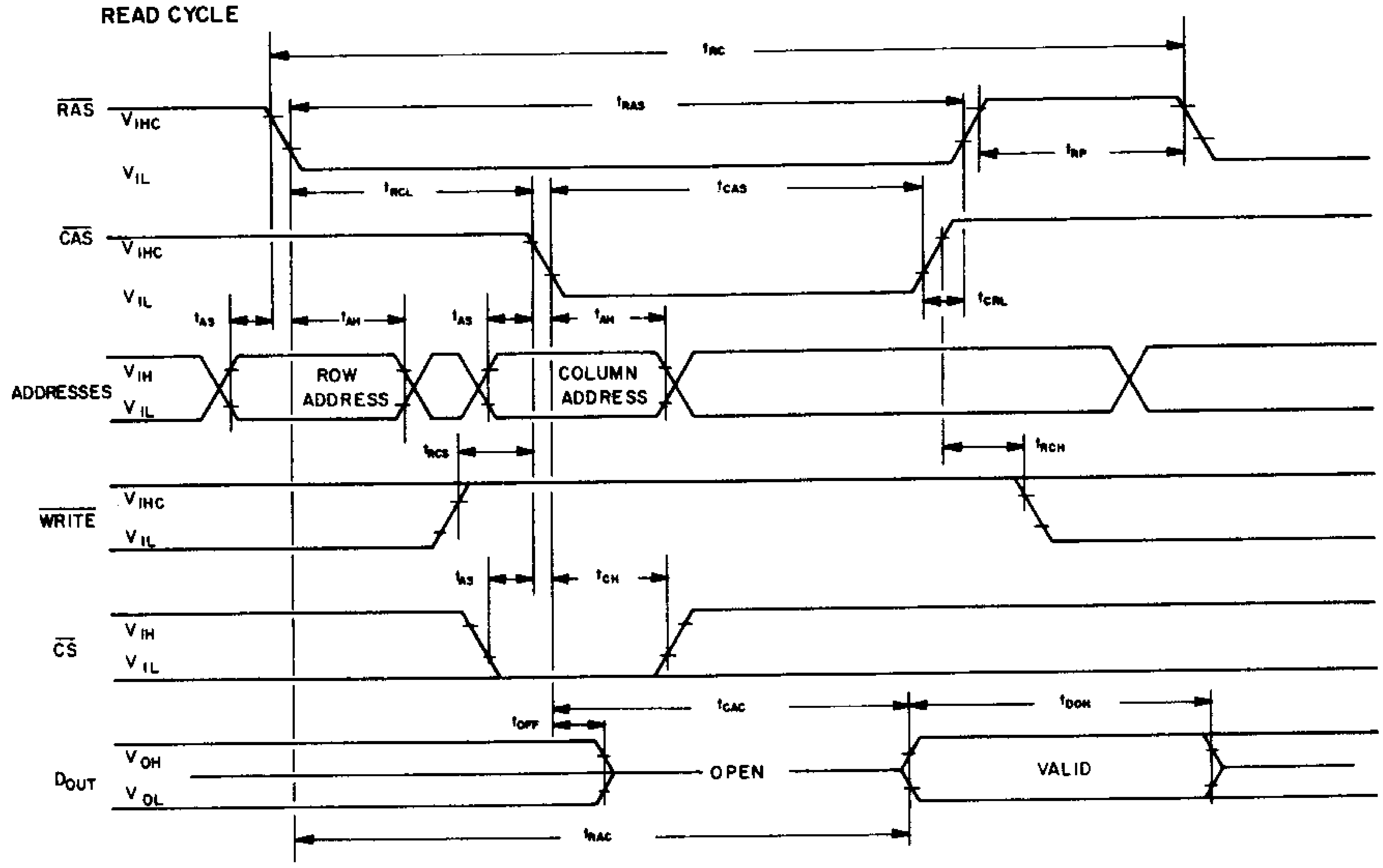
AC ELECTRICAL CHARACTERISTICS

$(0°C \leq T_A \leq +70°C)$ $(V_{DD} = 12.0V \pm 5\%, V_{CC} = 5.0V \pm 10\%, V_{SS} = 0V, V_{BB} = -5.0V \pm 10\%)$

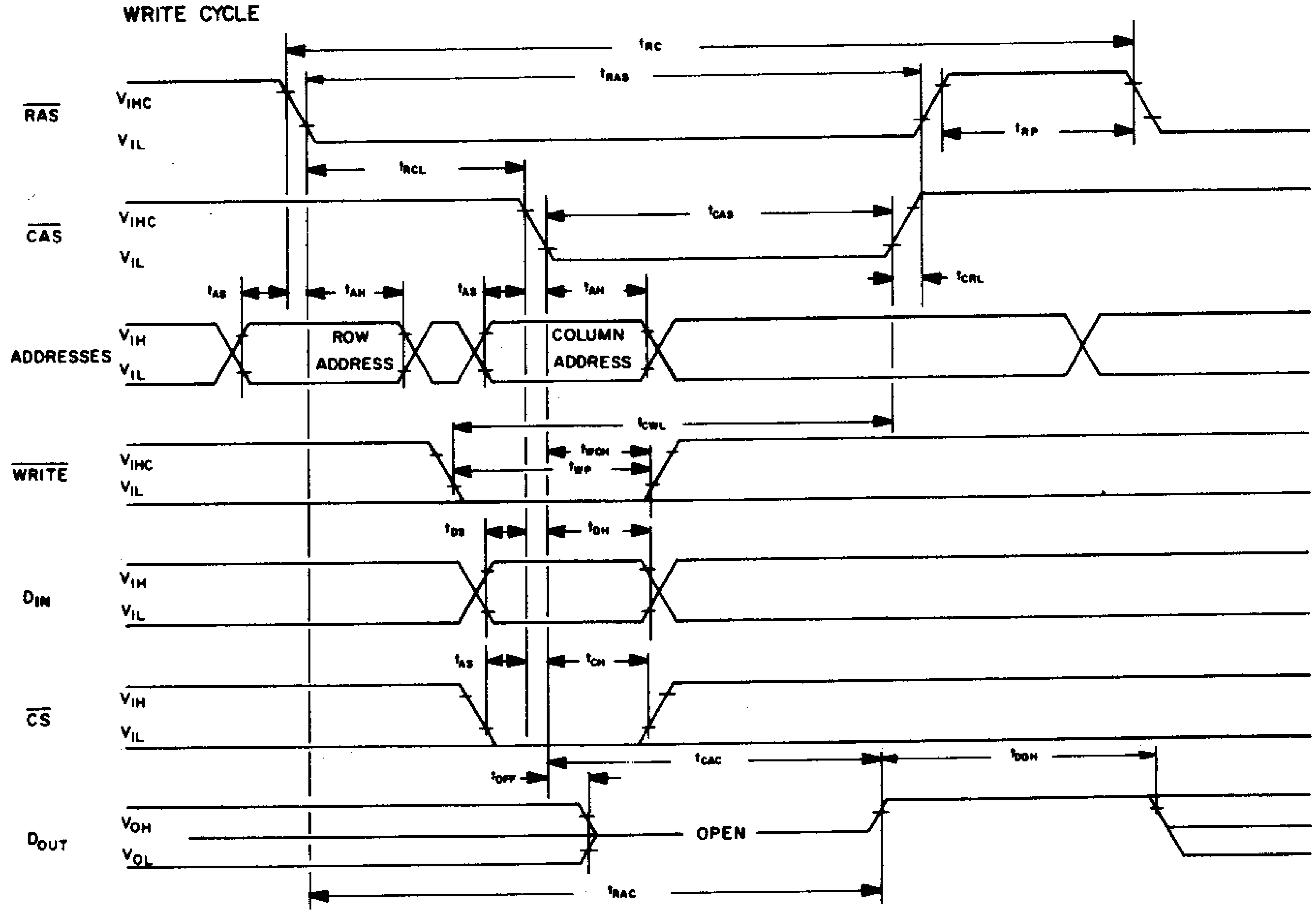
	PARAMETER	TYP	MAX	UNITS	NOTES
C_{I1}	Input Capacitance ($A_0 - A_5$)	7	10	pF	9
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, D_{IN}, $\overline{WRITE}$, $\overline{CS}$)	5	7	pF	9
C_O	Output Capacitance (D_{OUT})	5	8	pF	7,9

TIMING WAVEFORMS

READ CYCLE

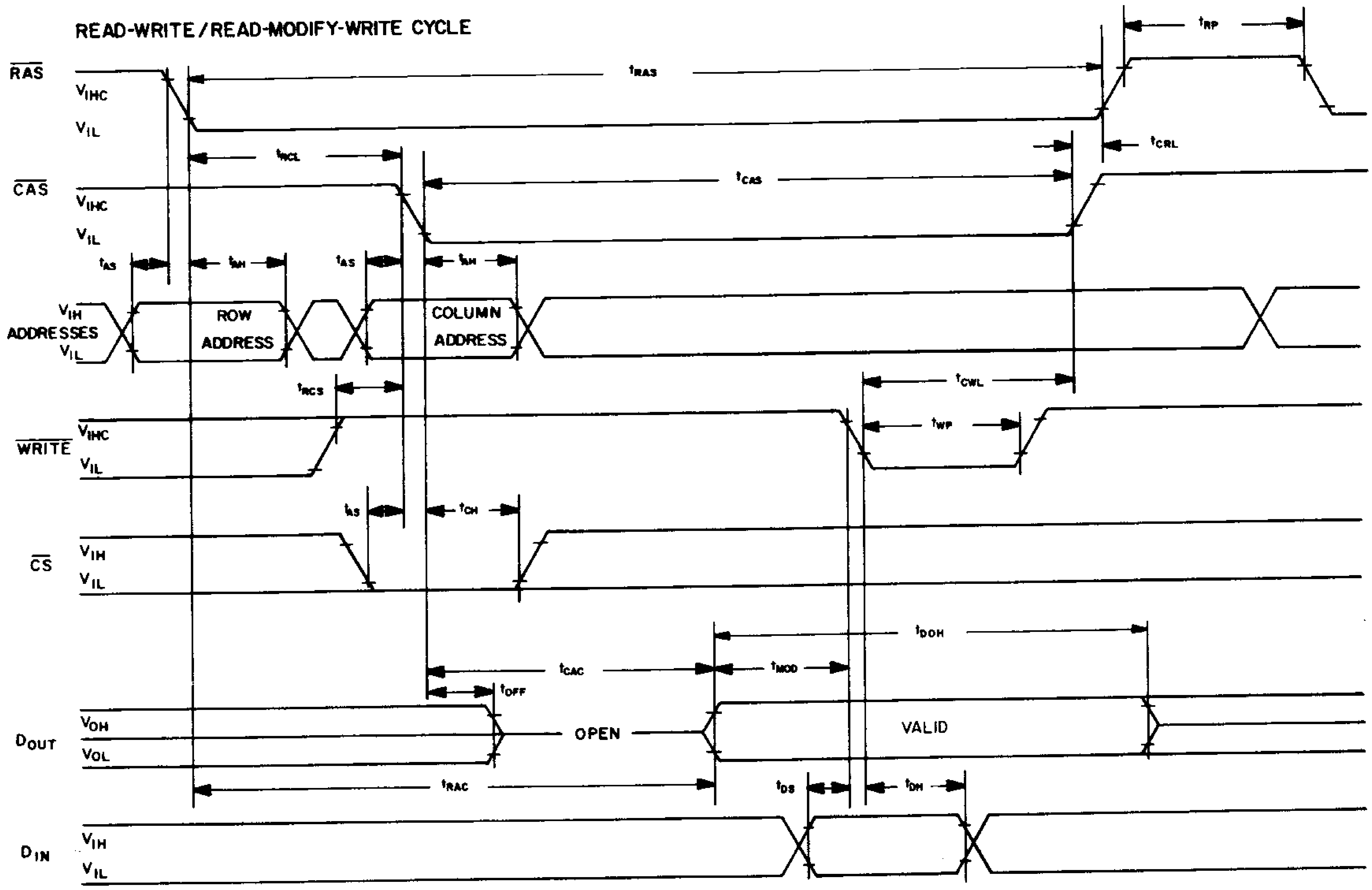


WRITE CYCLE

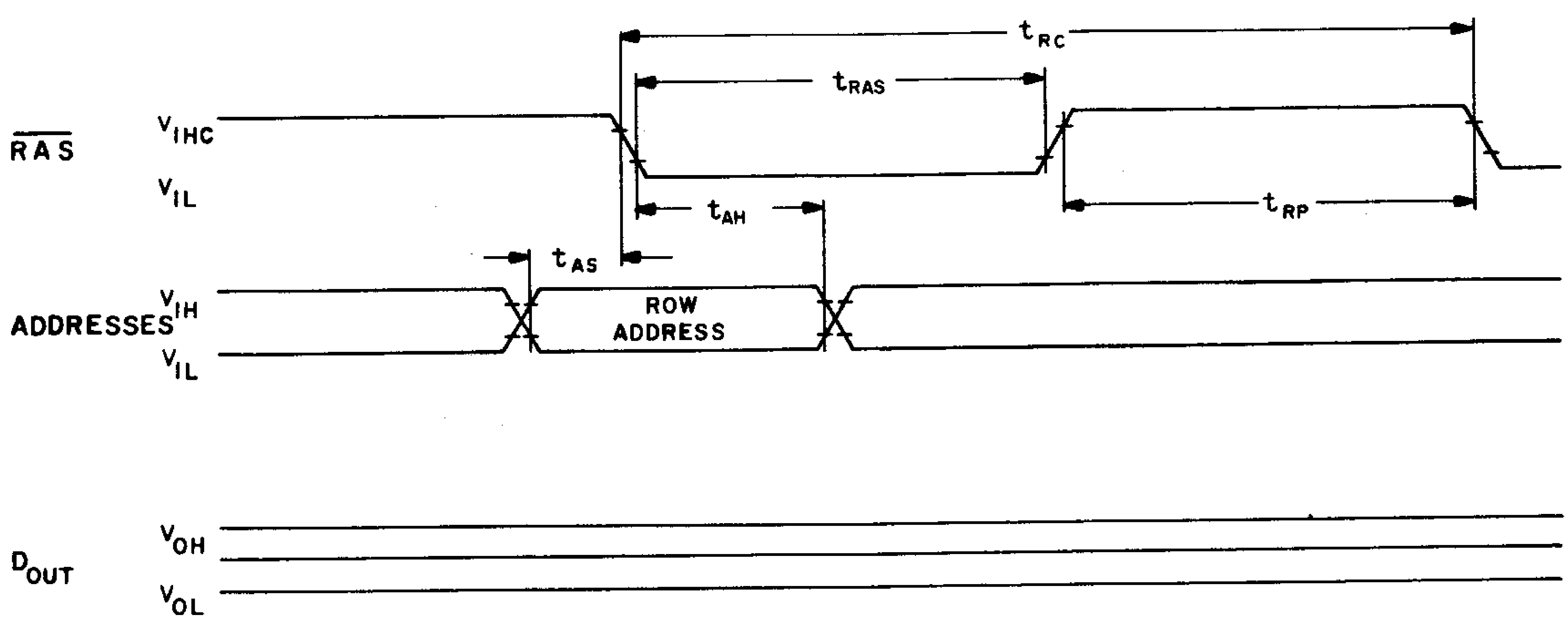


TIMING WAVEFORMS

READ-WRITE/READ-MODIFY-WRITE CYCLE



"$\overline{RAS}$ ONLY" REFRESH CYCLE



NOTE:

Prior to the first memory cycle following a period (beyond 2mS) of "$\overline{RAS}$-only refresh, a memory-cycle employing both $\overline{RAS}$ and $\overline{CAS}$ must be performed to insure proper device operation.

ADDRESSING

The 12 address bits required to decode one of the 4096 cell locations within the MK 4096 are multiplexed onto the 6 address inputs and latched into the on-chip address latches by externally applying two negative going TTL level clocks. The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 6 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 6 column address bits plus Chip Select ($\overline{CS}$) into the chip. (Note that since the Chip Select signal is not required until $\overline{CAS}$ time, which is well into the memory cycle, its decoding time does not add to system access or cycle time). Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{AH}) has been satisfied and the 6 address inputs have been changed from Row address to Column address information.

Note that $\overline{CAS}$ can be activated at any time after t_{AH} and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing end points result from the internal gating of $\overline{CAS}$ which are called t_{RCL} (min) and t_{RCL} (max). No data storage or reading errors will result if $\overline{CAS}$ is applied to the MK 4096 at a point in time beyond the t_{RCL} (max) limit. However, access time will then be determined exclusively by the access time from $\overline{CAS}$ (t_{CAC}) rather than from $\overline{RAS}$ (t_{RAC}), and access time from $\overline{RAS}$ will be lengthened by the amount that t_{RCL} exceeds the t_{RCL} (max) limit.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low prior to $\overline{CAS}$, the Data In is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. If the data input is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write or read-modify-write cycle, the $\overline{WRITE}$ signal must be delayed until after $\overline{CAS}$. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than to $\overline{CAS}$. (To illustrate this feature, Data In is referenced to $\overline{WRITE}$ in the timing diagram depicting the read-modify-write cycle while the "early write" cycle diagram shows Data In referenced to $\overline{CAS}$). Note that if the chip is unselected ($\overline{CS}$ high at $\overline{CAS}$ time) $\overline{WRITE}$ commands are not executed and, consequently, data stored in the memory is unaffected.

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cyle in which $\overline{CAS}$ is active. Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT LATCH

Any change in the condition of the Data Out Latch is initiated by the $\overline{CAS}$ signal. The output buffer is not affected by memory (refresh) cycles in which only the $\overline{RAS}$ signal is applied to the MK 4096. Whenever $\overline{CAS}$ makes a negative transition, the output will go unconditionally open-circuited, independent of the state of any other input to the chip. If the cycle in progress is a read, read-modify-write, or a delayed write cycle and the chip is selected, then the output latch and buffer will again go active and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. If the cycle in progress is a write cycle ($\overline{WRITE}$ active low before $\overline{CAS}$ goes low) and the chip is selected, then at access time the output latch and buffer will contain a logic 1. Once having gone active, the output will remain valid until the MK 4096 receives the next $\overline{CAS}$ negative edge. Intervening refresh cycles in which a $\overline{RAS}$ is received (but no $\overline{CAS}$) will not cause valid data to be affected. Conversely, the output will assume the open-circuit state during any cycle in which the MK 4096 receives a $\overline{CAS}$ but no $\overline{RAS}$ signal (regardless of the state of any other inputs). The output will also assume the open-circuit state in normal cycles (in which both $\overline{RAS}$ and $\overline{CAS}$ signals occur) if the chip is unselected.

The three-state data output buffer presents the data output pin with a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The effective resistance to V_{CC} (logic 1 state) is 500Ω maximum and 150Ω typically. The resistance to V_{SS} (logic 0 state) is 200Ω maximum and 100Ω typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may have power removed without affecting the MK 4096 refresh operation. This allows all system logic except the $\overline{RAS}/\overline{CAS}$ timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses within each 2 millisecond time interval. Any cycle in which a $\overline{RAS}$ signal occurs accomplishes a refresh operation. A read cycle will refresh the selected row, regardless of the Chip Select ($\overline{CS}$) input. A write or read-modify-write cycle also refreshes the selected row, but the chip should be unselected to prevent writing data into the selected cell.

For standby operation, a "$\overline{RAS}$-only" cycle can be employed to refresh the MK 4096. However, if "$\overline{RAS}$-only" refresh cycles (where $\overline{RAS}$ is the only signal applied to the chip) are continued for extended periods, the output buffer may eventually lose proper data and go open-circuit. Prior to the first memory cycle following a period (beyond 2ms) of "$\overline{RAS}$-only" refresh, a memory cycle employing both $\overline{RAS}$ and $\overline{CAS}$ must be performed to precharge the internal circuitry. This "dummy cycle" allows the output buffer to regain activity and enables the device to perform a read or write cycle upon command.

POWER DISSIPATION/STANDBY MODE

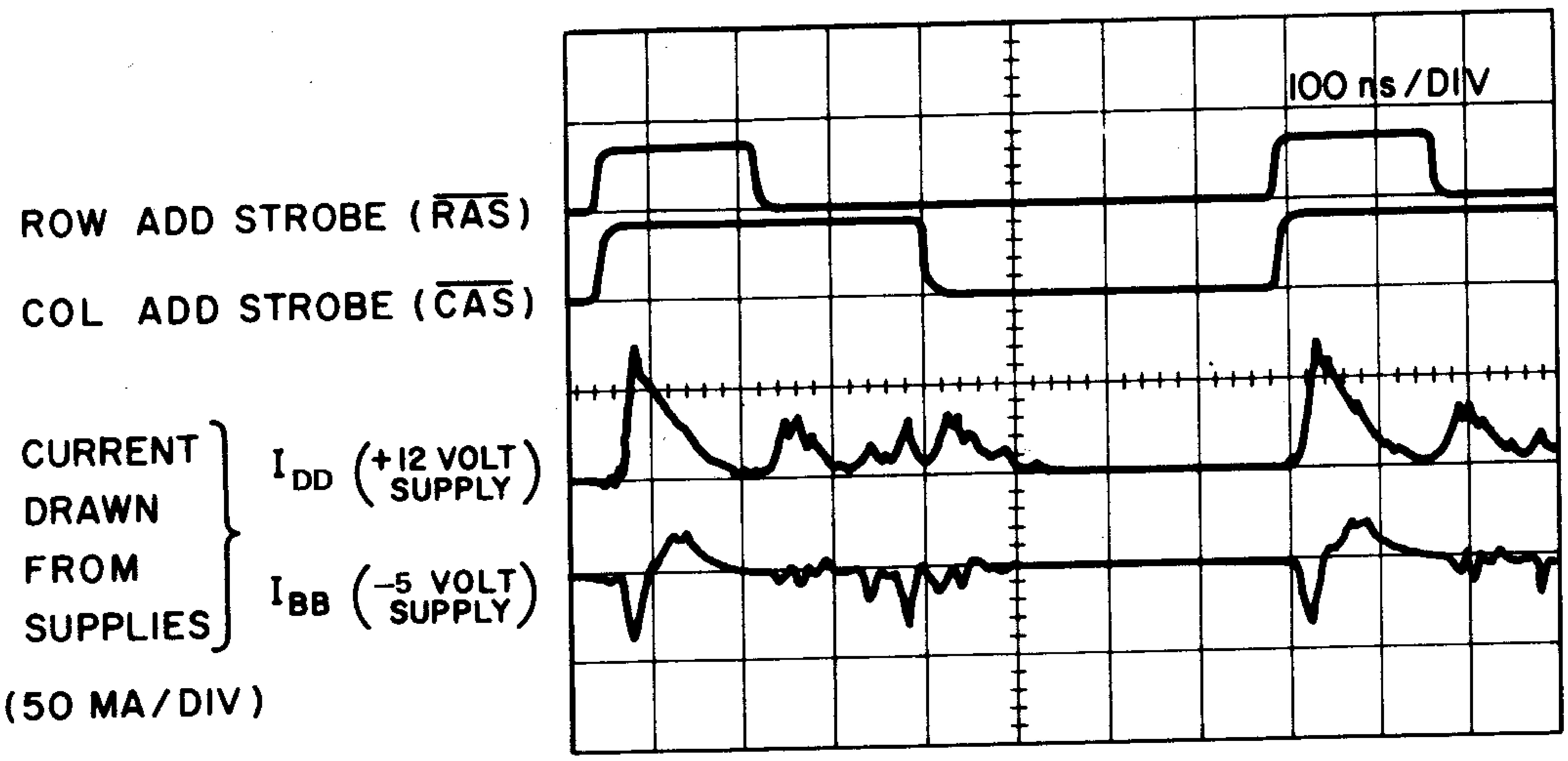
Most of the circuitry used in the MK 4096 is dynamic and most of the power drawn is the result of an address strobe edge. Because the power is not drawn during the whole time the strobe is active, the dynamic power is a function of operating frequency rather than active duty cycle. Typically, the power is 120 mW at a 1 μsec cycle rate for the MK 4096 with a maximum power of less than 450 mW at 375 nsec cycle time. To minimize the overall system power, the Row Address Strobe ($\overline{RAS}$) should be decoded and supplied to only the selected chips. The $\overline{CAS}$ must be supplied to all chips (to turn off the unselected output). Those chips that did not receive a $\overline{RAS}$, however, will not dissipate any power on the $\overline{CAS}$ edges, except for that required to turn off the outputs. If the $\overline{RAS}$ signal is decoded and supplied only to the selected chips, then the Chip Select ($\overline{CS}$) input of all chips can be at a logic 0. The chips that receive a $\overline{CAS}$ but no $\overline{RAS}$ will be unselected (output open-circuited) regardless of the Chip Select input. For refresh cycles, however, either the $\overline{CS}$ input of all chips must be high or the $\overline{CAS}$ input must be held high to prevent several "wire-ORed" outputs from turning on with opposing force.

The current waveforms for the current drawn from the V_{DD} and V_{BB} supplies are shown in Figure A. Since the current is pulsed, proper power distribution and bypassing techniques are required to maintain system power supply noise levels at an acceptable level. Low inductance supply lines for V_{DD} and V_{SS} are desirable. One 0.01 microfarad, low inductance, bypass capacitor per two MK 4096 devices and one 6.8 microfarad electrolytic capacitor per eight MK 4096 devices on each of the V_{DD} and V_{BB} supply lines is desirable.

POWER–UP

Under normal operating conditions the MK 4096 requires no particular power-up sequence. However, in order to achieve the most reliable performance from the MK 4096, proper consideration should be given to the V_{BB}/V_{DD} power supply relationship. The V_{BB} supply is an extremely important "protective voltage" since it performs two essential functions within the device. It establishes proper junction isolation and sets field-effect thresholds, both thin field and thick field. Misapplication of V_{BB} or device operation without the V_{BB} supply can affect long term device reliability. For optimum reliability performance from the MK 4096, it is suggested that measures be taken to not have V_{DD} (+12V) applied to the device for over five (5) seconds without the application of V_{BB} (−5V).

After power is applied to the device, the MK 4096 requires at least one memory cycle ($\overline{RAS}/\overline{CAS}$) before proper device operation is achieved. A normal 64 cycle refresh with both $\overline{RAS}$ and $\overline{CAS}$ is adequate for this purpose.



Power Supply Current Waveforms

MOSTEK

4096 X 1 BIT DYNAMIC RAM

MK4096 (P/N)-15

FEATURES

- ☐ Industry standard 16-pin DIP configuration
- ☐ Access time 350ns (MAX)
- ☐ Input latches for address, chip select and data in
- ☐ All inputs are low capacitance and TTL compatible
- ☐ Low cost for consumer and hobbyist microprocessor applications
- ☐ Three-state TTL compatible output, latched and valid into next cycle
- ☐ Low power dissipation
- ☐ Inputs protected against static charge

DESCRIPTION

The MK 4096 is the recognized industry standard 4096 word by 1 bit MOS Random Access Memory circuit packaged in a standard 16-pin DIP on 0.3 inch centers. This package configuration is made possible by a unique multiplexing and latching technique for the address inputs. The use of the 16-pin DIP for the MK 4096 provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

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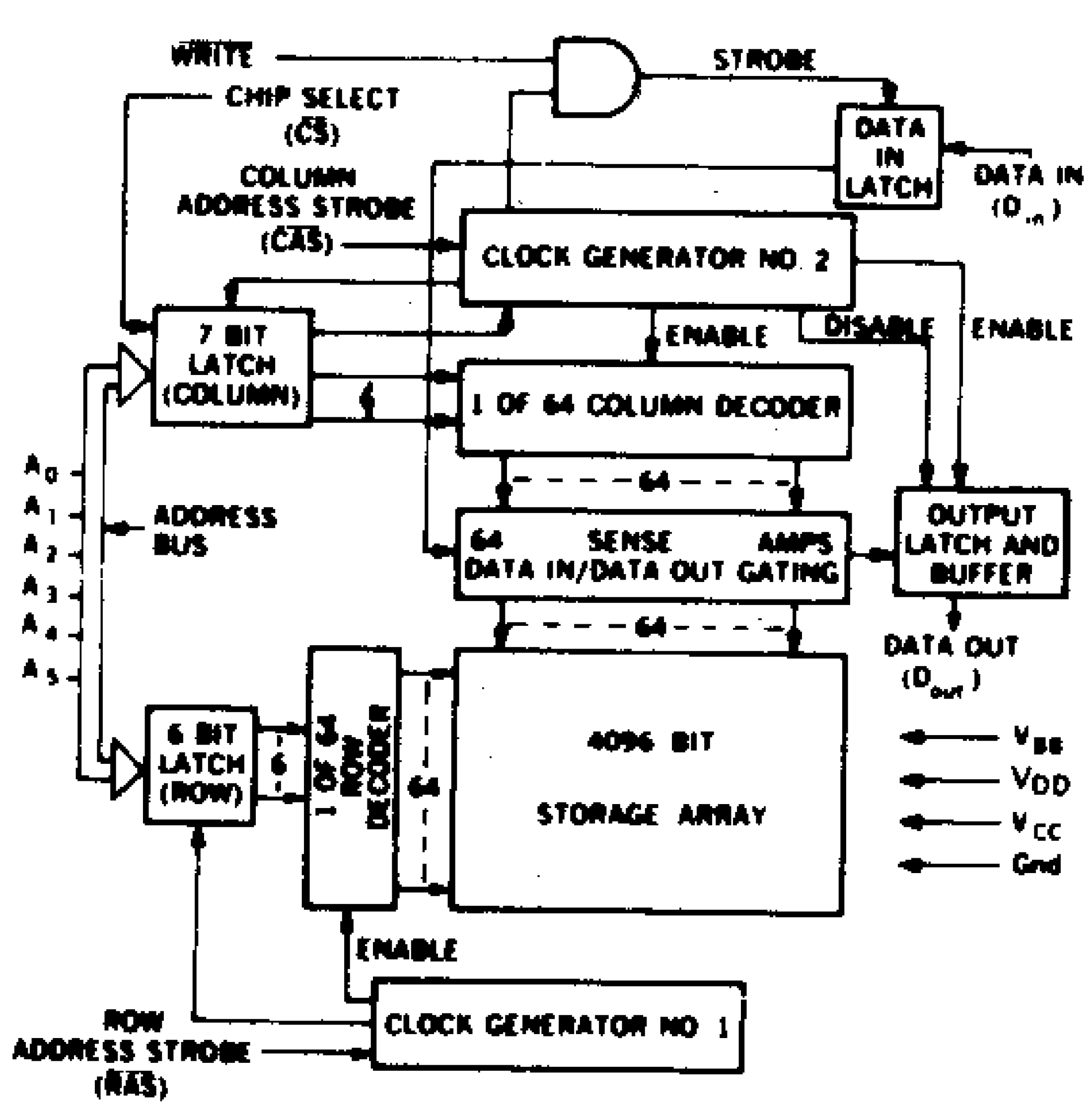
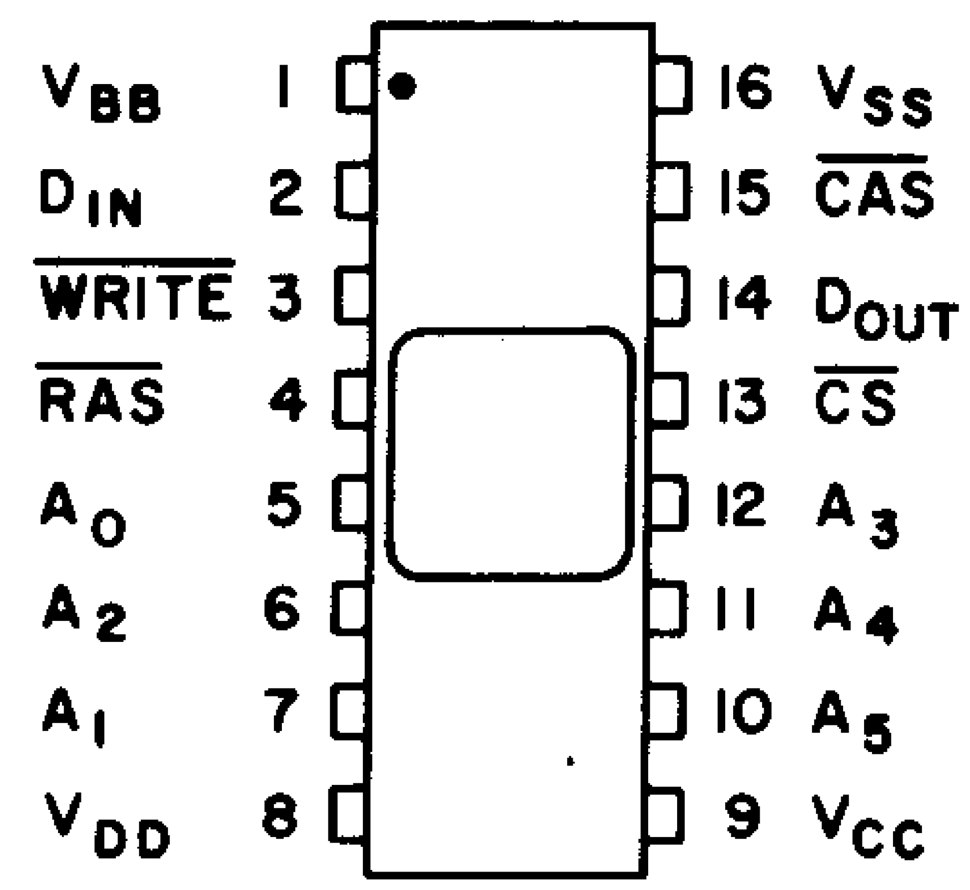
System oriented features incorporated within the MK 4096 include direct interfacing capability with TTL, 6 instead of 12 address lines to drive, on-chip registers which can eliminate the need for interface registers, input logic levels selected to optimize the noise immunity, and two chip select methods to allow the user to determine the speed/power characteristics of his memory system.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN NAMES

A_0 - A_5	ADDRESS INPUTS	D_{IN}	DATA IN
$\overline{CAS}$	COLUMN ADDRESS STROBE	D_{OUT}	DATA OUT
$\overline{CS}$	CHIP SELECT	V_{BB}	POWER (−5V)
$\overline{RAS}$	ROW ADDRESS STROBE	V_{CC}	POWER (+5V)
$\overline{WRITE}$	READ/WRITE INPUT	V_{DD}	POWER (+15V)
		V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} .... –0.5V to + 25V
(V_{SS}–V_{BB} ≥ 4.5V
Operating temperature T_A (Ambient) .... 0°C to + 55°C
Storage temperature (Ceramic) ...... –65°C to + 150°C
Storage temperature (Plastic) .... –55°C to + 125°C
Power dissipation .... 1 Watt
Data out current 50mA

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS (17)
(0°C ≤ T_A ≤ +55°C)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	14.25	15.0	15.75	Volts	1
V_{CC}	Supply Voltage	V_{SS}		V_{DD}	Volts	1,2
V_{SS}	Supply Voltage	0		0	Volts	1
V_{BB}	Supply Voltage	–4.5	–5.0	–5.5	Volts	1
V_{IHC}	Logic 1 Voltage –$\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	3.5		7.0	Volts	1,3
V_{IH}	Logic 1 Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	3.0		7.0	Volts	1,3
V_{IL}	Logic 0 Voltage, all inputs	–1.0		0.8	Volts	1,3

DC ELECTRICAL CHARACTERISTICS (17)
(0°C ≤ T_A ≤ 55°C) (V_{DD} = 15.0V ± 5%; V_{CC} = 5.0V ± 10%; V_{SS} = 0V; V_{BB} = –5.0V ± 10%)

	PARAMETER	MIN	MAX	UNITS	NOTES
I_{DD1}	Average V_{DD} Power Supply Current		35	mA	4
I_{CC}	V_{CC} Power Supply Current			mA	5
I_{BB}	Average V_{BB} Power Supply Current		75	μA	
I_{DD2}	Standby V_{DD} Power Supply Current		2	mA	7
I_{DD3}	Average V_{DD} Supply Current during "$\overline{RAS}$-only" cycles		24	mA	4
$I_{I(L)}$	Input Leakage Current (any input)		5	μA	6
$I_{O(L)}$	Output Leakage Current		10	μA	7,8
V_{OH}	Output Logic 1 Voltage @ I_{OUT} = –5mA	2.4		Volts	2
V_{OL}	Output Logic 0 Voltage @ I_{OUT} = 2mA		0.4	Volts	

NOTES

1. All voltages referenced to V_{SS}. V_{BB} must be applied to and removed from the device within 5 seconds of V_{DD}.
2. Output voltage will swing from V_{SS} to V_{CC} if $V_{CC} \leq V_{DD} - 4$ volts. If $V_{CC} \geq V_{DD} - 4$ volts, the output will swing from V_{SS} to a voltage somewhat less than V_{DD}.
3. Device speed is not guaranteed at input voltages greater than TTL levels (0 to 5V).
4. Current is proportional to cycle rate; maximum current is measured at the fastest cycle rate.
5. I_{CC} depends upon output loading. The V_{CC} supply is connected to the output buffer only.
6. All device pins at 0 volts except V_{BB} which is at –5 volts and the pin under test which is at +10 volts.
7. Output is disabled (open-circuit) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1.
8. $0V \leq V_{OUT} \leq +10V$.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITONS (10,15,17)
($0°C \leq T_A \leq 55°C$) (V_{DD} = 15.0V ± 5%; V_{CC} = 5.0V ± 10%, V_{SS} = 0V, V_{BB} = –5.0V ±10%)

PARAMETER		MIN	MAX	UNITS	NOTES
t_{RC}	Random Read or Write Cycle Time	500		nsec	11
t_{RAC}	Access time from Row Address Strobe		350	nsec	11,13
t_{CAC}	Access Time from Column Address Strobe		200	nsec	12,13
t_{OFF}	Output Buffer Turn-Off Delay	0	100	nsec	
t_{RP}	Row Address Strobe Precharge Time	150		nsec	
t_{RAS}	Row Address Strobe Pulse Width	350	10,000	nsec	
t_{RCL}	Row To Column Strobe Lead Time	100	150	nsec	14
t_{CAS}	Column Address Strobe Pulse Width	200		nsec	12
t_{AS}	Address Set-Up Time	0		nsec	
t_{AH}	Address Hold Time	100		nsec	
t_{CH}	Chip Select Hold Time	100		nsec	
t_T	Rise and Fall Times	3	50	nsec	15
t_{RCS}	Read Command Set-Up Time	0		nsec	
t_{RCH}	Read Command Hold Time	0		nsec	
t_{WCH}	Write Command Hold Time	150		nsec	
t_{WP}	Write Command Pulse Width	150		nsec	
t_{CRL}	Column to Row Strobe Lead Time	–50	+50	nsec	
t_{CWL}	Write Command to Column Strobe Lead Time	150		nsec	
t_{DS}	Data In Set-Up Time	0		nsec	16
t_{DH}	Data In Hold Time	150		nsec	16
t_{RFSH}	Refresh Period		1	msec	
t_{MOD}	Modify Time		10	μ sec	
t_{DOH}	Data Out Hold Time	10		μ sec	

NOTES Continued

9. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation: $C = \frac{I \Delta t}{\Delta V}$ with current equal to a constant 20mA.

10. A C measurements assume t_T = 5ns.

11. Assumes that $t_{RCL} + t_T \leq t_{RCL}$ (max).

12. Assumes that $t_{RCL} + t_T \geq t_{RCL}$ (max).

13. Measured with a load circuit equivalent to 1 TTL load and C_L = 100pF.

14. Operation within the t_{RCL} (max) limit insures that t_{RAC} (max) can be met. t_{RCL} (max) is specified as a reference point only; if t_{RCL} is greater than the specified t_{RCL} (max) limit, then access time is controlled exclusively by t_{CAC} and t_{RAS} . t_{RAC} and t_{RCL} will be longer by the amount $t_{RCL} + t_T$ exceeds t_{RCL} (max).

15. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

16. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

17. After the application of supply voltages or after extended periods of operation without clocks, the device must perform a minimum of one initialization cycle (any valid memory cycle containing both $\overline{RAS}$ and $\overline{CAS}$) prior to normal operation.

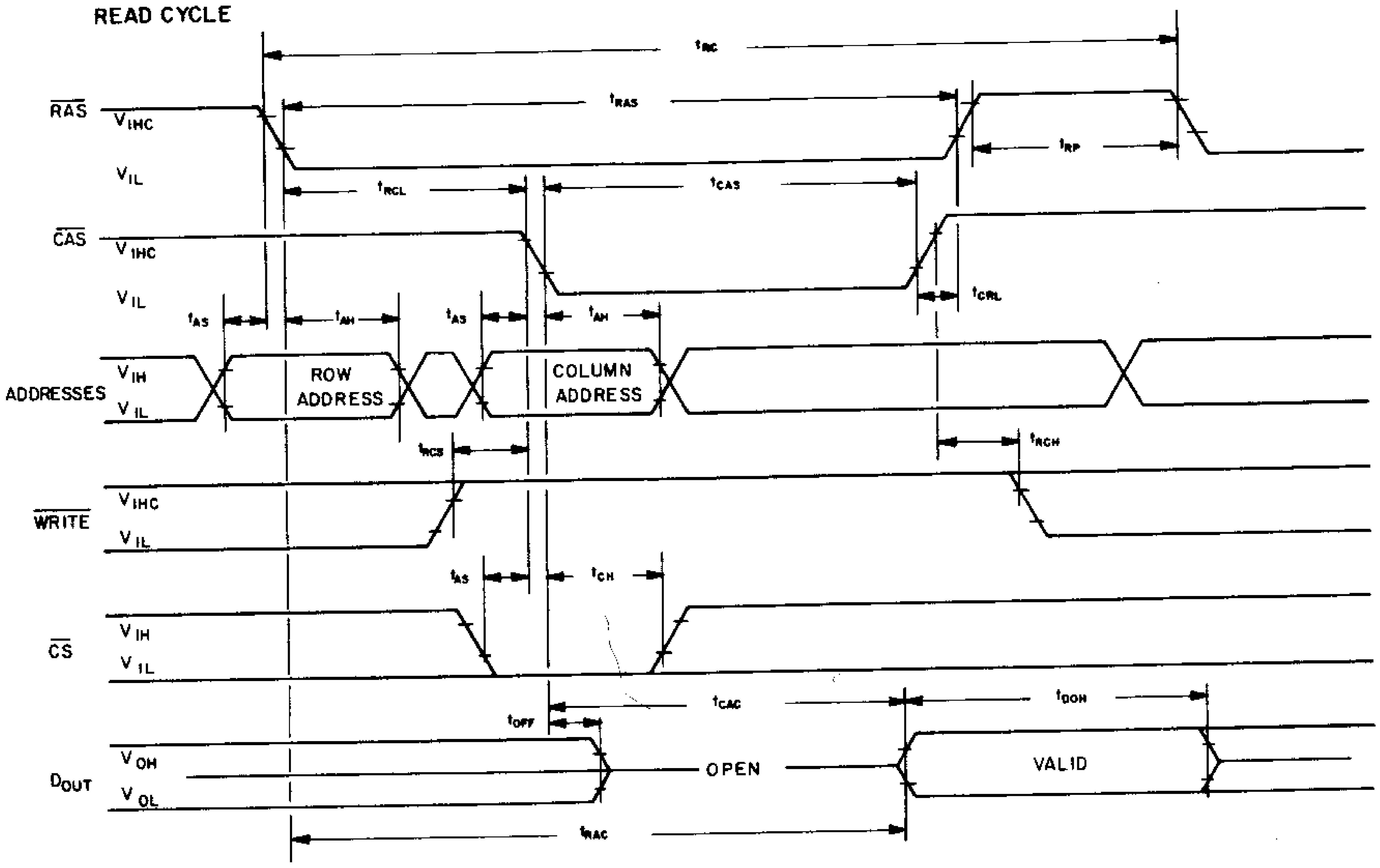
AC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ + 55°C) (V_{DD} = 15.0V ± 5%, V_{CC} = 5.0V ± 10%, V_{SS} = 0V, V_{BB} = –5.0V ± 10%)

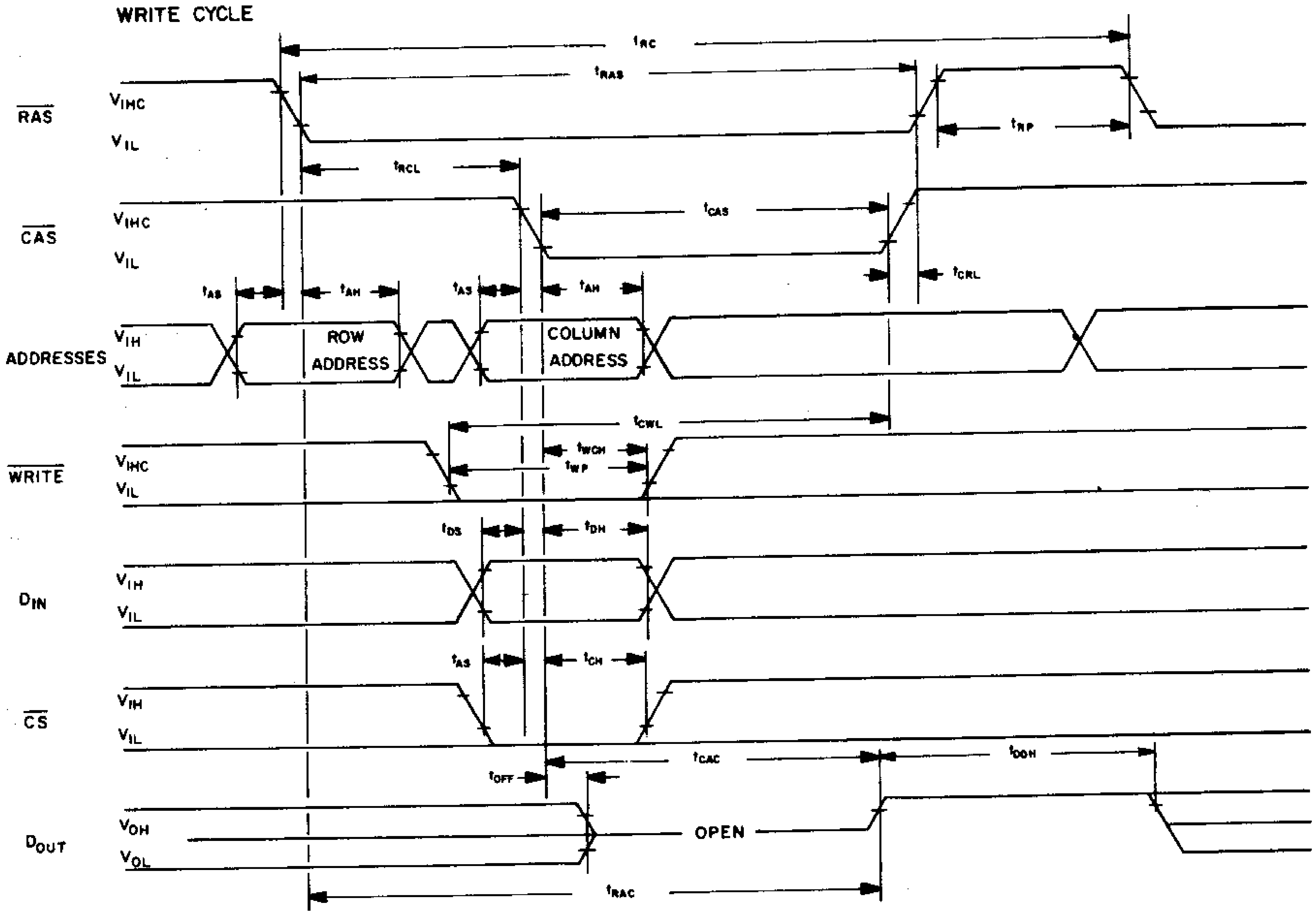
	PARAMETER	TYP	MAX	UNITS	NOTES
C_{I1}	Input Capacitance (A_0 – A_5)	7	10	pF	9
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, D_{IN}, $\overline{WRITE}$, $\overline{CS}$)	5	7	pF	9
C_O	Output Capacitance (D_{OUT})	5	8	pF	7,9

TIMING WAVEFORMS

READ CYCLE

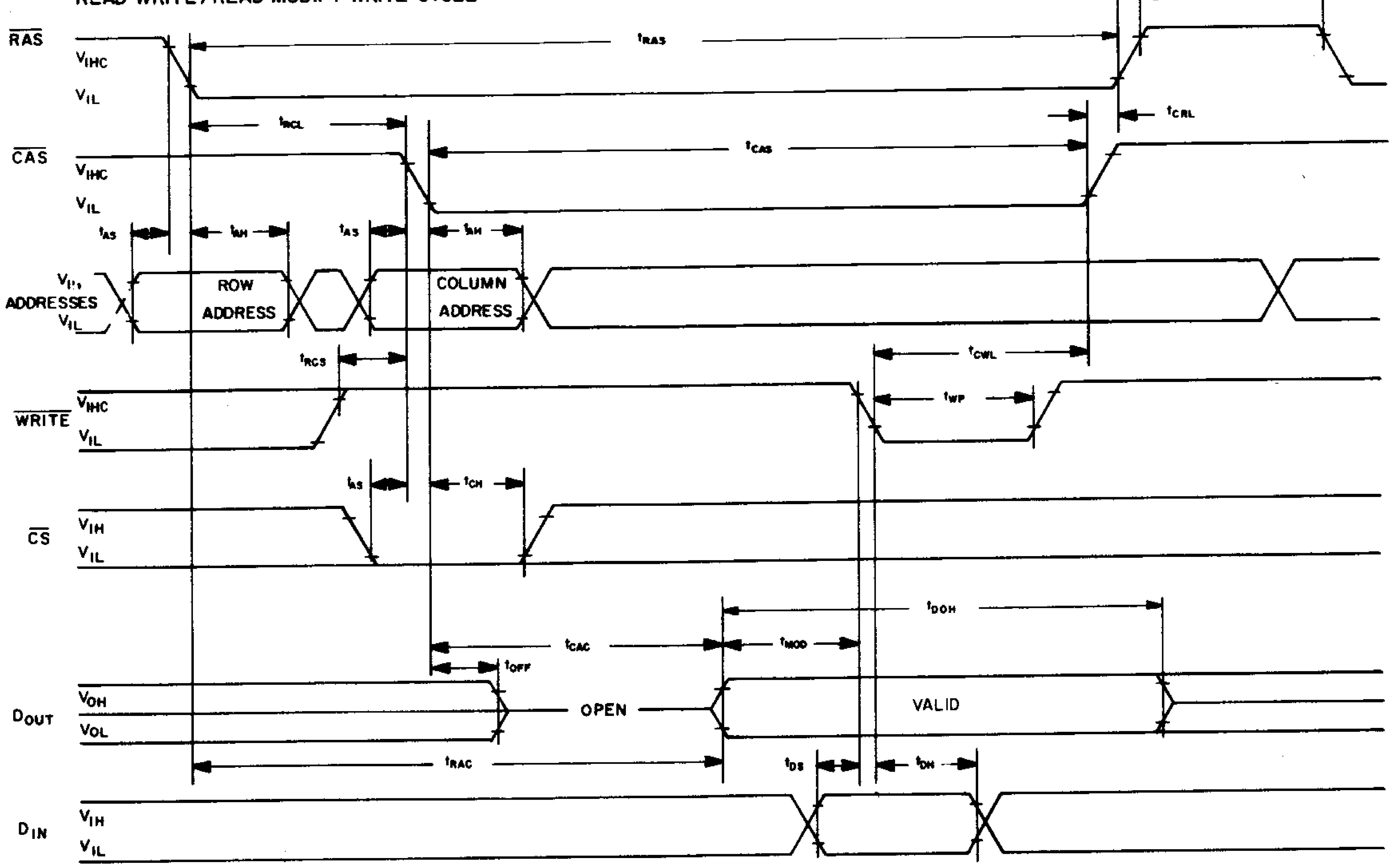


WRITE CYCLE

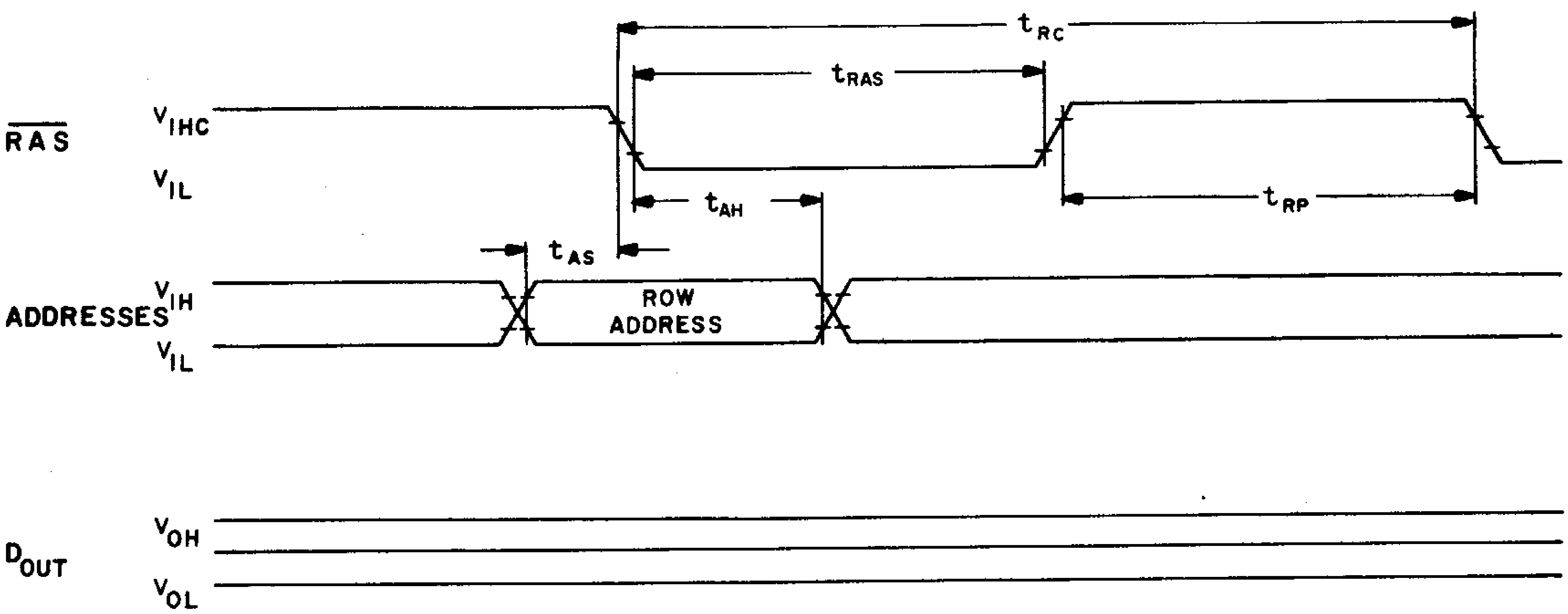


TIMING WAVEFORMS

READ-WRITE / READ-MODIFY-WRITE CYCLE



"RAS ONLY" REFRESH CYCLE (See text under Refresh)



NOTE:

Prior to the first memory cycle following a period (beyond 1mS) of "RAS-only refresh, a memory cycle employing both RAS and CAS must be performed to insure proper device operation.

ADDRESSING

The 12 address bits required to decode one of the 4096 cell locations within the MK 4096 are multiplexed onto the 6 address inputs and latched into the on-chip address latches by externally applying two negative going TTL level clocks. The first clock, the Row Address Strobe (RAS), latches the 6 row address bits into the chip. The second clock, the Column Address Strobe (CAS), subsequently latches the 6 column address bits plus Chip Select (CS) into the chip. (Note that since the Chip Select signal is not required until CAS time, which is well into the memory cycle, its decoding time does not add to system access or cycle time). Each of these signals, RAS and CAS, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the CAS clock sequence are inhibited until the occurrence of a delayed signal derived from the RAS clock chain. This " gated CAS" feature allows the CAS clock to be externally activated as soon as the Row Address Hold Time specification (t_{AH}) has been satisfied and the 6 address inputs have been changed from Row address to Column address information.

Note that CAS can be activated at any time after t_{AH} and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing end points result from the internal gating of CAS which are called t_{RCL} (min) and t_{RCL} (max). No data storage or reading errors will result if CAS is applied to the MK 4096 at a point in time beyond the t_{RCL} (max) limit. However, access time will then be determined exclusively by the access time from CAS (t_{CAC}) rather than from RAS (t_{RAC}), and access time from RAS will be lengthened by the amount that t_{RCL} exceeds the t_{RCL} (max) limit.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of WRITE and CAS while RAS is active. The later of the signals (WRITE or CAS) to make its negative transition is the strobe for the Data In register. This permits several options in the write cycle timing. In a write cycle, if the WRITE input is brought low prior to CAS, the Data In is strobed by CAS, and the set-up and hold times are referenced to CAS. If the data input is not available at CAS time or if it is desired that the cycle be a read-write or read-modify-write cycle, the WRITE signal must be delayed until after CAS. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of WRITE rather than to CAS. (To illustrate this feature, Data In is referenced to WRITE in the timing diagram depicting the read-modify-write cycle while the "early write" cycle diagram shows Data In referenced to CAS). Note that if the chip is unselected (CS high at CAS time) WRITE commands are not executed and, consequently, data stored in the memory is unaffected.

Data is retrieved from the memory in a read cycle by maintaining WRITE in the inactive or high state throughout the portion of the memory cyle in which CAS is active. Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT LATCH

Any change in the condition of the Data Out Latch is initiated by the CAS signal. The output buffer is not affected by memory (refresh) cycles in which only the RAS signal is applied to the MK 4096. Whenever CAS makes a negative transition, the output will go unconditionally open-circuited, independent of the state of any other input to the chip. If the cycle in progress is a read, read-modify-write, or a delayed write cycle and the chip is selected, then the output latch and buffer will again go active and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. If the cycle in progress is a write cycle (WRITE active low before CAS goes low) and the chip is selected, then at access time the output latch and buffer will contain a logic 1. Once having gone active, the output will remain valid until the MK 4096 receives the next CAS negative edge. Intervening refresh cycles in which a RAS is received (but no CAS) will not cause valid data to be affected. Conversely, the output will assume the open-circuit state during any cycle in which the MK 4096 receives a CAS but no RAS signal (regardless of the state of any other inputs). The output will also assume the open-circuit state in normal cycles (in which both RAS and CAS signals occur) if the chip is unselected.

The three-state data output buffer presents the data output pin with a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The effective resistance to V_{CC} (logic 1 state) is 500Ω maximum and 150Ω typically. The resistance to V_{SS} (logic 0 state) is 200Ω maximum and 100Ω typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may have power removed without affecting the MK 4096 refresh operation. This allows all system logic except the RAS/CAS timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses within each 1 millisecond time interval. Any cycle in which a $\overline{RAS}$ signal occurs accomplishes a refresh operation. A read cycle will refresh the selected row, regardless of the Chip Select ($\overline{CS}$) input. A write or read-modify-write cycle also refreshes the selected row, but the chip should be unselected to prevent writing data into the selected cell.

For standby operation, a "$\overline{RAS}$-only" cycle can be employed to refresh the MK 4096. However, if "$\overline{RAS}$-only" refresh cycles (where $\overline{RAS}$ is the only signal applied to the chip) are continued for extended periods, the output buffer may eventually lose proper data and go open-circuit. Prior to the first memory cycle following a period (beyond 2ms) of "$\overline{RAS}$-only" refresh, a memory cycle employing both $\overline{RAS}$ and $\overline{CAS}$ must be performed to precharge the internal circuitry. This "dummy cycle" allows the output buffer to regain activity and enables the device to perform a read or write cycle upon command.

POWER DISSIPATION/STANDBY MODE

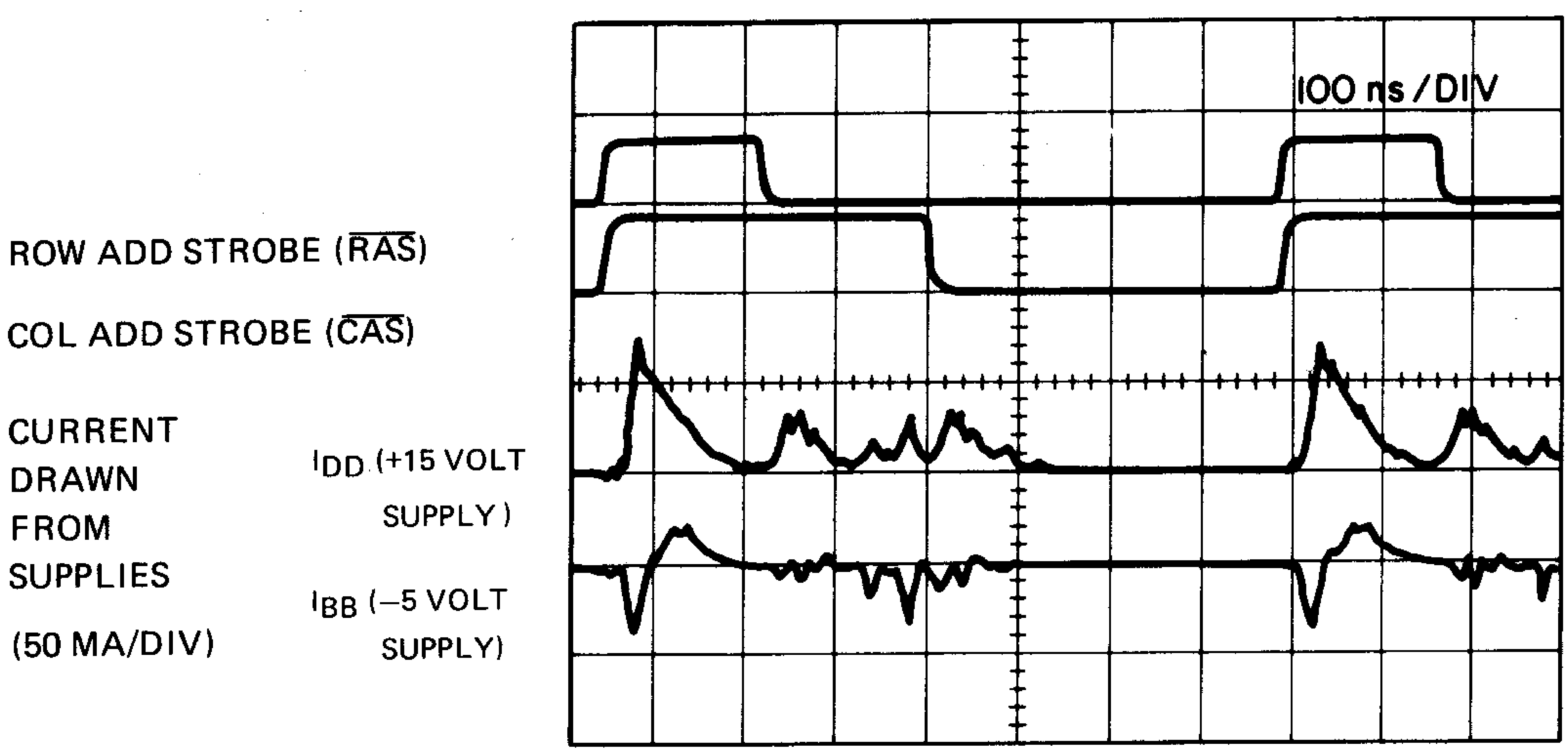
Most of the circuitry used in the MK 4096 is dynamic and most of the power drawn is the result of an address strobe edge. Because the power is not drawn during the whole time the strobe is active, the dynamic power is a function of operating frequency rather than active duty cycle. Typically, the power is 120 mW at a 1 μsec cycle rate for the MK 4096 with a maximum power of less than 550 mW at 500 nsec cycle time. To minimize the overall system power, the Row Address Strobe ($\overline{RAS}$) should be decoded and supplied to only the selected chips. The $\overline{CAS}$ must be supplied to all chips (to turn off the unselected output). Those chips that did not receive a $\overline{RAS}$, however, will not dissipate any power on the $\overline{CAS}$ edges, except for that required to turn off the outputs. If the $\overline{RAS}$ signal is decoded and supplied only to the selected chips, then the Chip Select ($\overline{CS}$) input of all chips can be at a logic 0. The chips that receive a $\overline{CAS}$ but no $\overline{RAS}$ will be unselected (output open-circuited) regardless of the Chip Select input. For refresh cycles, however, either the $\overline{CS}$ input of all chips must be high or the $\overline{CAS}$ input must be held high to prevent several "wire-ORed" outputs from turning on with opposing force.

The current waveforms for the current drawn from the V_{DD} and V_{BB} supplies are shown in Figure A. Since the current is pulsed, proper power distribution and bypassing techniques are required to maintain system power supply noise levels at an acceptable level. Low inductance supply lines for V_{DD} and V_{SS} are desirable. One 0.01 microfarad, low inductance, bypass capacitor per two MK 4096 devices and one 6.8 microfarad electrolytic capacitor per eight MK 4096 devices on each of the V_{DD} and V_{BB} supply lines is desirable.

POWER—UP

Under normal operating conditions the MK 4096 requires no particular power-up sequence. However, in order to achieve the most reliable performance from the MK 4096, proper consideration should be given to the V_{BB}/V_{DD} power supply relationship. The V_{BB} supply is an extremely important "protective voltage" since it performs two essential functions within the device. It establishes proper junction isolation and sets field-effect thresholds, both thin field and thick field. Misapplication of V_{BB} or device operation without the V_{BB} supply can affect long term device reliability. For optimum reliability performance from the MK 4096, it is suggested that measures be taken to not have V_{DD} (+15V) applied to the device for over five (5) seconds without the application of V_{BB} (−5V).

After power is applied to the device, the MK 4096 requires at least one memory cycle ($\overline{RAS}/\overline{CAS}$) before proper device operation is achieved. A normal 64 cycle refresh with both $\overline{RAS}$ and $\overline{CAS}$ is adequate for this purpose.



Power Supply Current Waveforms