

### 32Kx8 Static RAM CMOS, Monolithic

The EDI8832C is a high performance, low power 262,144bit CMOS Static RAM organized as 32Kx8.

It is available in standard (EDI8832C) and low power with data retention (EDI8832LP) versions.

Inputs and outputs are TTL compatible and allow for direct interfacing with common system bus structures.

The EDI8832LP offers battery back-up data retention capability at VDD equal to 2V and operates from a 5 volt supply.

Military product is compliant to MIL-STD-883, paragraph 1.2.1.

### Features

32Kx8 bit CMOS Static  
 Random Access Memory

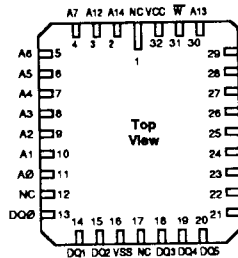
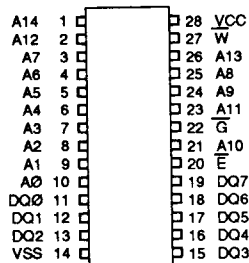
- Access Times 70, 85, 100, 120 and 150ns
- Data Retention Function (EDI8832LP only)
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks

Jedec Approved Pinouts

- 28 Pin Sidebraced DIP, 300 mils wide, No. 2
- 28 Pin Sidebraced DIP, 600 mils wide, No. 8
- 32 Pad Leadless Chip Carrier, No. 12

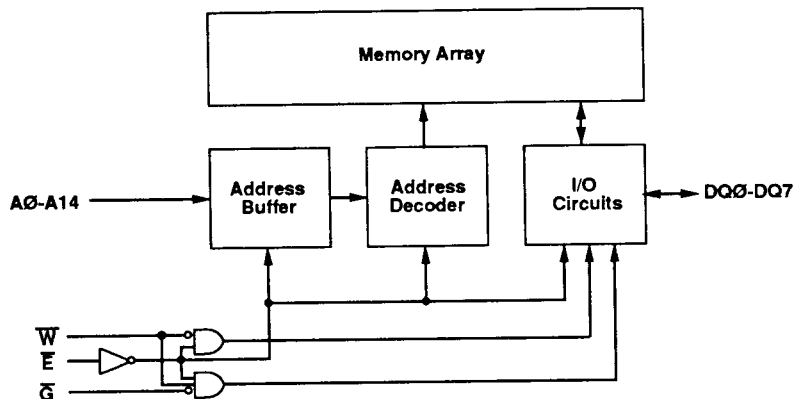
Single +5V (±10%) Supply Operation

### Pin Configurations and Block Diagram



### Pin Names

A0-A14	Address Inputs
E	Chip Enable
W	Write Enable
G	Output Enable
DQ0-DQ7	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection



## Absolute Maximum Ratings\*

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Voltage on any pin relative to VSS .....	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Industrial.....	-40°C to +85°C
Military.....	-55°C to +125°C
Storage Temperature .....	-65°C to +150°C
Power Dissipation .....	1 Watt
Output Current .....	20 mA
Junction Temperature, TJ .....	175°C

\*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

## AC Test Conditions

Input Pulse Levels .....	VSS to 3.0V
Input Rise and Fall Times .....	5ns
Input and Output Timing Levels .....	1.5V
Output Load: 70ns .....	1TTL, CL = 30pF
85/150ns .....	1TTL, CL = 100pF
(note: For TEHQZ, TGHQZ and TWLQZ, CL = 5pF)	

## DC Electrical Characteristics

Parameter	Sym	Conditions	Min	Typ*	Max	Units	
Operating Power Supply Current	ICC1	$\bar{E} = VIL, I/O = 0mA, \text{Min Cycle}$	--	45	80	mA	
Standby (TTL) Power Supply Current	ICC2	$\bar{E} \geq VIH, VIN \leq VIL \text{ or } \geq VIH$	--	0.5	2	mA	
Full Standby Power Supply Current	ICC3	$\bar{E} \geq VCC - 0.2V$ $VIN \geq VCC - 0.2V \text{ or } VIN \leq 0.2V$	C	--	100	850	$\mu A$
			LP	--	30	400	$\mu A$
Input Leakage Current	IIL	$VIN = 0V \text{ to } VCC$	--	--	$\pm 5$	$\mu A$	
Output Leakage Current	IOL	$V I/O = 0V \text{ to } VCC$	--	--	$\pm 5$	$\mu A$	
Output High Voltage	VOH	$IOH = -1.0mA$	2.4	--	--	V	
Output Low Voltage	VOL	$IOL = 2.1mA$	--	--	0.4	V	

\*Typical = TA = 25°C, VCC = 5.0V

## Truth Table

$\bar{G}$	$\bar{E}$	$\bar{W}$	Mode	Output	Power
X	H	X	Standby	High Z	ICC2, ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

## Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max			Unit
		LCC	FP	DIP	
Address Lines	CI	6	10	10	pF
Data Lines	CD/Q	8	12	12	pF

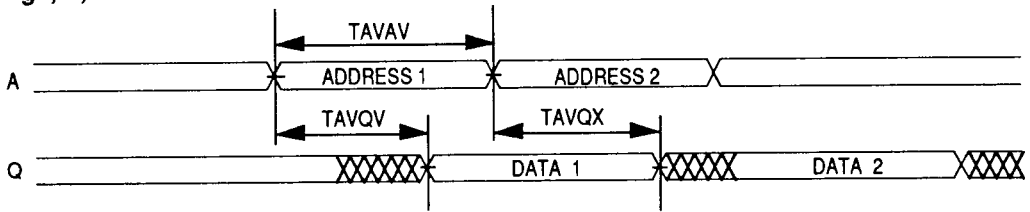
These parameters are sampled, not 100% tested.

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**AC Characteristics**  
**Read Cycle**

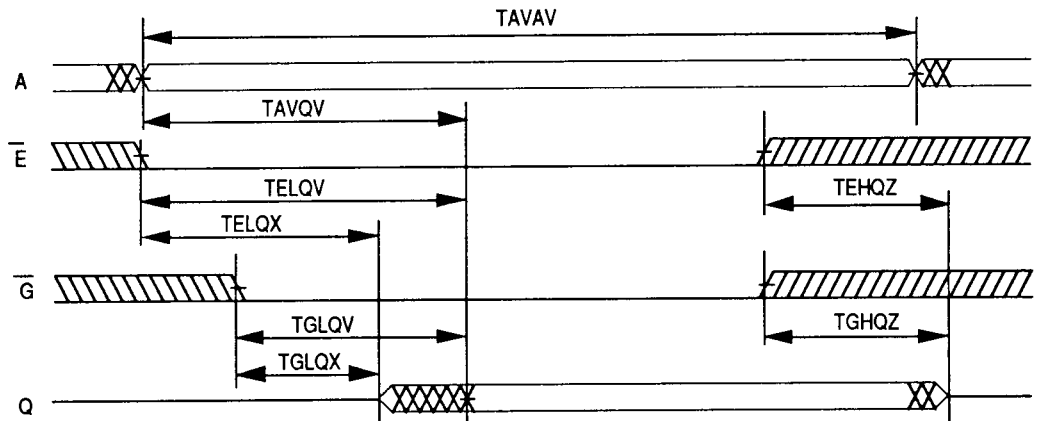
Parameter	Symbol		70ns		85ns		100ns		120ns		150ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	TRC	70		85		100		120		150		ns
Address Access Time	TAVQV	TAA		70		85		100		120		150	ns
Chip Enable Access Time	TELOV	TACS		70		85		100		120		150	ns
Chip Enable to Output Low Z (1)	TELOX	TCLZ	3		3		3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ	0	35	0	35	0	35	0	40	0	45	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		35		35		60		60		75	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		0		0		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ	0	35	0	35	0	35	0	40	0	45	ns

Note 1: Parameter guaranteed, but not tested.

**Read Cycle 1**  
**W High; G, E Low**



**Read Cycle 2**  
**W High**

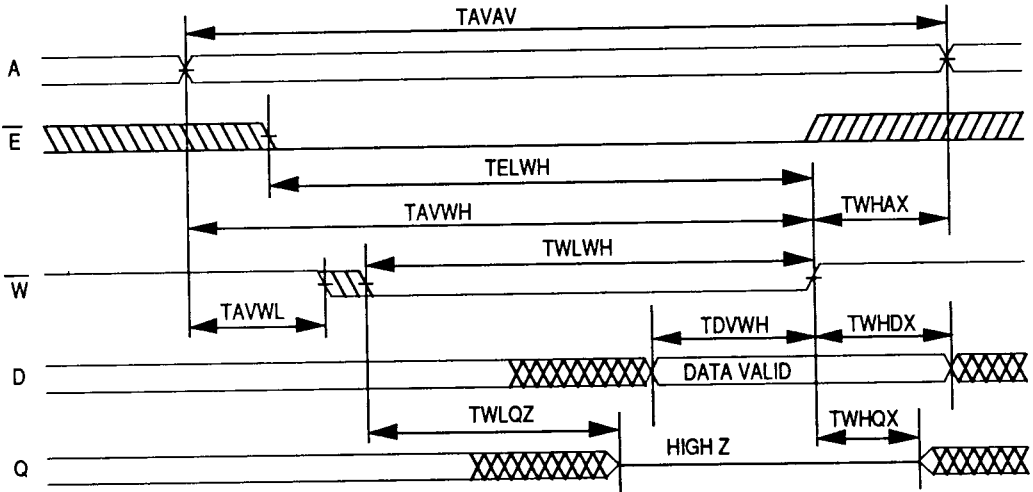


**AC Characteristics**  
**Write Cycle**

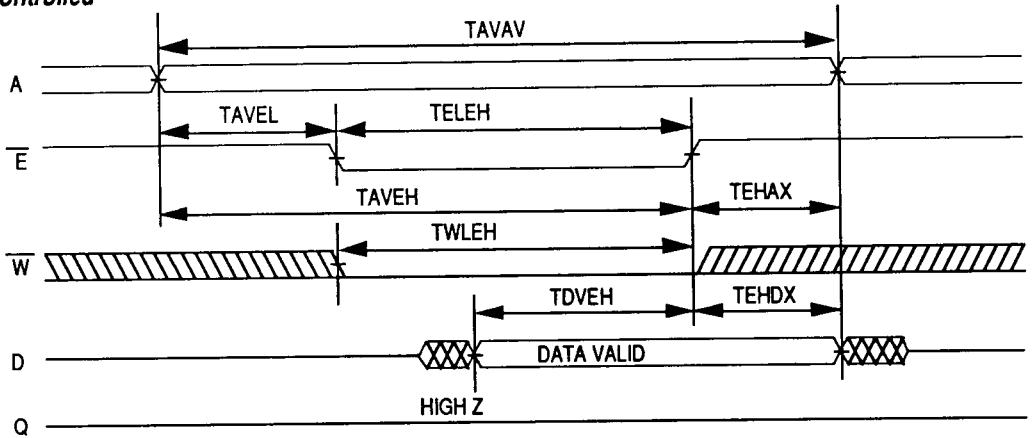
Parameter	Symbol		70ns		85ns		100ns		120ns		150ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV	TWC	70		85		100		120		150		ns
Chip Enable to End of Write	TELWH	TCW	60		70		80		85		90		ns
	TELEH	TCW	60		70		80		85		90		ns
Address Setup Time	TAVWL	TAS	0		0		0		0		0		ns
	TAVEL	TAS	0		0		0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	60		70		80		85		90		ns
	TAVEH	TAW	60		70		80		85		90		ns
Write Pulse Width	TWLWH	TWP	50		55		70		70		80		ns
	TWLEH	TWP	50		55		70		70		80		ns
Write Recovery Time	TWHAX	TWR	0		0		0		0		0		ns
	TEHAX	TWR	0		0		0		0		0		ns
Data Hold Time	TWHDX	TDH	3		3		3		3		3		ns
	TEHDX	TDH	3		3		3		3		3		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	40	0	45	0	50	0	50	0	50	ns
Data to Write Time	TDVWH	TDW	30		35		35		40		50		ns
	TDVEH	TDW	30		35		35		40		50		ns
Output Active from End of Write (1)	TWHQX	TWLZ	3		3		3		3		3		ns

Note 1: Parameter guaranteed, but not tested.

**Write Cycle 1**  
**W Controlled**



**Write Cycle 2**  
**E Controlled**



## Data Retention Characteristics

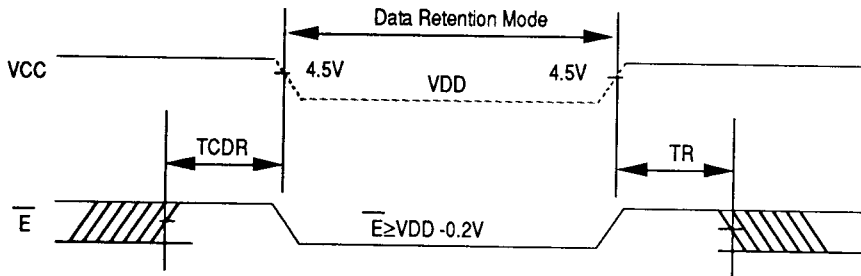
(TA = -55°C to +125°C)

LP Version Only

Characteristic	Sym	Test Conditions	Min	Typ	Max	Unit
Data Retention Voltage	VDD	VDD = 2.0V	2	--	--	V
Data Retention Quiescent Current	ICCDR	$\bar{E} \geq VDD - 0.2V$	--	10	150	$\mu A$
Chip Disable to Data Retention Time	TCDR	VIN $\geq$ VDD - 0.2V	0	--	--	ns
Operation Recovery Time	TR	or VIN $\leq$ 0.2V	TAVAV*	--	--	ns

\*Read Cycle Time

## Data Retention E Controlled



## Ordering Information

Part No.	Speed (ns)	Leads	Package Style	No.
EDI8832C70CB	70	28	0.6 DIP	8
EDI8832C85CB	85	28	0.6 DIP	8
EDI8832C100CB	100	28	0.6 DIP	8
EDI8832C120CB	120	28	0.6 DIP	8
EDI8832C150CB	150	28	0.6 DIP	8
EDI8832C70QB	70	28	0.3 DIP	2
EDI8832C85QB	85	28	0.3 DIP	2
EDI8832C100QB	100	28	0.3 DIP	2
EDI8832C120QB	120	28	0.3 DIP	2
EDI8832C150QB	150	28	0.3 DIP	2
EDI8832C70LB	70	32	LCC	12
EDI8832C85LB	85	32	LCC	12
EDI8832C100LB	100	32	LCC	12
EDI8832C120LB	120	32	LCC	12
EDI8832C150LB	150	32	LCC	12

Low Power with Data Retention	Speed (ns)	Leads	Package Style	No.
EDI8832LP70CB	70	28	0.6 DIP	8
EDI8832LP85CB	85	28	0.6 DIP	8
EDI8832LP100CB	100	28	0.6 DIP	8
EDI8832LP120CB	120	28	0.6 DIP	8
EDI8832LP150CB	150	28	0.6 DIP	8
EDI8832LP70QB	70	28	0.3 DIP	2
EDI8832LP85QB	85	28	0.3 DIP	2
EDI8832LP100QB	100	28	0.3 DIP	2
EDI8832LP120QB	120	28	0.3 DIP	2
EDI8832LP150QB	150	28	0.3 DIP	2
EDI8832LP70LB	70	32	LCC	12
EDI8832LP85LB	85	32	LCC	12
EDI8832LP100LB	100	32	LCC	12
EDI8832LP120LB	120	32	LCC	12
EDI8832LP150LB	150	32	LCC	12