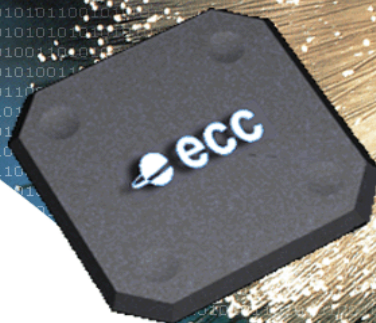




# **ECC3100EP - ECC3100 SkyPHY Receiver Evaluation Board Data Sheet**

**Version 1.0**





## Revision History

Revision Number	Date	Company	Comments
1.0	5/22/06	Efficient Channel Coding, Inc.	Initial Release

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## 1 Overview

The ECC3100 evaluation board design provides a platform for evaluation and demonstration of the ECC3100 SkyPHY Receiver ASIC in a DVB-S2 forward link receiver sub-system.

The evaluation board provides three analog signal inputs:

- 75 $\Omega$  RF input to Analog Devices AD8347 Direct Conversion Quadrature Demodulator
- 75 $\Omega$  RF input to Zarlink ZL10038 Advanced Modulation Satellite Tuner
- Baseband I & Q analog inputs (direct input to ADCs)

The evaluation board provides four digital data outputs:

- MPEG-2 TS Synchronous Parallel Interface (SPI)
- ASI serial output based on a Cypress Hotlink II transceiver
- Serial BERT clock and data output
- NEC processor local bus

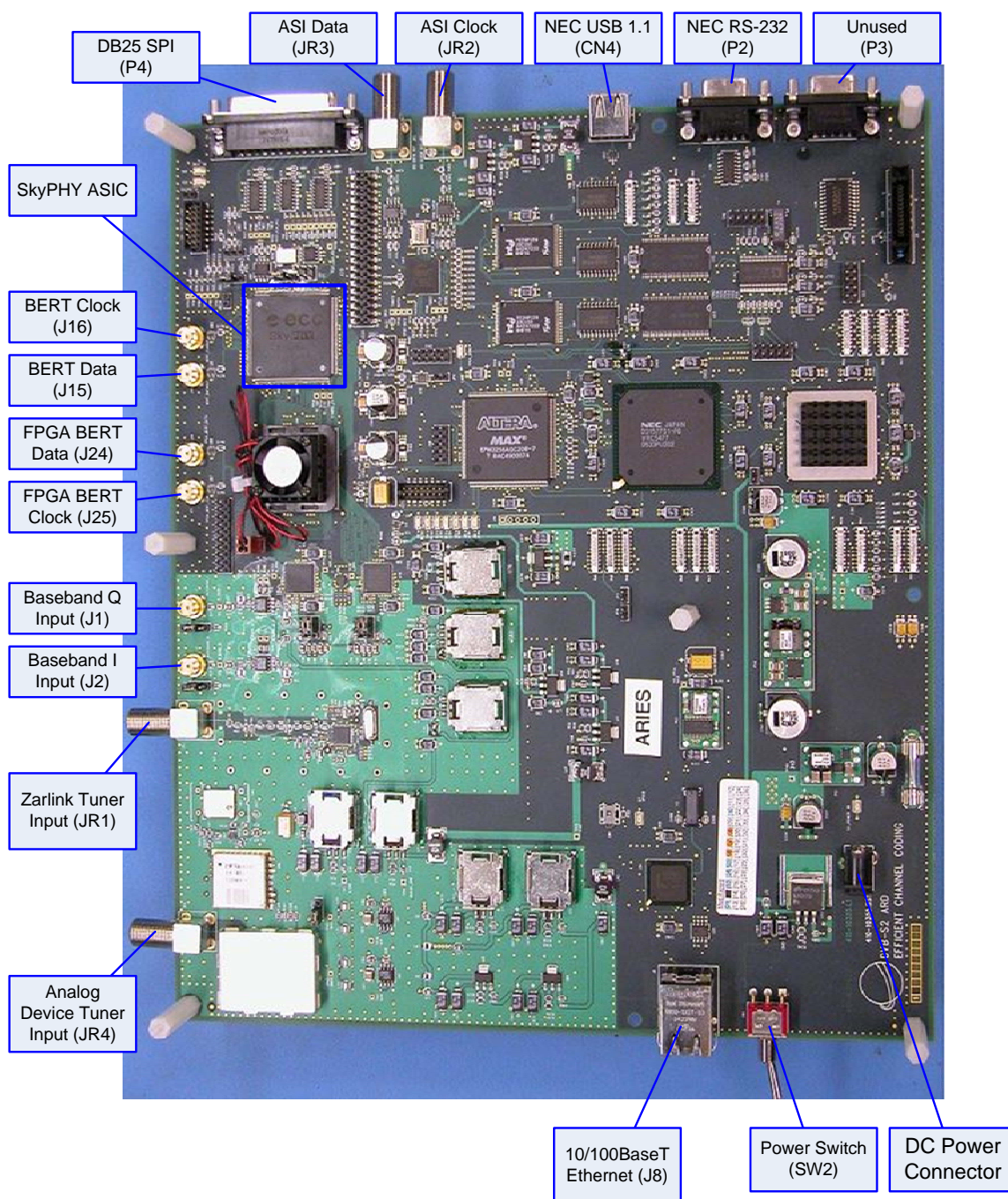
This platform processor is the NEC VR5500 with VRC5477 companion chip. The processor is supported with 32MB of SDRAM, 32MB of FLASH memory and interfaces to Ethernet, USB & RS232 Serial ports.

The processor is running an ASIC device driver that provides for the initial configuration of the ASIC, periodic ASIC maintenance, and tuning of the Analog Devices demodulator.

The processor is also running an embedded Java applet that provides the user with a GUI for ASIC configuration and status monitoring. The GUI can be accessed by connecting the evaluation board to your local area network and pointing a web browser to the IP address of the board.

The evaluation platform contains a single FPGA which is currently used to translate the 1.8V signal voltage level out of the ADCs to 3.3V for the ASIC. Future releases of the FPGA image will allow for on-board testing of the ASIC's demodulator bypass mode.

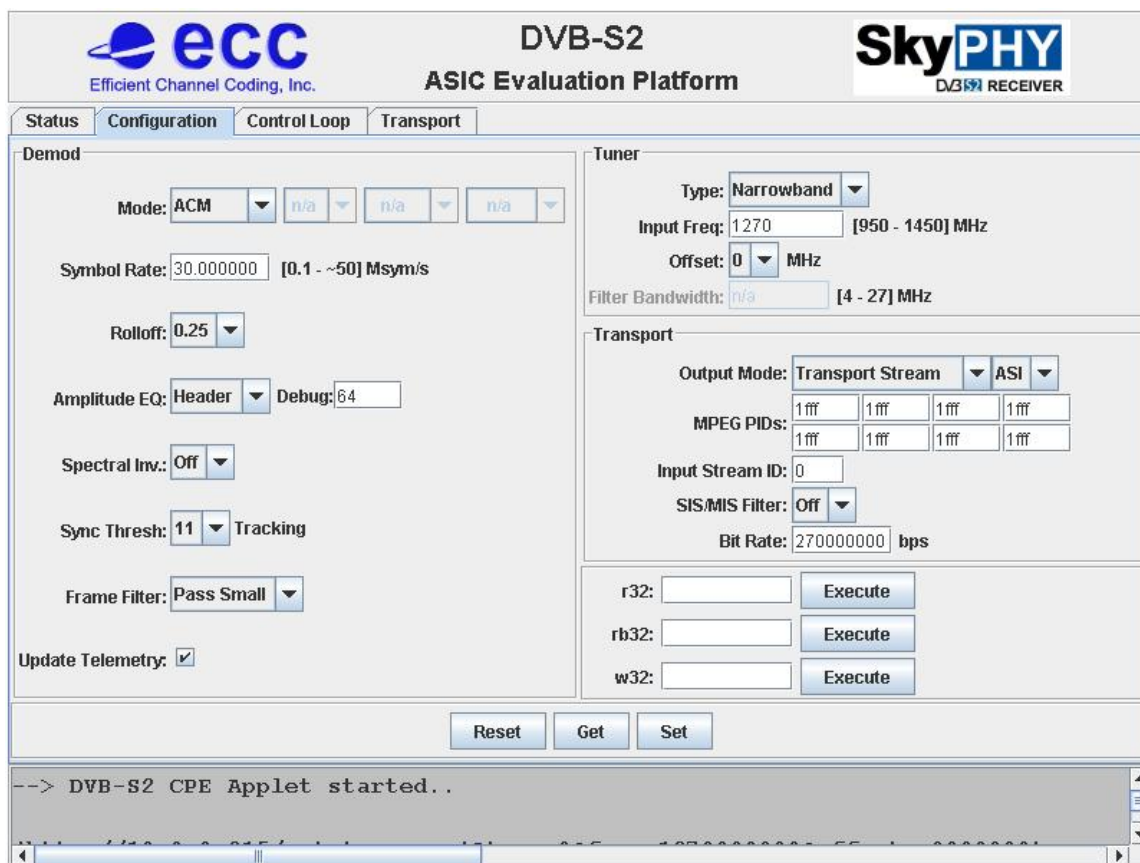
The picture on the following page shows the evaluation board and its various inputs and outputs.



*The evaluation board is designed for use in a lab environment. Care should be taken to ensure antistatic precautions are taken when handling the board. Electrostatic shock, excessive heat and moisture may cause damage to the board and attached components.*

## 2 Configuration Tab

The figure below shows the GUI Configuration tab. This tab displays panes for configuration of the evaluation platform.



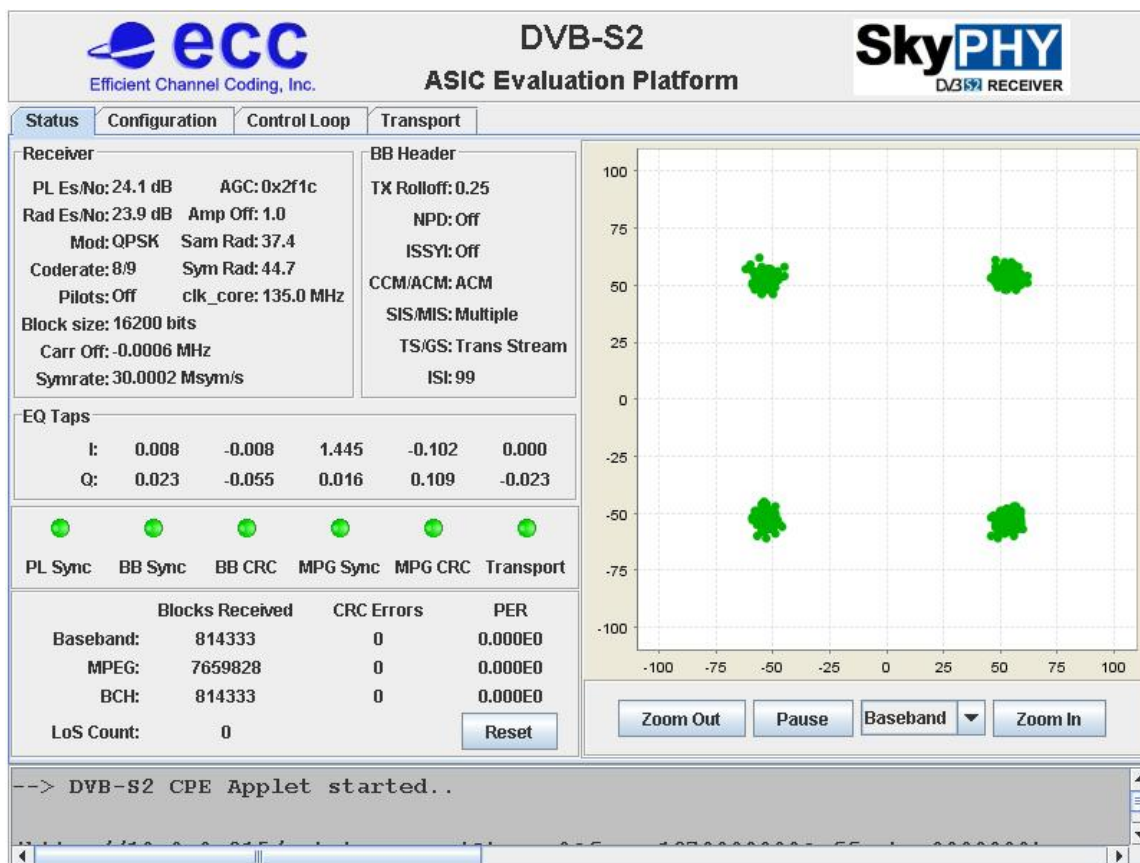
The screenshot shows the 'Configuration' tab of the DVB-S2 ASIC Evaluation Platform GUI. The interface is divided into several sections:

- Demod Section:**
  - Mode: ACM (dropdown), n/a (dropdown), n/a (dropdown), n/a (dropdown)
  - Symbol Rate: 30.000000 [0.1 - ~50] Msym/s
  - Rolloff: 0.25 (dropdown)
  - Amplitude EQ: Header (dropdown), Debug: 64
  - Spectral Inv.: Off (dropdown)
  - Sync Thresh: 11 (dropdown) Tracking
  - Frame Filter: Pass Small (dropdown)
  - Update Telemetry: ☒
- Tuner Section:**
  - Type: Narrowband (dropdown)
  - Input Freq: 1270 [950 - 1450] MHz
  - Offset: 0 MHz
  - Filter Bandwidth: n/a [4 - 27] MHz
- Transport Section:**
  - Output Mode: Transport Stream (dropdown), ASI (dropdown)
  - MPEG PIDs: 1fff, 1fff, 1fff, 1fff
  - Input Stream ID: 0
  - SIS/MIS Filter: Off (dropdown)
  - Bit Rate: 270000000 bps
- Buttons:**
  - Reset, Get, Set
  - Execute buttons for r32, rb32, and w32 registers.
- Log Console:**
  - Log output: --> DVB-S2 CPE Applet started..



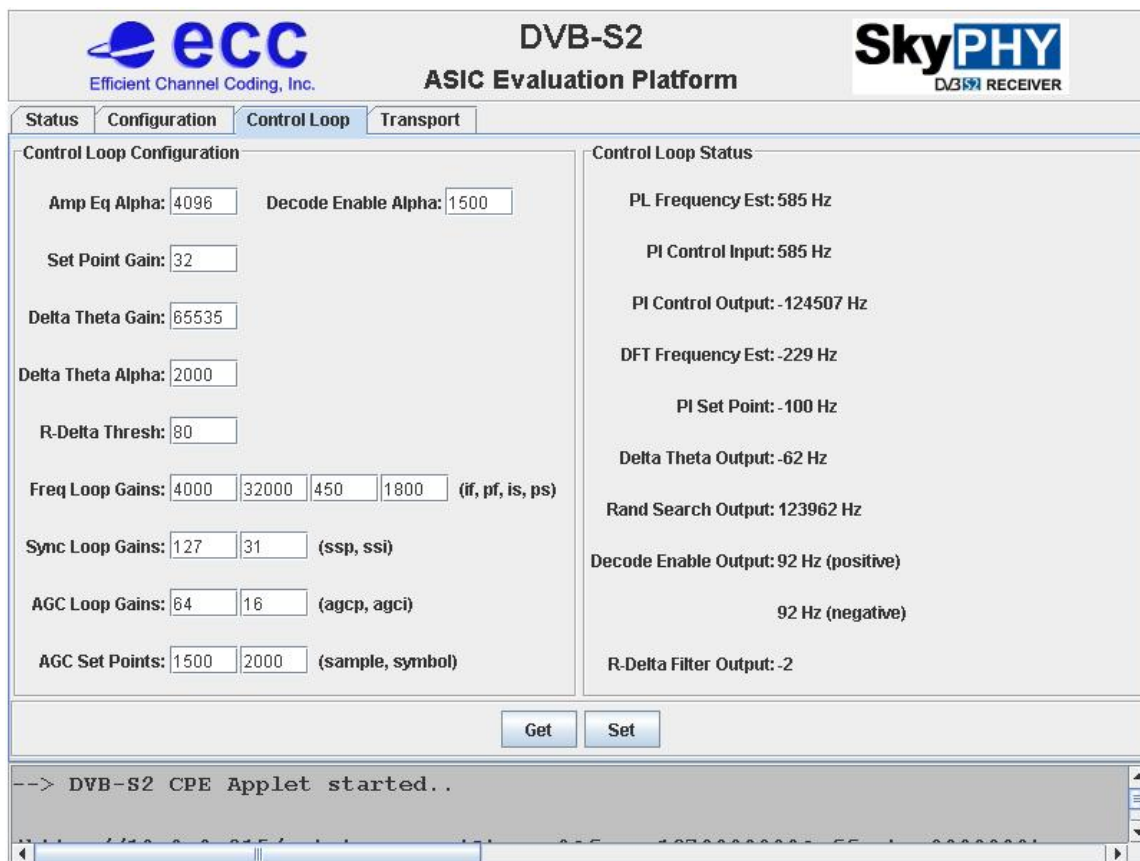
### 3 Status Tab

The Status Tab displays demodulator and transport telemetry information, a constellation plot, and status of blocks being received.



## 4 Control Loop Tab

The control loop tab displays the current status of several demodulator control loops and allows the user to modify some of the demodulator control loop parameters.



The screenshot shows the 'Control Loop' tab of the 'DVB-S2 ASIC Evaluation Platform' software. The interface is divided into two main sections: 'Control Loop Configuration' on the left and 'Control Loop Status' on the right. Below these sections are 'Get' and 'Set' buttons, and a command window at the bottom.

**Control Loop Configuration:**

- Amp Eq Alpha: 4096
- Decode Enable Alpha: 1500
- Set Point Gain: 32
- Delta Theta Gain: 65535
- Delta Theta Alpha: 2000
- R-Delta Thresh: 80
- Freq Loop Gains: 4000, 32000, 450, 1800 (if, pf, is, ps)
- Sync Loop Gains: 127, 31 (ssp, ssi)
- AGC Loop Gains: 64, 16 (agcp, agci)
- AGC Set Points: 1500, 2000 (sample, symbol)

**Control Loop Status:**

- PL Frequency Est: 585 Hz
- PI Control Input: 585 Hz
- PI Control Output: -124507 Hz
- DFT Frequency Est: -229 Hz
- PI Set Point: -100 Hz
- Delta Theta Output: -62 Hz
- Rand Search Output: 123962 Hz
- Decode Enable Output: 92 Hz (positive)  
92 Hz (negative)
- R-Delta Filter Output: -2

**Command Window:**

```
--> DVB-S2 CPE Applet started..
```






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## ECC3100 Evaluation Board Data Sheet



## 5 Transport Tab


The transport tab displays the packet processing statistics for all modulation and code pairs. The table does not distinguish between normal and small frames or between pilot on and pilot off modes. The last row of the table shows the sum of the statistics in each column.



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DVB-S2

ASIC Evaluation Platform



DVB-S2 RECEIVER

Status	Configuration	Control Loop		Transport							
Mode	Code	BB Recv'd	BB CRC	BCH CRC	MPEG	MPEG CRC	BB PER	BCH PER	MPG PER	Corrected	Iterations
QPSK	1/4	0	0	0	0	0				0	0
QPSK	1/3	0	0	0	0	0				0	0
QPSK	2/5	0	0	0	0	0				0	0
QPSK	1/2	0	0	0	0	0				0	0
QPSK	3/5	0	0	0	0	0				0	0
QPSK	2/3	0	0	0	0	0				0	0
QPSK	3/4	0	0	0	0	0				0	0
QPSK	4/5	0	0	0	0	0				0	0
QPSK	5/6	0	0	0	0	0				0	0
QPSK	8/9	1874439	0	0	17631451	0	0.000E0	0.000E0	0.000E0	0	1
QPSK	9/10	0	0	0	0	0				0	0
8PSK	3/5	0	0	0	0	0				0	0
8PSK	2/3	0	0	0	0	0				0	0
8PSK	3/4	0	0	0	0	0				0	0
8PSK	5/6	0	0	0	0	0				0	0
8PSK	8/9	0	0	0	0	0				0	0
8PSK	9/10	0	0	0	0	0				0	0
16APSK	2/3	0	0	0	0	0				0	0
16APSK	3/4	0	0	0	0	0				0	0
16APSK	4/5	0	0	0	0	0				0	0
16APSK	5/6	0	0	0	0	0				0	0
16APSK	8/9	0	0	0	0	0				0	0
16APSK	9/10	0	0	0	0	0				0	0
Sum		1874439	0	0	17631451	0	0.000E0	0.000E0	0.000E0	0	1

PL Es/No: 24.1 dB

Reset

--> DVB-S2 CPE Applet started..