NEC

NEC Electronics Inc.

Preliminary

CB-C7, 3-VOLT 0.8-MICRON CELL-BASED CMOS ASIC

October 1993

Description

The CB-C7, 3-volt cell-based product family is intended for low power portables and battery-operated products. A power reduction of up to 60 percent is now possible compared with the CB-C7, 5-volt. The CB-C7, 3-volt is manufactured with a 0.8-micron (drawn) process with two- or three-layer metalization and is offered in 22 I/O ring sizes. Typical applications include handheld terminals, personal digital office assistants, word spellers, cellular phones and a variety of high-volume, portable PC-based applications. The family allows designing complex logic functions, up to 237,000 usable gates of user-defined logic. Megamacro blocks may include industry-standard CPU cores, peripherals, and analog functions — thus enabling complete system-on-a-chip solutions.

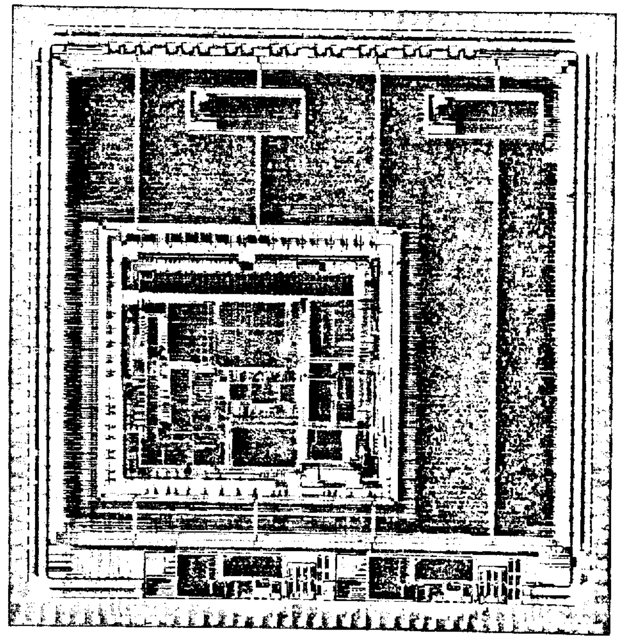
The CB-C7 series consists of two types of architectures, a Fast Turn FT-type embedded array and a High Density HD-type full standard cell. The FT-type uses fully-diffused standard cell embedded cores with sea-of-gates user-definable logic. The FT solution offers gate-array-like turn-around times while allowing the incorporation of large embedded functions. Another important advantage is that the FT-type is well-suited for multiple designs built around a common embedded CPU function, such as the V30HL (8086) CPU.

The HD-type is comprised of fully-diffused standard cell architecture for both the embedded cores and the user-defined logic area. This solution offers an optimal die size for economic cost-effective volume production. Full gate delay models are available for both in Verilog®, a golden simulator, as part of NEC's OpenCAD® Design System.

Features

- ❑ Low voltage cell-based library means power savings of up to 60% over 5V solutions
- ❑ 1.6 µW/gate per MHz power dissipation at 3 V
- ❑ Standby current I_{DDQ} < 150 nA
- ❑ Advanced 0.8 µ drawn gate (0.6 µ L_{eff}) length CMOS technology with three-layer metalizations
- ❑ Up to 237,000 usable gates on 3-layer HD full standard cell product with 440 I/Os and a pad pitch of 124 µm
- ❑ Extensive embedded core library includes CPU, analog, and video DAC functions
- ❑ Datapath compiler available for multipliers, FIFOs, and register files
- ❑ Supports leading third-party design tools

Figure 1. Integrated HDD Solution with CB-C7 Cell-Based ASIC and Embedded Megafunctions



Digital Megamacros in Library

Compatible Device	NEC Code	Description
8088	V20HL (NA70108H)	8-bit CPU
8086	V30HL (NA70116H)	16-bit CPU
Z80	NA70008A	Z80™ 8-bit CPU
80C42	NA80C42H	Keyboard Controller
8237A	NA71037	Programmable DMA Controller
8251A	NA71051	Serial Communications Controller
8254	NA71054	Interval Timer
8255A	NA71055	Peripheral Interface
8259A	NA71059	Interrupt Controller
4991A	NA4991A	Real Time Clock
72020	NA72020	Graphics Display Controller

Analog Megamacros in Library

NEC Code	Description
XXXA	135 MHz triple 8-bit video DAC
AADA8GPC	8-bit general-purpose DAC
AACP25NA	High-speed (25ns) comparator
AACP80NA	High-speed (80ns) comparator
AACP01UA	General-purpose comparator
AAOP10MA	High-speed operational amplifier
AAOP01MA	General-purpose operative amplifier
AASWGPCA	Analog switch with control
AASWGPTA	Analog switch with control

Note: Some analog functions are currently in development

OpenCAD Design System

CB-C7 is supported by the OpenCAD Design System, an ASIC design environment that merges the best of today's most powerful CAD ASIC software design tools and proprietary tools, such as a floorplanner and module compilers, into a single environment.

Sample design kits are available at no charge to qualified users: contact the NEC ASIC Design Center nearest you for more information. A software license agreement is required.

Digital Megafunctions

In addition to the V30HL/V20HL 8086, 8088 product families and support peripherals, NEC offers complex standard IC functions as well as A/D and D/A converters for multimedia applications. Compiled RAM and ROM are also available to satisfy a myriad of different product applications.

Analog Blocks

NEC is building upon its expertise in analog standard ICs by now offering select members of its analog family as analog megamacros. These megamacros are layed out in the I/O area to maximize die area in the core for digital functions and user-defined logic. This separation of the analog and digital functions and separate analog V_{DD} and V_{SS} line also contributes to better noise isolation.

Digital and analog functions on a CB-C7 cell-based array are tested separately.

Test and Emulation Bus Architecture

The test and emulation bus architecture used for CB-C7 design methodology approach to the testing and emulation of embedded functions. It allows the emulation of the production chip for system validation, reuse of the test bus circuit and use of standard micro IC functional test vectors and system vectors in a modularized fashion. It also provides real-time emulation support and its test bus structure allows testing of on-chip RAM/ROM or analog blocks.

On-Chip Compiled Memory

RAM and ROM blocks can be custom compiled in the CB-C7 design environment.

The RAM and ROM compiler allows ASIC designers to generate silicon-efficient memory blocks of specific size and performance to suit exact system requirements quickly and efficiently.

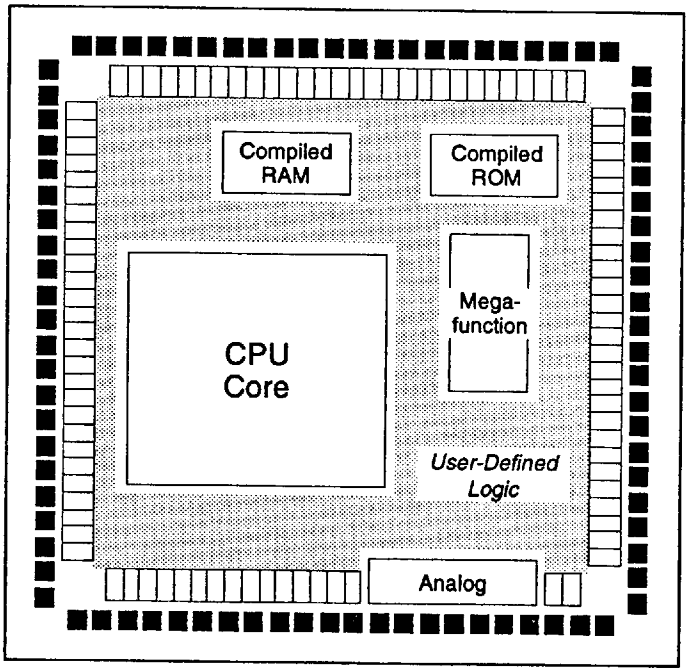
The table of compilable RAM and ROM, shown on page 4, describes three different MUX ratios along with the minimum and maximum size. For the 16:1 MUX, the minimum word depth is 256 and the minimum bit width is 1. The word depth can increase by 64 words in increments up to 2K and the bit width can increase by 1 bit up to a maximum of 8 bits. The other RAM and ROM configurations are determined in the same fashion.

Typical examples of applications containing digital memory and analog cores and their step size is shown in Figure 2.

3 V Operation

CB-C7 CMOS is ideal for low power, high volume, battery-operated products. The CB-C7 process has been recharacterized to operate at two voltage levels, 5 V ± 10% and 3.0 V ± 10%. Not only have macrocells been recharacterized to operate at the lower voltage, but complex megamacros and compiled memory as well.

Figure 2. Typical Application Example (See Table 2)



Trademarks

®OpenCAD is a registered trademark of NEC Electronics ™Z80 is a trademark of Zilog, Inc.
®Verilog is a registered trademark of Cadence Design System, Inc.
™MACRObus is a trademark of NEC Electronics Inc.

Table 1. CB-C7 Step Sizes and Usable Gate Count

No.	Step Size	I/O[1]	Total Raw Grids	HD-Type Usable Gates[2]		FT-Type Usable Gates[2]	
				2-Layer Metal	3-Layer Metal	2-Layer Metal	3-Layer Metal
1	B18	88	35,400	5,930	7,040	3,140	3,860
2	B57	104	49,600	8,840	10,430	4,720	5,760
3	B97	120	66,600	12,390	14,560	6,660	8,070
4	C37	136	86,000	16,530	19,370	8,910	10,760
5	C76	152	107,700	21,150	24,740	11,440	13,780
6	D16	168	131,800	26,460	30,900	14,340	17,230
7	D55	184	158,300	32,230	37,590	17,490	20,990
8	D75	192	172,500	35,390	41,260	19,230	23,050
9	E15	208	202,700	42,160	49,100	22,930	27,450
10	E54	224	235,800	49,360	57,440	26,870	32,140
11	E94	240	270,800	57,290	66,630	31,220	37,300
12	F34	256	307,800	65,810	76,500	35,890	42,850
13	F74	272	348,300	74,730	86,820	40,780	48,660
14	G14	288	390,700	84,410	98,030	46,100	54,970
15	G53	304	435,500	94,480	109,680	51,620	61,520
16	G93	320	482,100	105,330	122,240	57,580	68,590
17	H33	336	531,700	116,770	135,470	63,860	76,040
18	H72	352	583,800	128,550	149,100	70,330	83,710
19	J32	376	662,900	147,680	171,230	80,830	96,170
20	J71	392	720,900	160,890	186,510	88,090	104,770
21	K11	408	781,300	174,960	202,780	95,820	113,930
22	K90	440	907,800	204,550	236,990	112,070	133,200

Notes: 1. I/O may be configured as VDD/GND
2. Usable gates: equivalent estimated 2-input NAND, will vary depedning ons pecific design
   a. 2-layer metal FT = 55% utilization for routing HD = 65% utilization for routing
   b. 3-layer metal FT = 65% utilization for routing HD = 75% utilization for routing
   c. Grid/gate ratio* FT = 4.3 grid/gate ratio HD = 2.8
   d. Grid to gate ratio based on conversion from other libraries will be different. Contact NEC Design Center for die size estimation
   * Based on CMOS-6 L302 cell equivalents

Table 2. Examples of Core Use (Refer to Figure 2)

Application	Core	UDL*	I/O	Step Size	Metalization	Package
Cellular Phone	Z80	40,000	102	E94	3LM	120 TQFP
Wireless or GPS	V20HL	10,000	88	D55	3LM	100 TQFP
Hard Disk Drive	V20HL 71054 71059	3,000	80	D55	2LM	100 TQFP
Graphics Controller	Triple Video DAC HS RAM 256 W x 8 bits x 3	40,000	182	E94	3LM	208 PQFP
Document Scanner	ROM 256 W x 16 bits RAM 64W x 8 bits x 5	3,000	88	C37	2LM	100 QFP

* UDL = User-Defined Logic; measured in 2-input NAND gate equivalents of CMOS-6 family

Table 3. Compilable RAM, ROM and Datapath Elements for CB-C7

Compiled SRAM

- Single port, asynchronous operation

	Min Size	Max Size	Increment
16:1 Column MUX	256 x 1	2K x 8	64 words, 1 bit
8:1 Column MUX	128 x 1	1K x 16	32 words, 1 bit
4:1 Column MUX	64 x 1	512 x 32	16 words, 1 bit

Compiled High-Speed SRAM

- Single port, asynchronous high speed operation
- Speed: 12.6ns (typ) (512W x 8 bit)

	Min Size	Max Size	Increment
8:1 Column MUX	16 x 1	2K x 20	16 words, 1 bit

Example: For a 8:1 column MUX minimum size is 16 x 1. Increments can thus be 16, 32, 48 words up to 2K max. Bit size can be a mimimum of 1 bit, one bit at time increments to 20 bits max.

Compiled Dual Port RAM

- Dual port, asynchronous operation
- Speed: 43ns (typ) (512W x 8 bit)

	Min Size	Max Size	Increment
8:1 Column MUX	16 x 1	2K x 32	16 words, 1 bit

Compiled ROM

- Single port, asynchronous operation
- Speed: 63ns (typ) (512W x 8 bit)

	Min Size	Max Size	Increment
32:1 Column MUX	512 x 1	32K x 16	512 words, 1 bit
16:1 Column MUX	256 x 2	16K x 32	256 words, 1 bit
8:1 Column MUX	128 x 4	8K x 64	128 words, 2 bits

Datapath Modules

	Min Size	Max Size	Increment
Multiplier	6 x 6	32 x 32	2 bits
Register File	8 x 2	256 x 32	4 words, 1 bit
FIFO	8 x 2	256 x 32	2 words, 1 bit

* Please check with the Design Center for exact specifications and availability.

Examples for Compiled High-Speed SRAM: For a 8:1 column MUX, minimum size is 16 x 1. Increments can thus be 16, 32, 48, words up to 2K max. Bit size can be minimum of 1 bit, one bit at a time in increments to 20 bits max.

Absolute Maximum Ratings

Power supply voltage, V_{DD}	–0.5 to +6.5 V
Input/output voltage, V_I / V_O	–0.5 V to V_{DD} + 0.5 V
Output current, I_O	
I_{OL} (min) = 2.2 mA (typ)	8 mA
I_{OL} (min) = 4.4 mA (typ)	16 mA
I_{OL} (min) = 6.6 mA (typ)	24 mA
Operating temperature, T_{OPT}	–40 to +85°C
Storage temperature, T_{STG}	–65 to +150°C

Caution: Exposure to absolute maximum ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should not be operated outside the recommended operating conditions.

Input/Output Capacitance

$V_{DD} = V_I = 0$ V; f = 1 MHz

Terminal	Symbol	Typ	Max	Unit
Input	C_{IN}	10	20	pF
Output	C_{OUT}	10	20	pF
I/O	$C_{I/O}$	10	20	pF

Note:

(1) Values include package pin capacitance.

Power Consumption

Description	Limits (max)	Unit	Test Conditions
Internal cell (L302)	1.6	µW/MHz	F/O = 2; L = 2 mm

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Power supply voltage	V_{DD}	2.7	3.3	V
Ambient temperature	T_A	– 40	+85	°C
Input voltage	V_I	0	V_{DD}	V
High-level input voltage	V_{IH}	0.7 V_{DD}	V_{DD}	V
Low-level input voltage	V_{IL}	0.3 V_{DD}	V_{DD}	V
Input rise or fall time (normal input)	t_{RI}, t_{FI}	0	200	ns
Input rise or fall time (Schmitt-trigger input)	t_{RI}, t_{FI}	0	10	ms
Positive Schmitt-trigger voltage	V_P	1.8	4.0	V
Negative Schmitt-trigger voltage	V_N	0.6	3.1	V
Hysteresis voltage	V_H	0.3	1.5	V

Note: The rise/fall time given for a Schmitt-trigger input buffer varies depending on the operating environment. Simultaneous switching of output buffers should be analyzed before deciding to use a Schmitt-trigger input buffer.

AC Characteristics

V_{DD} = 3 V ± 10%; T_A = –40 to +85°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Internal toggle frequency	f_{TOG}	52			MHz	D-F/F; F/O = 2
Delay time, 2-input NAND Gate*						
Standard gate (F302) HD-type	t_{PD}		520 (HL)		ps	F/O = 1; L = 2 mm
Standard gate (F302) HD-type	t_{PD}		870 (HL)		ps	F/O = 2; L = 1 mm
Low power gate (L302) HD-type	t_{PD}		680 (HL)		ps	F/O = 1; L = 0 mm
Low power gate (L302) HD-type	t_{PD}		1310 (HL)		ps	F/O = 2; L = 1 mm
Delay time, Buffer						
Input buffer (FI01)	t_{PD}		760		ps	F/O = 2; L = 2 mm
Output buffer (FO01)	t_{PD}		4800		ps	C_L = 15 pF, IOL = 4mA
Rise and Fall Times						
Output rise time (FO01)	t_R		TBD		ps	C_L = 15 pF, IOL = 2.2 mA
Input fall time (FO01)	t_F		TBD		ps	C_L = 15 pF, IOH = -2mA

* With L101 as load

DC Characteristics

V_{DD} = 3 V ± 10%; T_A = −40 to +85°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Static current (Note 1)	I_L		TBD	TBD	µA	$V_I = V_{DD}$ or GND
Input leakage current						
Normal input	I_I		$\pm 10^{-5}$	±8	µA	$V_I = V_{DD}$ or GND
100 kΩ pull-up	I_I	-10	-30	-90	µA	V_I = GND
12 kΩ pull-up	I_I	-0.08	-0.25	-0.75	mA	V_I = GND
100 kΩ pull-down	I_I	10	30	90	µA	$V_I = V_{DD}$
Off-state output leakage current						
Normal Input	I_{OZ}		$\pm 10^{-5}$	± 8	µA	$V_O = V_{DD}$ or GND
100K pull-up	I_{OZ}	-10	-30	-90	µA	V_I = GND
12K pull-up	I_{OZ}	-0.08	-0.25	-0.75	mA	V_I = GND
100K pull-down	I_{OZ}	10	30	90	µA	$V_I = V_{DD}$
Low-level output voltage (CMOS)						
	V_{OL}			0.4	V	I_{OL} = 2.2mA
	V_{OL}			0.4	V	I_{OL} = 4.4 mA
	V_{OL}			0.4	V	I_{OL} = 6.6 mA
High-level output voltage	V_{OH}	V_{DD} −0.4			V	I_{OH} = −1.1mA
	V_{OH}	V_{DD} −0.4			V	I_{OH} = −2.2mA
	V_{OH}	V_{DD} −0.4			V	I_{OH} = −3.3mA

Notes:

(1) The maximum value reflects the use of pull-up/pull-down resistors and oscillator blocks. Contact an NEC ASIC Design Center for assistance in calculation.

Table 4. Package Options

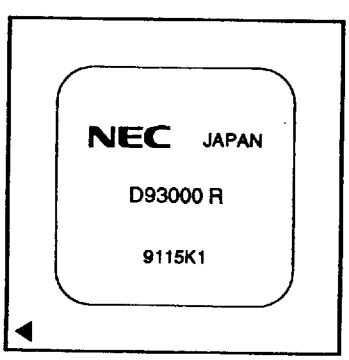
Pad Ring Step Sizes	B18	B57	B97	C37	C76	D16	D55	D75	E15	E54	E94
Package Type											
Plastic Quad Flatpack (QFP)											
44-pin (0.8 mm lead pitch)	A	A	A	A	A	A	–	–	–	–	–
52-pin (1 mm lead pitch)	A	A	A	A	A	A	A	–	–	–	–
64-pin (1 mm lead pitch)	A	A	A	A	A	A	A	A	A	A	A
80-pin (0.8 mm lead pitch)	A	A	A	A	A	A	A	A	A	A	A
100-pin (0.65 mm lead pitch)	–	A	A	A	A	A	A	A	A	A	A
120-pin (0.8 mm lead pitch)	–	–	A	A	A	A	A	A	A	A	A
136-pin (0.65 mm lead pitch)	–	–	A	A	A	A	A	A	A	A	A
160-pin (0.65 mm lead pitch)	–	–	–	–	–	A	A	A	A	A	A
160[1]-pin (0.65 mm lead pitch)	–	–	–	–	–	–	–	A	A	A	A
160[2]-pin (0.65 mm lead pitch)	–	–	–	–	–	–	–	A	A	A	A
Plastic Quad Flatpack (QFP-FP)											
100-pin (0.5 mm lead pitch)	–	A	A	A	A	A	A	A	A	A	A
120-pin (0.5 mm lead pitch)	–	–	A	A	A	A	A	A	A	A	A
144-pin (0.5 mm lead pitch)	–	–	–	A	A	A	A	A	A	A	A
160-pin (0.5 mm lead pitch)	–	–	–	–	–	A	A	A	A	A	A
160[2]-pin (0.5 mm lead pitch)	–	–	–	–	–	–	–	A	A	A	A
176-pin (0.5 mm lead pitch)	–	–	–	–	–	A	A	A	A	A	A
176[1]-pin (0.5 mm lead pitch)	–	–	–	–	–	–	–	–	–	A	A
176[2]-pin (0.5 mm lead pitch)	–	–	–	–	–	–	–	–	–	A	A
208-pin (0.5 mm lead pitch)	–	–	–	–	–	–	–	–	–	–	A
Thin Plastic Quad Flatpack (TQFP)											
64-pin (0.5 mm lead pitch)	A	A	A	A	–	–	–	–	–	–	–
80-pin (0.5 mm lead pitch)	A	A	A	A	–	–	–	–	–	–	–
100[1]-pin (0.5 mm lead pitch)	–	A	A	A	A	A	A	A	A	–	–
Plastic Leaded Chip Carrier (PLCC)											
68-pin (50 mils lead pitch)	–	–	–	A	A	A	A	A	A	A	–
84-pin (50 mils lead pitch)	–	–	–	A	A	A	A	A	A	A	–

1 = Cu lead frame
2 = Cu lead frame and heat sink

A = Available or under development
– = Unavailable

Note: NEC reserves the right to alter these package options based on the results of qualification. Each cell-based design/package combination must be cleared for manufacturing suitability. For the latest package availability for CB-C7, please contact your local NEC ASIC Design Center.

Typical CB-C7 Package Marking



NEC: Company Mark
JAPAN: Origin
D93000: Part Number
R: Package Code
9115K1: Lot Number
◀: Pin Number 1 Index

83NR-7687A

CB-C7 Numbering System

Part Number	Description
μPD93XXX	Contains logic only or logic plus RAM and/or ROM
μPD94XXX	Contains not only the μPD93XXX ROM code change, but also with mask change on CB-C7 FT-type (after ES mask completion)
μPD95XXX	Same as μPD93XXX but contains megamacro blocks, such as a 710XXX or V20HL/V30HL
μPD96XXX	Same as μPD95XXX but with an additional ROM code change

Table 4. Package Options (Cont'd)

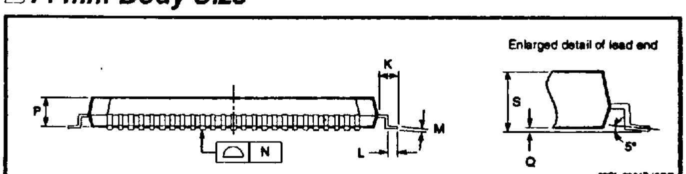
Pad Ring Step Size	F34	F74	G14	G53	G93	H33	H72	J32	J71	K11	K90
Package Type											
Plastic Quad Flatpack (QFP)											
64-pin (1 mm lead pitch)	A	–	–	–	–	–	–	–	–	–	–
80-pin (0.8 mm lead pitch)	A	–	–	–	–	–	–	–	–	–	–
100-pin (0.65 mm lead pitch)	A	–	–	–	–	–	–	–	–	–	–
120-pin (0.8 mm lead pitch)	A	A	A	A	A	A	A	A	–	–	–
136-pin (0.65 mm lead pitch)	A	A	A	A	A	A	A	A	–	–	–
160-pin (0.65 mm lead pitch)	A	A	A	A	A	A	A	A	A	A	A
160[1]-pin (0.65 mm lead pitch)	A	A	A	A	A	A	A	A	A	A	A
160[2]-pin (0.65 mm lead pitch)	A	A	A	A	A	A	A	A	A	A	A
184[1]-pin (0.65 mm lead pitch)	A	A	A	A	A	A	A	A	A	A	A
Plastic Quad Flatpack (QFP-FP)											
100-pin (0.5 mm lead pitch)	A	A	–	–	–	–	–	–	–	–	–
120-pin (0.5 mm lead pitch)	A	A	A	A	A	A	A	–	–	–	–
144-pin (0.5 mm lead pitch)	A	A	A	A	A	A	A	–	–	–	–
160-pin (0.5 mm lead pitch)	A	A	A	A	A	A	A	A	A	A	A
160[2]-pin (0.5 mm lead pitch)	A	A	A	A	A	A	A	–	–	–	–
176-pin (0.5 mm lead pitch)	A	A	A	A	A	A	A	A	A	A	A
176[1]-pin (0.5 mm lead pitch)	A	A	A	A	A	A	A	A	A	A	A
176[2]-pin (0.5 mm lead pitch)	A	A	A	A	A	A	A	–	–	–	–
208-pin (0.5 mm lead pitch)	A	A	A	A	A	A	A	A	A	A	A
208[1]-pin (0.5 mm lead pitch)	–	–	A	A	A	A	A	A	A	A	A
208[2]-pin (0.5 mm lead pitch)	–	–	A	A	A	A	A	A	A	A	A
240[1]-pin (0.5 mm lead pitch)	–	–	A	A	A	A	A	A	A	A	A
256[1]-pin (0.4 mm lead pitch)	–	–	A	A	A	A	A	A	A	A	A
272[1]-pin (0.5 mm lead pitch)	–	–	–	–	–	–	–	A	A	A	A
304[1]-pin (0.5 mm lead pitch)	–	–	–	–	–	–	–	–	–	A	A

1 = Cu lead frame
2 = Cu lead frame and heat sink

A = Available or under development
– = Unavailable

Note: NEC reserves the right to alter these package options based on the results of qualification. Each cell-based design/package combination must be cleared for manufacturing suitability. For the latest package availability for CB-C7, please contact your local NEC ASIC Design Center.

Figure 3. Popular CB-C7 Package 100-pin TQFP — □14 mm Body Size



P = 1.0 mm
K = 1.0 ± 0.2 mm
L = 0.5 ± 0.2 mm
Q = 0.1 ± 0.1 mm
M = 0.125 ± 0.05 mm
N = 0.10 mm
S = 1.25 max

NEC's ASIC Design System

NEC supports its ASIC products with a comprehensive CAD system that significantly reduces the time and expense usually associated with the development of semi-custom devices. NEC's OpenCAD Design System is a front-end to back-end ASIC design package that merges several advanced CAE/CAD tools into a single structure. The design flow combines tools for floorplanning, logic synthesis, automatic test generation, accelerated fault-grading, full timing simulation, and advanced place-and-route algorithms. RAM/ROM and Datapath Compilers are also available for use in CB-C7 designs.

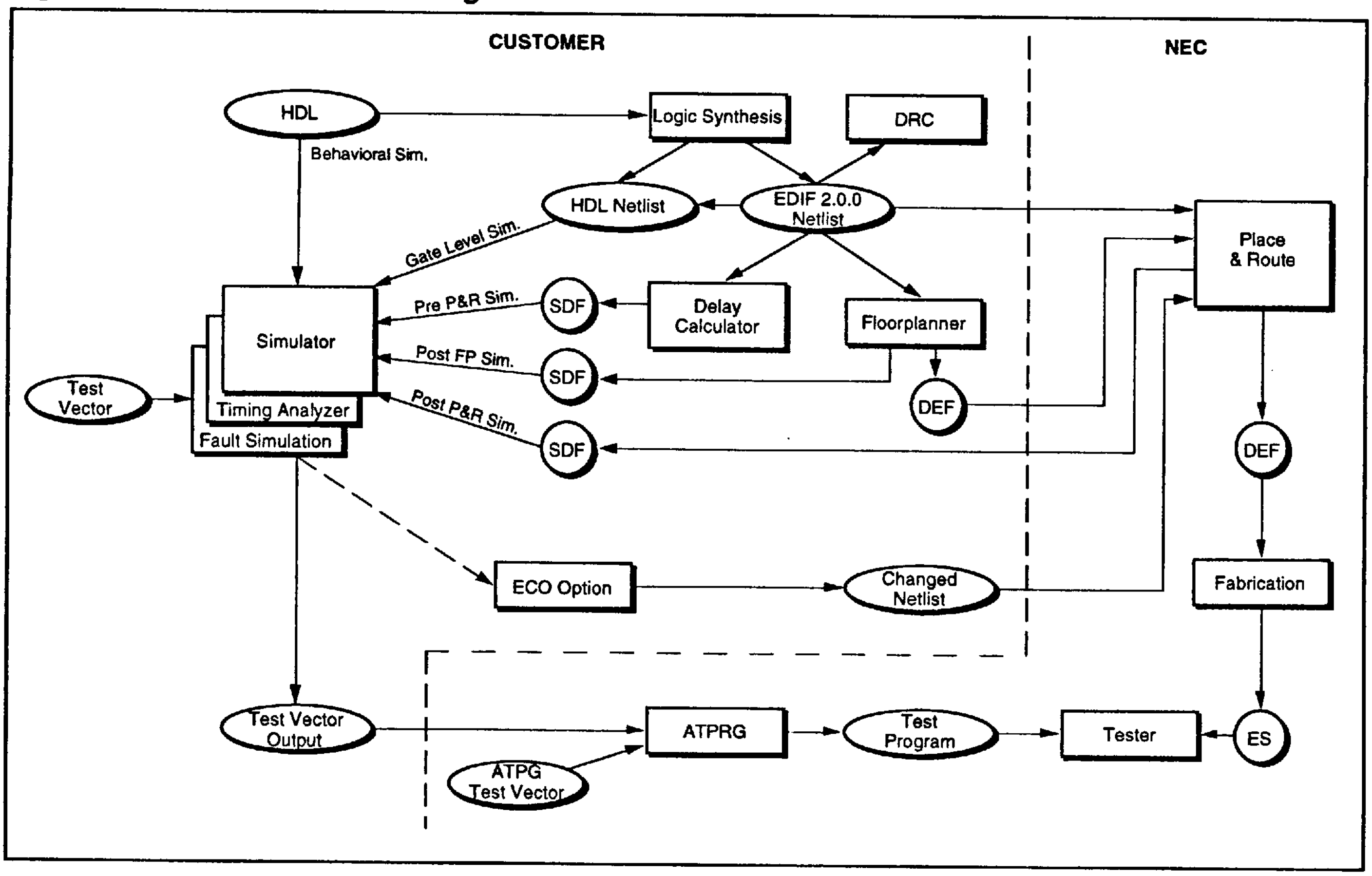
A top-down modeling methodology is possible by means of HDL specification. Designers can concentrate their design effort at a higher level of abstraction, specifying, modeling, and simulating their designs at a systems level. This leaves the details of the gate-level implementation to the synthesis tools. After having verified proper functionality, designers are free to explore functional and architectural trade-offs, and can optimize chip performance while minimizing chip area. An engineer can evaluate several architectures and select the best solution before committing to silicon. The design flow is shown below.

One of the key benefits of the ASIC design flow is that sign-off simulation can be accomplished at the customer's site since NEC offers designers a choice of simulators with the "golden simulator" status. Golden simulator status means that after receiving the post place-and-route simulation results from the customer, NEC can proceed directly to photomask production, by-passing the additional post-simulation steps.

To simplify simulation and testing of embedded cores and megamacros, full Verilog gate delay models are provided for all megamacros. The megamacros are then fully tested with a standard set of production test vectors.

The floorplanner tool provides a realistic estimate of wire length by grouping hierarchical blocks in a specific physical location on the chip. This allows for more accurate simulation results by minimizing critical path interconnect delays.

Figure 4. CB-C7 HDL-Based Design Flow



The floorplanner also allows for placement of fully-diffused functions such as memory and microprocessors. Graphical I/O assignment is available with the floorplanner. The floorplanner generates a delay file for post-floorplanner simulation, as shown in the design flow.

The ECO option allows the designer to make minor corrections in the design without requiring an entirely new placement and routing of the device. The tool ensures that relatively small changes, such as connectivity changes, will not greatly impact the timing of the current design. This can vastly improve turnaround time for the design.

NEC also incorporates proprietary tools to facilitate the design process. A single delay calculator is used for all CAE platforms to ensure consistent timing and simulation results. A comprehensive design rule check, DRC, program reports design rule violations as well as chip utilization statistics for the design netlist. The generated report contains information such as cell count and usage rate as well as net and total pin counts. Unused input pins, violations in pin naming conventions, and exceeded fan-out limits are examples of the design rule violations reported by this program.

Sample design kits are available at no charge to qualified users: Contact an NEC ASIC design center for more information. NEC's ASIC Design Centers are listed on the back of this data sheet. A software license agreement is required.

Cell Library List

The CB-C7 standard cell library offers a variety of blocks, macrocells and megafunctions. SSI library elements shown include gates, flip-flop circuits, and shift registers. The names and functions of these blocks are designed to be compatible with those of the CMOS-7 and CMOS-6 families.

Block List

Block Name	Description	I_{OL} (mA)	Area[1] (grids)
	Interface Blocks		
Input Buffers			
FI01	Input buffer, CMOS in	-	12/6
Output Buffers			
FO01	Output buffer, CMOS out	4	8/5
FO02	Output buffer, CMOS out	8	16/9
FO03	Output buffer, CMOS out	12	16/9
B007	Output buffer, CMOS 3-state out	8	24/15
Open Drain Output Buffers			
EXT1	Output buffer, N-ch open drain	4	8/4
Bi-directional I/O Buffers			
B001	I/O buffer, CMOS in, CMOS 3-state out 50 kΩ pull-up res.	8	36/21

Block Name	Description	Area[1] (grids)
	Function Blocks - Normal Power	
Inverters		
F101	Inverter (F/O = 25) (FT)	4/3
F102	Inverter (F/O = 25) (FT)	8/5
F103SD	Inverter (x3)	-/1
F104SD	Inverter (x4)	
F108SD	Inverter (x5)	
Buffers		
F111	Non-inverting buffer (F/O = 25) (FT)	8/5
F112	Non-inverting buffer (F/O = 51) (FT)	12/7
F113SD	Non-inverting buffer	-/9
F114SD	Non-inverting buffer	
F118SD	Non-inverting buffer	
Delays		
F131	Delay gate	24/13
F132	Delay gate	40/22

Block Name	Description	Area[1] (grids)
	Function Blocks - Normal Power (Cont)	
NOR Gates		
F202	2-input NOR	8/5
F203	3-input NOR	12/7
F204	4-input NOR	16/10
F208	8-input NOR	24/18
F222	2-input NOR, power	16/9
F223	3-input NOR, power	24/13
F224	4-input NOR, power	32/17
OR Gates		
F212	2-input OR	8/5
F213	3-input OR	12/6
F214	4-input OR	12/7
F232	2-input OR, power	12/7
F233	3-input OR, power	16/8
F234	4-input OR, power	16/9
NAND Gates		
F302	2-input NAND	8/5
F303	3-input NAND	12/7
F304	4-input NAND	16/9
F305	5-input NAND	20/11
F306	6-input NAND	20/12
F308	8-input NAND	24/14
F322	2-input NAND, power	16/9
F323	3-input NAND, power	24/13
F324	4-input NAND, power	32/17
AND Gates		
F312	2-input AND	8/5
F313	3-input AND	12/6
F314	4-input AND	12/7
F332	2-input AND, power	12/7
F333	3-input AND, power	16/8
F334	4-input AND, power	16/9
AND-NOR Gates		
F421	2-wide 1-2-input AND-OR inverter	12/7
F422	3-wide 1-1-2-input AND-OR inverter	16/10
F423	2-wide 1-3-input AND-OR inverter	16/9
F424	2-wide 2-2-input AND-OR inverter	16/9
F425	3-wide 2-2-2-input AND-OR inverter	24/14
F426	2-wide 3-3-input AND-OR inverter	24/13
F429	4-wide 2-2-2-2-input AND-OR inverter	32/18
F442	2-wide 4-4 input AND-OR inverter	32/17
F462	3-wide 1-2-3 input AND-OR inverter	24/14

Note (1): Grids shown are for FT/HD types respectively; * indicates I_{OH}

Block Name	Description	Area[1] (grids)
Function Blocks - Normal Power (Cont)		
OR-NAND Gates		
F431	2-wide 1-2-input OR-AND inverter	12/7
F432	3-wide 1-1-2-input OR-AND inverter	16/10
F433	2-wide 1-3-input OR-AND inverter	16/9
F434	2-wide 2-2-input OR-AND inverter	16/9
F435	2-wide 2-3-input OR-AND inverter	20/11
F436	2-wide 3-3-input OR-AND inverter	24/13
F454	4-wide 2-2-2-2-input OR-AND inverter	32/18
Parity Generators		
F581	8-bit odd parity generator	76/48
F582	8-bit even parity generator	76/48
EX-OR Gate		
F511	Exclusive-OR	16/9
EX-NOR Gate		
F512	Exclusive-NOR	16/9
Adders		
F521	1-bit full-adder	36/24
F523	4-bit binary full-adder	128/89
Buffers		
F531	3-state buffer with Enable	20/11
F532	3-state buffer with Enable low	20/11
F533	3-state buffer	36/14
Decoders		
F561	2-to-4 decoder	40/24
F981	2-to-4 decoder with Enable low	52/31
F982	3-to-8 decoder with Enable low	104/60
Shift Registers		
F911	4-bit shift register with Reset	136/75
F912	4-bit serial/parallel shift register	144/80
F913	4-bit parallel shift register with Reset low, Load	160/92
F914	4-bit shift register	112/61
Multiplexers		
L655	2-to-1 multiplexer (no enable/low drive)	-/7
F569	8-to-1 multiplexer	72/46
F570	4-to-1 multiplexer	36/27
F571	2-to-1 multiplexer	20/16
F572	Quad 2-to-1 multiplexer	76/35
Latches		
F595	R-S latch	20/14
F601	D-latch	24/14
F602	D-latch with Reset	24/15
F603	D-latch with Reset low	28/16

Block Name	Description	Area[1] (grids)
Function Blocks - Normal Power (Cont)		
Latches (Cont)		
F604	D-latch with G driver low	24/14
F605	D-latch with G low, Reset low	28/16
F901	4-bit D-latch	80/45
F902	8-bit D-latch	152/85
Flip-Flops		
F596	Synchronous R-S F/F with Set-Reset	44/28
F611	D-F/F	32/18
F614	D-F/F with Set-Reset	40/24
F617	D-F/F with Set-Reset low	40/24
F631	D-F/F C low	32/18
F637	D-F/F C low with Set-Reset low	40/24
F641	D-F/F, buffered	32/22
F644	D-F/F with Set-Reset, buffered	40/28
F647	D-F/F with Set-Reset low, buffered	40/28
F661	D-F/F C low, buffered	32/22
F667	D-F/F C low with Set-Reset low, buffered	40/28
F714	Toggle F/F with Set-Reset	36/23
F717	Toggle F/F with Set-Reset low	36/23
F737	Toggle low F/F with Set-Reset low	36/23
F744	Toggle F/F with Set-Reset, buffered	36/27
F747	Toggle F/F with Set-Reset low, buffered	36/27
F767	Toggle low F/F with Set-Reset low, buffered	36/27
F771	J-K F/F, buffered	40/24
F774	J-K F/F with Set-Reset, buffered	48/30
F777	J-K F/F with Set-Reset low, buffered	48/30
F781	J-K F/F C low, buffered	40/24
F787	J-K F/F C low with Set-Reset low, buffered	48/30
F791	Toggle F/F with Set-Reset and Toggle Enable	48/30
F792	Toggle low F/F with Set-Reset and Toggle Enable low	48/30
F922	4-bit D-F/F with Reset	136/75
F924	4-bit D-F/F	112/61
F615	D-F/F with RB	-/21
F616	D-F/F with SB	-/22
S999	2-to-1 Data Slector (Scan path)	-/10
Counters		
F961	4-bit synchronous binary counter with Reset low, buffered	240/158
F962	4-bit synchronous binary up counter with Reset low	152/102
Comparator		
F985	4-bit magnitude comparator	128/82
Miscellaneous		
F091	H, L level Generator	

Note (1): Grids shown are for FT/HD types respectively.

Block Name	Description	Area[1] (grids)
	Function Blocks - Low Power	
Inverters		
L101	(F/O = 25) (FT)	4/2
Buffers		
L111	Non-inverting buffer (F/O = 25) (FT)	4/3
NOR Gates		
L202	2-input NOR	4/3
L203	3-input NOR	8/4
L204	4-input NOR	8/5
OR Gates		
L212	2-input OR	8/4
L213	3-input OR	8/5
L214	4-input OR	12/6
NAND Gates		
L302	2-Input NAND	4/3
L303	3-Input NAND	8/4
L304	4-Input NAND	8/5
L305	5-Input NAND	12/6
L306	6-Input NAND	8/7
AND Gates		
L312	2-Input AND	8/4
L313	3-Input AND	8/5
L314	4-Input AND	12/6
AND-NOR Gates		
L421	2-Wide, 1-2-Input AND-OR Inverter	8/4
L422	3-Wide 1-1-2-Input AND-OR Inverter	8/5
L423	2-Wide, 1-3-Input AND-OR Inverter	8/5
L424	2-Wide, 2-2-Input AND-OR Inverter	8/5
L425	3-Wide, 2-2-2-Input AND-OR Inverter	12/8
L426	2-Wide, 3-3-Input AND-OR Inverter	12/7
L429	4-Wide, 2-2-2-2-Input AND-OR Inverter	16/10
L442	2-Wide, 4-4-Input AND-OR Inverter	12/9
L462	3-Wide, 1-2-3-Input AND-OR Inverter	12/8
OR-NAND Gates		
L431	2-Wide, 1-2-Input OR-AND Inverter	8/4
L432	3-Wide, 1-1-2-Input OR-AND Inverter	8/5
L433	2-Wide, 1-3-Input OR-AND Inverter	8/5
OR-AND Gates		
L434	2-Wide, 2-2-Input OR-AND Inverter	8/5
L435	2-Wide, 2-3-Input OR-AND Inverter	12/6
L436	2-Wide, 3-3-Input OR-AND Inverter	12/7
L454	4-Wide, 2-2-2-2-Input OR-AND Inverter	16/10

Block Name	Description	Area[1] (grids)
	Function Blocks - Low Power (Cont)	
Exclusive-OR		
L511	EX-OR	12/8
Exclusive-NOR		
L512	EX-NOR	12/8
Decoder		
L561	2-to-4 Decoder	24/17
L981	2-to-4 Decoder with Enable	68/42
L982	3-to-8 Decoder with Enable	68/42
Multiplexer		
L571	2-to-1 Multiplexer	16/10
L572	Quad 2-to-1 Multiplexer	40/27
Latches		
L901	4-Bit Latch	48/33
L902	8-Bit Latch	88/61
Shift Registers		
L911	4-Bit Shift Register with Reset	104/60
L912	4-Bit Serial/Parallel Shift Register	112/60
L913	4-Bit Parallel in Shift Register with Reset Low	128/80
Flip Flops		
L922	4-Bit D-F/F with Reset	104/63
L924	4-Bit D-F/F	80/49
Megafunctions		
70108H	V20HL 8-bit Microprocessor	73,367
70116H	V30HL 16-bit Microprocessor	73,367
70008A	Z80 8-bit Microprocessor	32,000
72065B	765 Floppy Disk Controller	78,580
71037	8237A Programmable DMA Controller	31,780
71051	8251A USART	17,750
71054	8254 Interval Timer	16,170
71055	8255A Peripheral Interface	9540
71059	8259A Interrupt Controller	7510
4991A	Real Time Clock	20,495
80C42	NA80C42H Keyboard	25,000/5,478
8250	NA8250	TBA

Note (1): Grids shown are for FT/HD types respectively.