AS2916
Primary Side PWM Controller

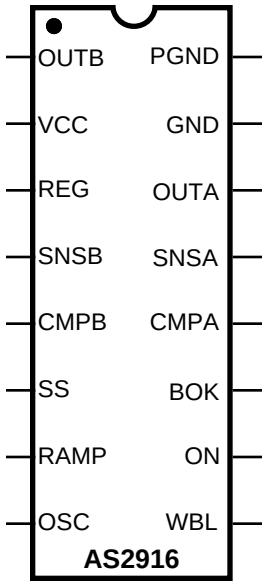
DESCRIPTION

The AS2916 is a dual, full featured, pulse width modulation controller. The second controller is intended to run the auxiliary supply. Both controllers share common oscillator and power up logic. Based on an improved AS3842, the AS2916 provides additional features that reduce component count and improve specifications in a wide range of power supply designs. The added functionality also includes bulk voltage sensing, overvoltage input and soft start.

The PWM function is controlled by the current sense comparator for normal current mode control and a second comparator for voltage mode soft start. A buffered RAMP signal is available for slope compensation without loading the oscillator. The output stage is a high current totem pole output that sees only 140 ns delay from the PWM comparators.

The AS2916 requires less than 25 μA of startup current. The undervoltage lockout (UVLO) thresholds are nominally 13.5 V for turn on and 7.5 V for turn off. The oscillator discharge current is trimmed to provide guaranteed duty cycle clamping. The AS2916 has a second low frequency oscillator, which frequency modulates the operating frequency of the PWM by 25 %, thus reducing EMI emissions..

PINOUT



AS2916
16L PDIP
16L SOIC

PIN FUNCTION DESCRIPTION

Pin Number	Function	Description
1	OUTB	This is the gate drive output for the Main FET. The totem pole output has equivalent of an extra 10 Ω resistor to limit the FET turn on speed and a pull down reisistor to ensure the FET gate is never open. No external circuitry except for the FET is expected on this pin. The largest FET expected to be driven is IRFBC40. If a larger power FET is used, a buffer might be required.
2	VCC	Positive supply for the IC. Absolute maximum rating is 20 V. The running voltage shall be provided by the Auxiliary convertor.
3	REG	Output of 5 V series regulator.
4	SNSB	This is the Main convertor current sense pin. An external RC filter from the Main power FET and slope compensation resistor from the RAMP pin is all the expected external circuitry.
5	CMPB	This is the Main output control pin. An opto isolated control signal from the secondary side error amplifier is buffered and connected to the invert pin of the main output current mode comparator. A pull-up current of 1 mA is provided so the only external circuitry expected is a common emitter opto-isolator.
6	SS	This pin provides a 6 μA current source to linearly charge an external capacitor. This pin is compared to the RAMP pin in the soft start comparator, terminating output pulses when RAMP goes above the SS voltage. While this pin is held low, the main output is inhibited.
7	RAMP	This pin is a level-shifted and buffered oscillator waveform, used to provide slope compensation for the Main and Auxiliary converters. The pin also serves as the non-inverting input of the soft-start comparator.
8	OSC	Oscillator frequency and maximum duty cycle are set by connecting a resistor (R_T) to VREG and a capacitor (C_T) to ground.
9	WBL	Provides an FM modulation of the oscillator, approximately ± 25 % deviation frequency, at a modulation rate set by an external cap at WBL. Shorting to GND eliminates modulation.
10	ON	This pin is used to remotely turn the main convertor ON/OFF either for normal user application or for protection.
11	BOK	Bulk OK. This is a brownout protection feature. The pin monitors the bulk voltage through a resistor divider. When BOK exceeds 2.5 V a 50 μA current is sourced from the pin for hysteresis. When the pin drops below 2.5 V the hysteresis is turned off and SS is pulled low, inhibiting the main output. The Auxiliary output is not tied to BOK and will run as long as there is sufficient bias voltage.
12	CMPA	This is the Auxiliary convertor error amplifier compensation pin or if secondary controller is desired, the Auxiliary control input pin. A simple capacitor to ground is the only circuitry expected. Note: There is no external connection for voltage feedback. Voltage sensing is provided internally in such way that VCC is not loaded until it reaches predefined threshold. If secondary control is required, it can be forced into the CMPA pin.
13	SNSA	This is the Auxiliary convertor current sense pin. An external RC filter from the Auxiliary power FET and slope compensation resistor from the RAMP pin is all the expected external circuitry.

Pin Number	Function	Description
14	OUTA	This is the gate drive output for the Auxiliary FET. The totem pole output has equivalent of an extra 33 Ω resistor to limit the FET turn on speed and a pull down reisistor to ensure the FET gate is never open. No external circuitry except for the FET is expected on this pin. The largest FET expected to be driven is IRF820. If a larger power FET is used, a buffer might be required.
15	GND	Signal ground.
16	PGND	Power ground.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Reference Current	I_{REF}	200	mA
Output Current	I_{OUT}	1	A
Supply Voltage	V_{CC}	20	V
Output Voltage	V_{OUT}	20	V
Continuous Power	P_D	500	mW
Junction Temperature	T_J	150	℃
Storage Temperature	T_{STG}	-60 to 150	℃
Lead Temperature (soldering, 10 seconds)	T_L	300	℃

ELECTRICAL CHARACTERISTICS

Electrical characteristics are guaranteed over the full junction temperature range (0-105 °C). Ambient temperature must be derated based upon power dissipation and package thermal characteristics. The conditions are: VCC = 15 V, BOK = 3 V, ON = 3 V, R_T = 680 Ω, C_T = 10 nF, and C_{WBL}=2.2nF, unless otherwise stated. To override UVLO, VCC should be raised above $UVLO_{high}$ prior to test.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
5 V Regulator						
Output Voltage	V_{REG}	I_{REG} = 1 mA, T_J= 25° C	4.9	5.00	5.1	V
Line Regulation	PSRR	12 ≤ V_{CC} ≤ 18 V		5	15	mV
Load Regulation		1≤ I_{REG} ≤ 20mA		5	15	mV
Temperature Stability	TC_{REG}			0.2	0.4	mV/°C
Total Output Variation		Line, Load,Temperature	4.85		5.15	V
Long-Term Stability		Over 1,000 hrs at 25°C		5	25	mV
Output Noise Voltage	V_{NOISE}	10 ≤ f ≤ 100kHz, T_J = 25°C		50		μV
Maximum Source Current	I_{MAX}	V_{REG} = 4.8 V	30	120	180	mA

Oscillator

Initial Frequency	F_{OSC}	T_J= 25° C, V_{WBL}= 0 V	117	132	143	kHz
Voltage Stability		8.5 ≤ VCC ≤ 18 V		0.2	1	%
Temperature Stability	TC_f	$T_{MIN} \leq T_J \leq T_{MAX}$		5		%
Amplitude	V_{OSC}	V_{OSC} peak-to-peak		1.55		V
Upper Trip Point	V_H	V_{WBL} = 0 V		2.8		V
Lower Trip Point	V_L	V_{WBL}= 0 V		1.25		V
Discharge Current	I_{DSC}	V_{OSC} = 3 V	7.5	8.7	9.5	mA
Duty Cycle Limit		R_T = 680 Ω, C_T = 10 nF, T_J = 25°	46	50	54	%
Over-Temperature Shutdown	T_{OT}			140		℃

Wobble Oscillator

Wobble rate	F_{WBL}	2.2 nF WBL to GND	3.4	4.5	6.0	kHz
OSC Frequency Deviation	DEV	Change in main oscillator frequency	+30	+40	+50	kHz
Amplitude	V_{WBL}	V_{WBL} peak-to-peak		1.8		V
Upper Trip Point	V_H			2.7		V
Lower Trip Point	V_L			0.9		V
Charge Current	I_{CHRG}	V_{WBL} = 0.7 V	-25	-36	-50	µA
Discharge Current	I_{DSC}	V_{WBL} = 4.8 V	25	36	50	µA

Auxiliary PWM Comparator Input (CMPA)

Regulation Voltage	VCC_{REG}		13.4	14.5	15.7	V
Transconductance	G_m			1		mS
Output Sink Current	$I_{CMPALow}$	VCC = 16V, V_{CMPA} = 1.1V	2	6		mA
Output Source Current	$I_{CMPAHigh}$	VCC = 12V, V_{CMPA} = 5V	-0.5	-1.1		mA
Output Swing High	$V_{CMPAHigh}$	VCC = 12V, I_{CMPA} = 0.5mA	5.4	5.7		V
Output Swing Low	$V_{CMPALow}$	VCC = 16V, I_{CMPA} = 2mA		0.2	1.1	V

Auxiliary Current Sense Comparator (SNSA)

Transfer Gain	A_{VSNSA}	$-0.2 \leq V_{SNSA} \leq 0.8$ V		3.00		V/V
CMPA Level Shift	V_{LS}	V_{SNSA} = 0V		1.5		V
Current Sense Threshold	V_{SNSA}	V_{CMPA} = 5V	0.95	1.05	1.15	V
Input Bias Current	I_{BIAS}			-1	-10	µA
Propagation Delay to Output	t_{PD}			80	150	ns

Main PWM Comparator Input (CMPB)

Comp Source Current	I_{CMPB}	V_{CMPB} = 2.5V	-1	-1.4		mA
Comp Source Impedance	Z_{CMPB}		10	15	20	kΩ
Comp Swing High	$V_{CMPBHigh}$		5.4	5.6		V

Main Current Sense Comparator (SNSB)

Transfer Gain	A_{VSNSB}	$-0.2 \leq V_{SNSB} \leq 0.8$ V		3.00		V/V
CMPB Level Shift	V_{LS}	V_{SNSB} = 0V		1.5		V
Current Sense Threshold	V_{SNSB}	V_{CMPB} = 5V	0.95	1.05	1.15	V
Input Bias Current	I_{BIAS}			-1	-10	µA
Propagation Delay to Output	t_{PD}			80	150	ns

Soft Start Comparator

SS charge current	$I_{Charge\ SS}$	$V_{SS} \leq V_{RAMP}$	-4	-6	-10	µA
SS discharge current	$I_{Dsc\ SS}$	V_{SS} =1 V, V_{ON} < 1.5 V	2	10		mA
SS Lower Clamp	$V_{SS\ low}$			0.05	0.2	V
Propagation Delay to Output	t_{PB}			50	100	ns
RAMP High Level	V_{RAMPH}	T_J = 25°C	2.0	2.15	2.3	V
RAMP Low Level	V_{RAMPL}	T_J = 25°C	0.45	0.6	0.75	V
RAMP Levels T_C		Note: RAMP waveform is same as OSC waveform, but level shifted down one diode drop		-2		mV/°C
RAMP Sink Current	I_{RAMPL}	T_J = 25°C	0.1	0.2		mA
RAMP Source Current	I_{RAMPH}	T_J = 25°C	-2	-10		mA

Main Output

Output Low Level	V_{OUTBL}	I_{SINK} = 10 mA		0.1	0.4	V
Output Low Level	V_{OUTBL}	I_{SINK} = 150 mA		1.5	2.2	V
Output High Level	V_{OUTBH}	I_{SOURCE} = 10 mA, VCC= 15V	12	13		V
Output High Level	V_{OUTBH}	I_{SOURCE} = 150 mA, VCC = 15V	10	10.7		V
On Resistance High				10		Ω
Rise Time	t_R	C_L = 1.3nF, 10%-90%		50	150	ns
Fall Time	t_F	C_L = 1.3nF, 90%-10%		50	150	ns
Output Impedance to GND in UVLO State	Z_{OUT}	VCC = 6 V		20		kΩ

Auxiliary Output

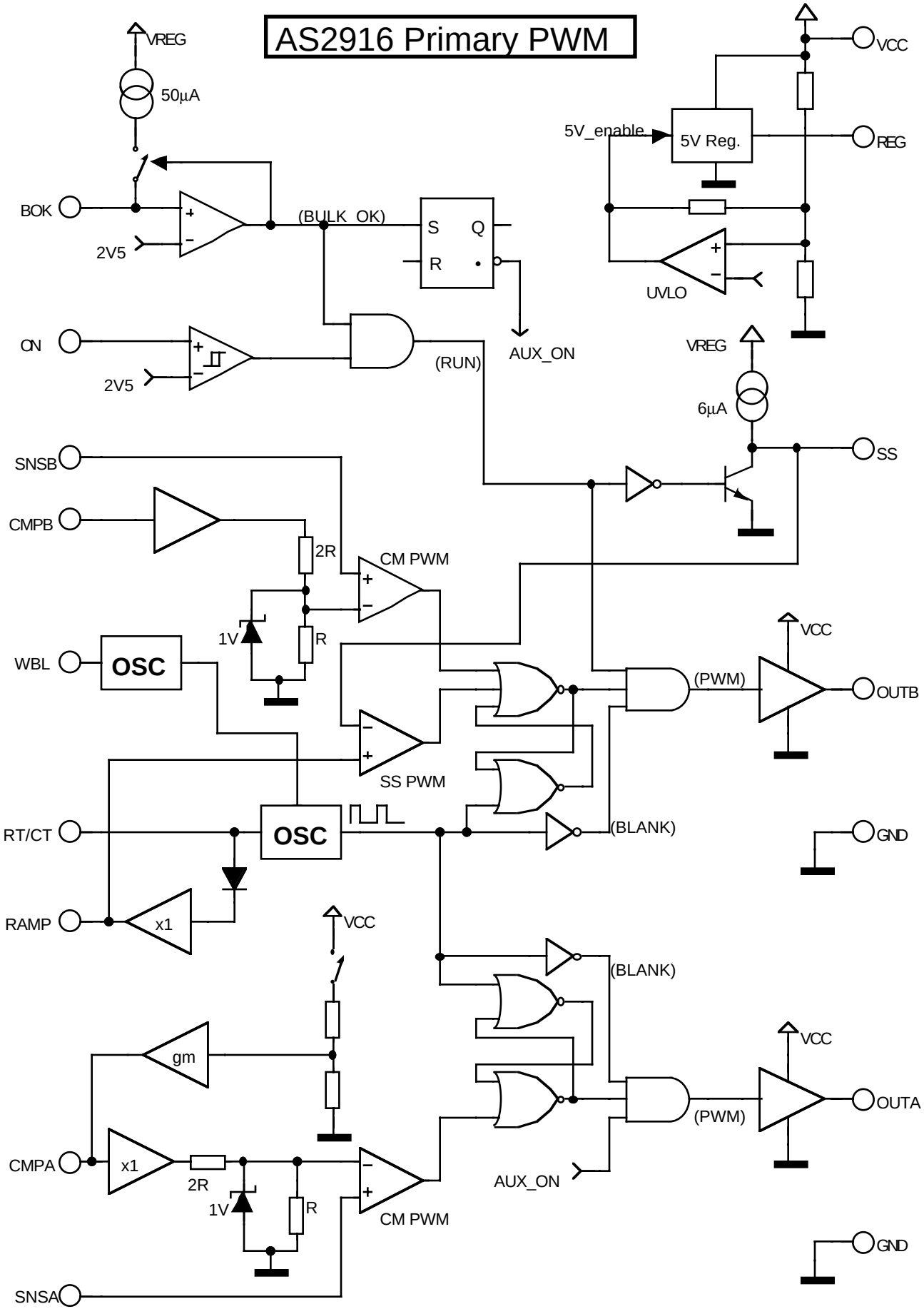
Output Low Level	V_{OUTBL}	I_{SINK} = 10 mA		0.1	0.4	V
Output Low Level	V_{OUTBL}	I_{SINK} = 150 mA		1.5	2.2	V
Output High Level	V_{OUTBH}	I_{SOURCE} = 10 mA, VCC= 15V, V_{CMPA} = 5V	12	13		V
Output High Level	V_{OUTBH}	I_{SOURCE} = 110 mA, VCC =15V, V_{CMPA} = 5V	7	8		V
On Resistance High				33		Ω
Rise Time	t_R	C_L = 350 pF, 10%-90%		70	150	ns
Fall Time	t_F	C_L = 350 pF, 90%-10%		50	150	ns
Output Impedance to GND in UVLO State	Z_{OUT}	VCC = 6 V		20		kΩ

Under-Voltage Lockout

Start-up Threshold	$V_{CC\ (ON)}$		12.4	13.5	14.7	V
Stop Threshold	$V_{CC\ (OFF)}$		7	7.5	8	V
Start-up Current	I_{CC}			0.1	25	µA
Operating Supply Current	I_{CC}	VCC = 15 V		18	25	mA

Housekeeping

BOK UV threshold	$V_{BOK\ UV}$	T_J= 25° C	2.50	2.537	2.575	V
BOK UV Hysteresis Current	$I_{HYST\ BOK}$	V_{BOK} = 2.6 V	42	50	58	µA
BOK Input Bias Current	I_{BOK}	V_{BOK} = 2.4 V		-0.1	-1	µA
ON Threshold	V_{ON}		2.35	2.5	2.65	V
ON Hysteresis	ΔV_{ON}		-0.7	-0.9	-1.1	V
ON Bias Current	$I_{BIAS\ ON}$	V_{ON} = 2.3 V		-0.5	-10	µA


AS2916 Primary PWM
VREG
50µA
BOK
2V5
(BULK_OK)
S
Q
R
AUX_ON
VCC
5V_enable
5V Reg.
REG
UVLO
ON
2V5
(RUN)
VREG
6µA
SS
SNSB
CMPB
2R
CM PWM
1V
R
WBL
OSC
VCC
(PWM)
OUTB
SS PWM
RT/CT
OSC
(BLANK)
GND
RAMP
x1
VCC
(BLANK)
gm
VCC
CMPA
x1
2R
1V
R
CM PWM
(PWM)
OUTA
AUX_ON
GND
SNSA