SSI 32R511/511R
SSI 32R5111/5111R
4, 6, 8-Channel Ferrite/MIG Read/Write Devices

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July, 1990

DESCRIPTION

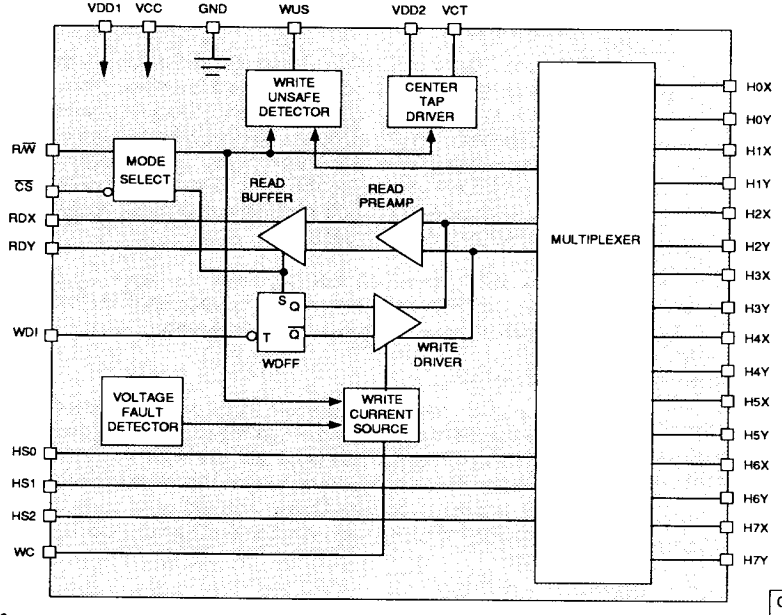
The SSI 32R511 and 32R5111 are bipolar monolithic integrated circuits designed for use with center-tapped ferrite or MIG recording heads. They offer the performance upgrades of the SSI 32R510A, along with the improved pin arrangement of the SSI 32R501. Both provide a low noise read path, write current control, and data protection circuitry for as many as 8 channels. They require +5V and +12V power supplies and are available in a variety of packages.

The R option adds internal 750Ω damping resistors. The M versions have a mirror image pin arrangement to simplify layout when using multiple devices.

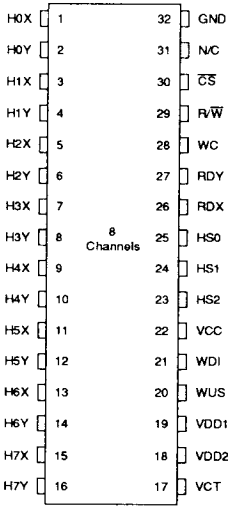
FEATURES

- **High performance**
  - **Read mode gain = 100 V/V (32R511)**
  - **= 150V/V (32R5111)**
  - **Input noise = 1.5 nV/√Hz maximum**
  - **Input capacitance = 20 pF**
  - **Write current range = 10 mA to 40 mA**
- **Enhanced system write to read recovery time**
- **Power supply fault protection**
- **Pin compatible with the SSI 32R501/501R**
- **Designed for center-tapped ferrite or MIG heads**
- **Programmable write current source**
- **Easily multiplexed for larger systems**
- **Includes write unsafe detection**
- **TTL compatible control signals**
- **+5V, +12V power supplies**
- **Mirror image pin arrangements**

BLOCK DIAGRAM



PIN DIAGRAM



32-LEAD SOW

CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

These devices give the user the ability to address up to 8 center-tapped ferrite heads and provide write drive or read amplification. Head selection and mode control is accomplished using the HSn, $\overline{CS}$ and R/$\overline{W}$ inputs as shown in tables 1 & 2. Internal pullups are provided for the $\overline{CS}$ & R/$\overline{W}$ inputs to force the device into a non-writing condition if either control line is opened accidentally.

TABLE 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

TABLE 2: Head Select

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

0 = Low level 1 = High level

WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects write mode which configures the SSI 32R511/5111 as a current switch and activates the Write Unsafe (WUS) detector circuitry. Write current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). Note that a preceding read mode selection initializes the Write Data Flip-Flop, WDFF, to pass write current through the "X" side of the head. The zero-peak write current magnitude is programmed by an external resistor Rwc from pin WC to GND and is given by:

Iw = K/Rwc, where K = Write Current Constant

The Write Unsafe detection circuitry monitors voltage transitions at the selected head connections and flags any of the following conditions as a high level on the Write Unsafe open collector output:

- Head open
- WDI frequency too low
- Device not selected
- Head center tap open
- Device in read mode
- No write current

Two negative transitions on WDI, after the fault is corrected, will clear the WUS flag.

To further assure data security a voltage fault detection circuit prevents application of write current during power loss or power sequencing.

To enhance write to read recovery time the change in RDX, RDY common mode voltage is minimized by biasing these outputs to a level within the read mode range when in write mode.

Power dissipation in write mode may be reduced by placing a resistor (RCT) between VDD1 & VDD2. The optimum resistor value is 120Ω x 40 /Iw (Iw in mA). At low write currents (<15 mA) read mode dissipation is higher than write mode and RCT, though recommended, may not be considered necessary. In this case VDD2 is connected directly to VDD1.

READ MODE

Taking $\overline{CS}$ low and R/$\overline{W}$ high selects read mode which configures the SSI 32R511/5111 as a low noise differential amplifier for the selected head. The RDX and RDY outputs are driven by emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The internal write current source is gated off in read mode eliminating the need for any external gating.

Read mode selection also initializes the Write Data Flip-Flop (WDFF) to pass write current through the "X" side of the head at a subsequent write mode selection.

IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RDX, RDY outputs into a high impedance state and deactivates the internal write current source. This facilitates multi-device installations by allowing the read outputs to be wire OR'ed and the write current programming resistor to be common to all devices.

PIN DESCRIPTIONS

NAME	I/O	DESCRIPTION
HS0-HS2	I	Head Select
$\overline{CS}$	I	Chip Select: a low level enables device
R/$\overline{W}$	I	Read/Write: a high level selects read mode
WUS	O*	Write Unsafe: a high level indicates an unsafe writing condition
WDI	I	Write Data In: negative transition toggles direction of head current
H0X-H7X H0Y-H7Y	I/O	X,Y head connections
RDX, RDY	O*	X, Y Read Data: differential read signal out
WC	*	Write Current: used to set the magnitude of the write current
VCT	-	Voltage Center Tap: voltage source for head center tap
VCC	-	+5V
VDD1	-	+12V
VDD2	-	Positive power supply for the center tap voltage source
GND	-	Ground

*When more than one R/W device is used, these signals can be wire OR'ed.

ELECTRICAL CHARACTERISTICS

RECOMMENDED OPERATING CONDITIONS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
DC Supply Voltage	VDD1		10.8	12.0	13.2	VDC
DC Supply Voltage	VCC		4.5	5.0	5.5	VDC
Head Inductance	Lh		5		15	µH
Damping Resistor	RD	32R511/5111 only	500		2000	Ω
RCT Resistor	RCT*	Iw = 40 mA	114	120	126	Ω
Write Current	IW		10		40	mA
Junction Temperature Range	Tj		+25		+135	°C

*For Iw = 40 mA. At other Iw levels refer to Applications Information that follows this specification.

ABSOLUTE MAXIMUM RATINGS (All voltages referenced to GND. Currents into device are positive. Operation above maximum ratings may permanently damage the device.)

PARAMETER		VALUE	UNITS
DC Supply Voltage	VDD1	-0.3 to +14	VDC
DC Supply Voltage	VDD2	-0.3 to +14	VDC
DC Supply Voltage	VCC	-0.3 to +6	VDC
Digital Input Voltage Range	VIN	-0.3 to VCC + 0.3	VDC
Head Port Voltage Range	VH	-0.3 to VDD1 + 0.3	VDC
WUS Pin Voltage Range	Vwus	-0.3 to +14	VDC
Write Current Zero Peak	IW	60	mA
RDX, RDy Output Current	Io	-10	mA
VCT Output Current	IVCT	-60	mA
WUS Output Current	Iwus	+12	mA
Storage Temperature Range	Tstg	-65 to 150	°C
Lead Temperature PDIP, Flat Pack (10 sec Soldering)		260	°C
Package Temperature PLCC, SO (20 sec Reflow)		215	°C

DC CHARACTERISTICS

(Unless otherwise specified, recommended operating conditions apply.)

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VCC Supply Current	Read/Idle Mode			35	mA
	Write Mode			30	mA
VDD Supply Current (sum of VDD1 and VDD2)	Idle Mode			20	mA
	Read Mode			35	mA
	Write Mode			20 + Iw	mA
Power Dissipation (Tj = +125°C)	Idle Mode			400	mW
	Read Mode			600	mW
	Write Mode, IW = 40 mA, RCT = 0Ω			800	mW
	Write Mode, IW = 40 mA, RCT = 120Ω			610	mW

DC CHARACTERISTICS (continued)

DIGITAL I/O

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VIL	Input Low Voltage				0.8	VDC
VIH	Input High Voltage		2.0		VCC + 0.3	VDC
IIL	Input Low Current	VIL = 0.8V	-0.4			mA
IIH	Input High Current	VIH = 2.0V			100	µA
VOL	WUS Output Low Voltage	IOL = 8 mA			0.5	VDC
IOH	WUS Output High Current	VOH = 5.0V			100	µA

WRITE MODE

Center Tap Voltage VCT	Write Mode		6.0		VDC
Head Current (per side)	Write Mode, 0 ≤ VCC ≤ 3.7V, 0 ≤ VDD1 ≤ 8.7V	-200		200	µA
Write Current Range		10		40	mA
Write Current Constant "K"		2.375		2.625	
Iwc to Head Current Gain			0.99		mA/mA
Unselected Head Leakage Current				85	µA
RDX, RDY Output Offset Voltage	Write/Idle Mode	-20		+20	mV
RDX, RDY Common Mode Output Voltage	Write/Idle Mode		5.3		VDC
RDX, RDY Leakage	RDX, RDY = 6V Write/Idle Mode	-100		100	µA

READ MODE

Center Tap Voltage	Read Mode		4.0		VDC
Head Current (per side)	Read or Idle Mode 0 ≤ VCC ≤ 5.5V 0 ≤ VDD1 ≤ 13.2V	-200		200	µA
Input Bias Current (per side)				45	µA
Input Offset Voltage	Read Mode	-4		+4	mV
Common Mode Output Voltage	Read Mode	4.5		6.5	VDC

DYNAMIC CHARACTERISTICS AND TIMING

(Unless otherwise specified, recommended operating conditions apply and IW = 35 mA, Lh = 10 µH, Rd = 750Ω 32R511 only, f(WDI) = 5 MHz, CL(RDX, RDY) ≤ 20 pF.)

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Differential Head Voltage Swing		7.0			V(pk)
Unselected Head Transient Current				2	mA(pk)
Differential Output Capacitance				15	pF
Differential Output Resistance	32R511, 32R5111	10K			Ω
	32R511R, 32R5111R	600		960	Ω
WDI Transition Frequency	WUS = low	250			KHz

READ MODE

Differential Voltage Gain	32R511	Vin = 1 mVpp @ 300 kHz, RL(RDX), RL(RDY)= 1kΩ	85		115	V/V
	32R5111		125		175	V/V
Dynamic Range		DC Input Voltage, Vi, Where Gain Falls by 10%. Vin = Vi + 0.5 mVpp @ 300 kHz	-3		+3	mV
Bandwidth (-3dB)		|Zs| < 5Ω, Vin = 1 mVpp	30			MHz
Input Noise Voltage		BW = 15 MHz, Lh = 0, Rh = 0			1.5	$nV/\sqrt{Hz}$
Differential Input Capacitance		f = 5 MHz			20	pF
Differential Input Resistance		32R511, f = 5 MHz	2K			Ω
Differential Input Resistance		32R511R, f = 5 MHz	460		860	Ω
Common Mode Rejection Ratio		Vcm = VCT + 100 mVpp @ 5 MHz	50			dB
Power Supply Rejection Ratio		100 mVpp @ 5 MHz on VDD1, VDD2 or VCC	45			dB
Channel Separation		Unselected Channels: Vin=100 mVpp @ 5 MHz; Selected Channel: Vin = 0 mVpp	45			dB
Single Ended Output Resistance		f = 5 MHz			30	Ω
Output Current		AC Coupled Load, RDX to RDY	±2.1			mA

DYNAMIC CHARACTERISTICS AND TIMING (continued)

SWITCHING CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
R/$\overline{W}$ To Write	Delay to 90% of Write Current			1.0	µs
R/$\overline{W}$ to Read	Delay to 90% of 100 mV, 10 MHz Read Signal Envelope or to 90% decay of Write Current			1.0	µs
$\overline{CS}$ to Select	Delay to 90% of Write Current or to 90% of 100 mV, 10 MHz Read Signal Envelope			1.0	µs
$\overline{CS}$ to Unselect	Delay to 90% Decay of Write Current			1.0	µs
HS0 - HS2 to any head	Delay to 90% of 100 mV, 10 MHz Read Signal Envelope			1.0	µs
WUS, Safe to Unsafe - TD1	Iw = 35 mA	1.6		8.0	µs
WUS, Unsafe to Safe - TD2	Iw = 35 mA			1.0	µs
Head Current (Lh = 0 µH, Rh = 0Ω)					
Prop. Delay - TD3	From 50% Points			25	ns
Asymmetry	WDI has 50% Duty Cycle and 1ns Rise/Fall Time			2	ns
Rise/Fall Time	10% - 90% Points			20	ns

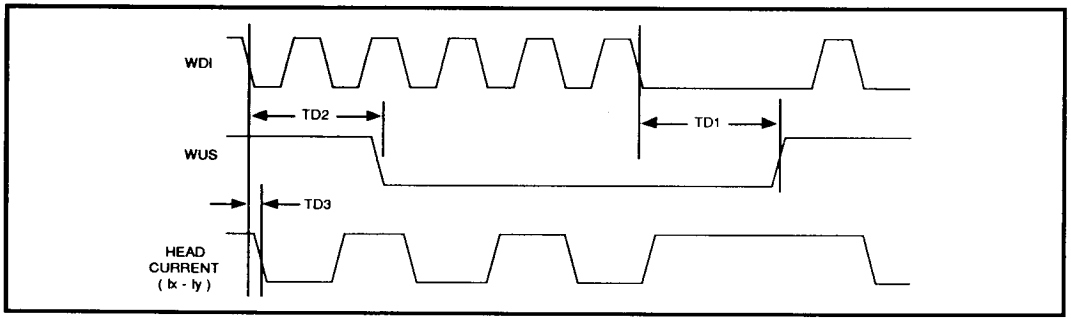
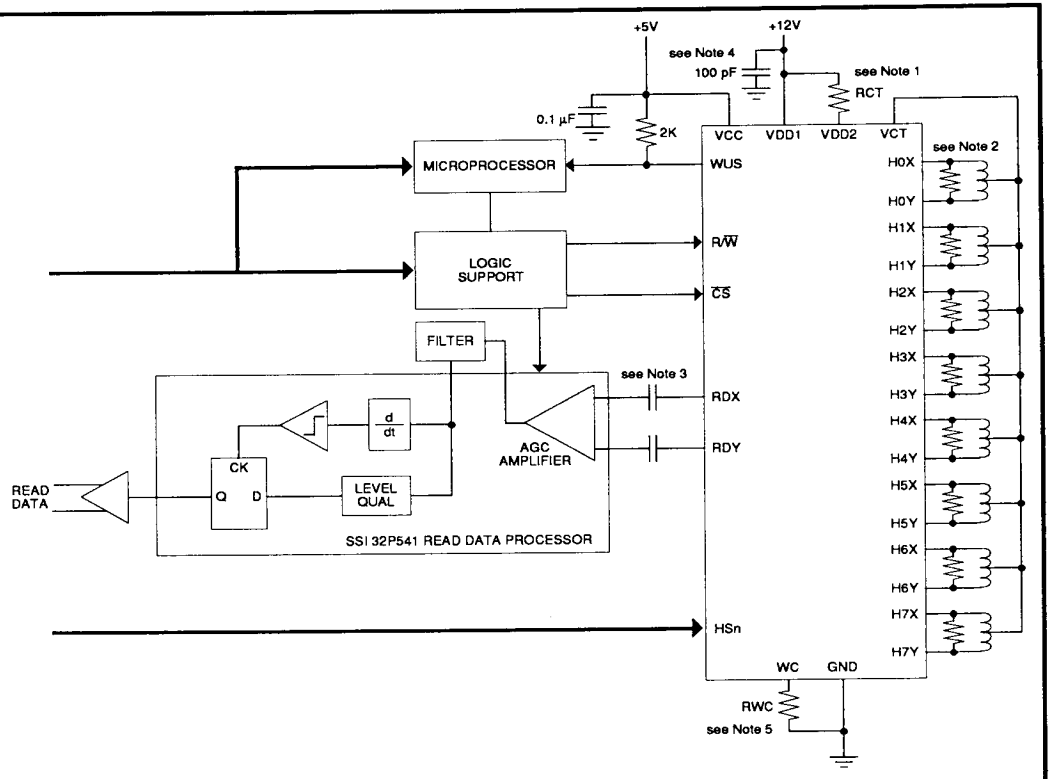


FIGURE 1: Write Mode Timing Diagram

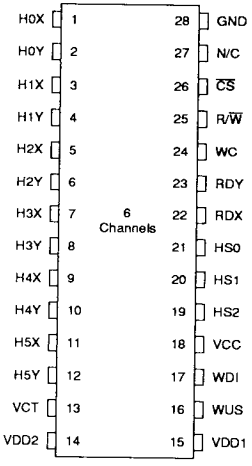


NOTES

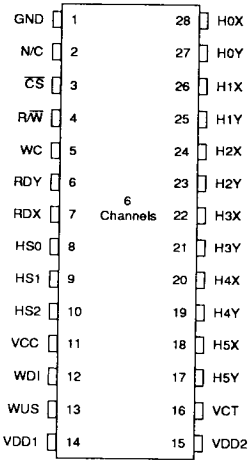
1. An external resistor, RCT, given by; RCT = 120 (40/Iw) where Iw is the zero-peak write current in mA, can be used to limit internal power dissipation. Otherwise connect VDD2 to VDD1.
2. Damping resistors not required on R versions.
3. Limit DC current from RDX and RDY to 100 µA and load capacitance to 20 pF. In multi-chip application these outputs can be wire-OR'ed.
4. The power bypassing capacitor must be located close to the device with its ground returned directly to device ground, with as short a path as possible.
5. To reduce ringing due to stray capacitance this resistor should be located close to the device. Where this is not desirable a series resistor can be used to buffer a long WC line. In multi-chip applications a single resistor common to all chips may be used.

FIGURE 2: Applications Information

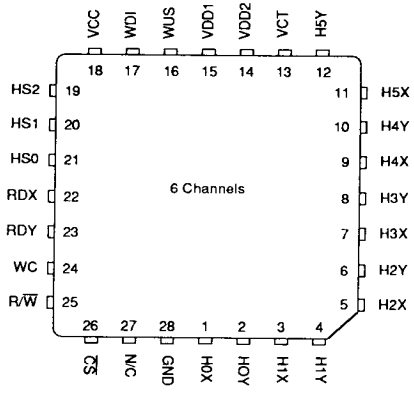
PACKAGE PIN DESIGNATIONS (Top View)



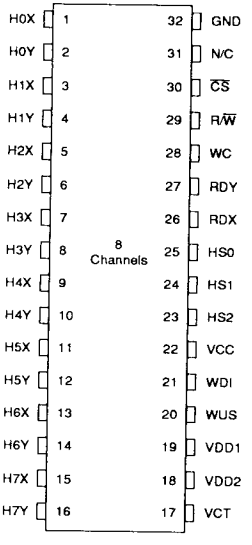
28-Lead SOL



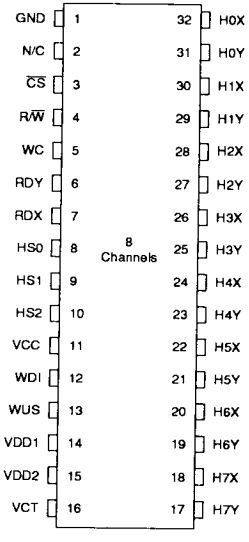
28-Lead SOL Mirror Image



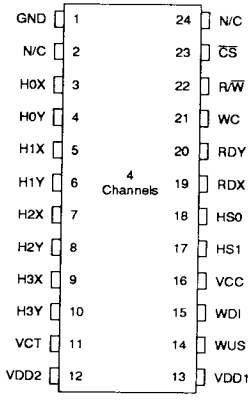
28-Lead PLCC



32-Lead Flatpack, SOW

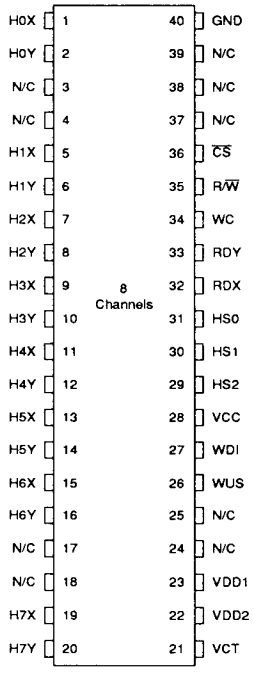


32-Lead SOW Mirror Image

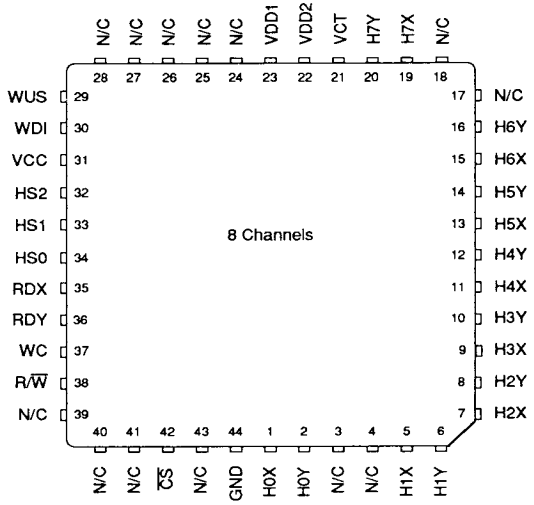


24-Lead SOL

PACKAGE PIN DESIGNATIONS (Continued)



40-Lead PDIP



44-Lead PLCC

THERMAL CHARACTERISTICS: Øja

24-lead	SOL	80°C/W
28-lead	PLCC	65°C/W
	SOL	70°C/W
32-lead	FLATPACK	60°C/W
	SOW	55°C/W
40-lead	PDIP	45°C/W
44-lead	PLCC	60°C/W

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32R511		
4-Channel SOL	SSI 32R511-4CL	32R511-4CL
6-Channel PLCC	SSI 32R511-6CH	32R511-6CH
6-Channel SOL	SSI 32R511-6CL	32R511-6CL
8-Channel Flat Pack	SSI 32R511-8F	32R511-8F
8-Channel SOW	SSI 32R511-8CW	32R511-8CW
8-Channel PDIP	SSI 32R511-8CP	32R511-8CP
8-Channel PLCC	SSI 32R511-8CH	32R511-8CH
SSI 32R511R		
4-Channel SOL	SSI 32R511R-4CL	32R511R-4CL
6-Channel PLCC	SSI 32R511R-6CH	32R511R-6CH
6-Channel SOL	SSI 32R511R-6CL	32R511R-6CL
8-Channel Flat Pack	SSI 32R511R-8F	32R511R-8F
8-Channel SOW	SSI 32R511R-8CW	32R511R-8CW
8-Channel PDIP	SSI 32R511R-8CP	32R511R-8CP
8-Channel PLCC	SSI 32R511R-8CH	32R511R-8CH
SSI 32R511M		
6-Channel SOL	SSI 32R511M-6CL	32R511M-6CL
8-Channel SOW	SSI 32R511M-8CW	32R511M-8CW
SSI 32R511RM		
6-Channel SOL	SSI 32R511RM-6CL	32R511RM6CL
8-Channel SOW	SSI 32R511RM-8CW	32R511RM-8CW

ORDERING INFORMATION (Continued)

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32R5111		
4-Channel SOL	SSI 32R5111-4CL	32R5111-4CL
6-Channel PLCC	SSI 32R5111-6CH	32R5111-6CH
6-Channel SOL	SSI 32R5111-6CL	32R5111-6CL
8-Channel SOW	SSI 32R5111-8CW	32R5111-8CW
8-Channel PLCC	SSI 32R5111-8CH	32R5111-8CH
8-Channel SOL	SSI 32R5111-8CL	32R5111-8CL
SSI 32R5111R		
4-Channel SOL	SSI 32R5111R-4CL	32R5111R-4CL
6-Channel PLCC	SSI 32R5111R-6CH	32R5111R-6CH
6-Channel SOL	SSI 32R5111R-6CL	32R5111R-6CL
8-Channel SOW	SSI 32R5111R-8CW	32R5111R-8CW
8-Channel PLCC	SSI 32R5111R-8CH	32R5111R-8CH
8-Channel SOL	SSI 32R5111R-8CL	32R5111R-8CL
SSI 32R5111M		
6-Channel SOL	SSI 32R5111M-6CL	32R5111M-6CL
8-Channel SOW	SSI 32R5111M-8CW	32R5111M-8CW
8-Channel SOL	SSI 32R5111M-8CL	32R5111M-8CL
SSI 32R5111RM		
6-Channel SOL	SSI 32R5111RM-6CL	32R5111RM-6CL
8-Channel SOW	SSI 32R5111RM-8CW	32R5111RM-8CW
8-Channel SOL	SSI 32R5111RM-8CL	32R5111RM-8CL

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 731-5457