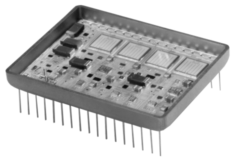
SMART POWER H-BRIDGE MOTOR DRIVE



DESCRIPTION

The PWR-82341 is a smart Power H-Bridge Motor Drive hybrid. The PWR-82341 uses a MOSFET output stage with a 100Vdc rating, and can deliver 5A continuous, 10 A peak current to the load.

This Smart Power Motor Drive has CMOS Schmitt Trigger inputs for high noise immunity. High and low-side input logic signals are XOR'd in each phase to prevent simultaneous turn on of in-line transistors, thus eliminating a shoot through condition.

The internal logic controls the high and low-side gate drivers for each phase and can operate from +5 to +15 V logic levels. An internal charge pump circuit provides the required voltage to the high-side gate drives. This ensures constant output performance for switching frequencies from DC to 50 kHz.

APPLICATIONS

Packaged in a small case, these hybrids are an excellent choice for high performance, high-reliability motor drives for Military and Aerospace servo-amps and speed controls.

Among the many applications are robotics; electro-mechanical valve assemblies; actuator systems; antenna and radar positioning; fan and blower motors for environmental conditioning; position control of mini-subs, drones, and RPV's; and compressor motors for cryogenic coolers.

The PWR-82341 hybrid is ideal for harsh military environments where shock, vibration, and temperature extremes are evident, such as missile applications including fin actuators and I. seeker head movement. The PWR-82341 operates over the -55°C to +125°C temperature range and is available with military processing.

FEATURES

- ***Small size (1.8" x 1.4" x 0.25")***
- ***100 VDC Rating***
- ***5 A Continuous, 10 A peak Capability***
- ***High-Efficiency MOSFET Drive Stage***
- ***Direct Drive from PWM***
- ***Drive Brush or Brushless DC Motors***
- ***Four Quadrant Operation***
- ***Military Processing Available***

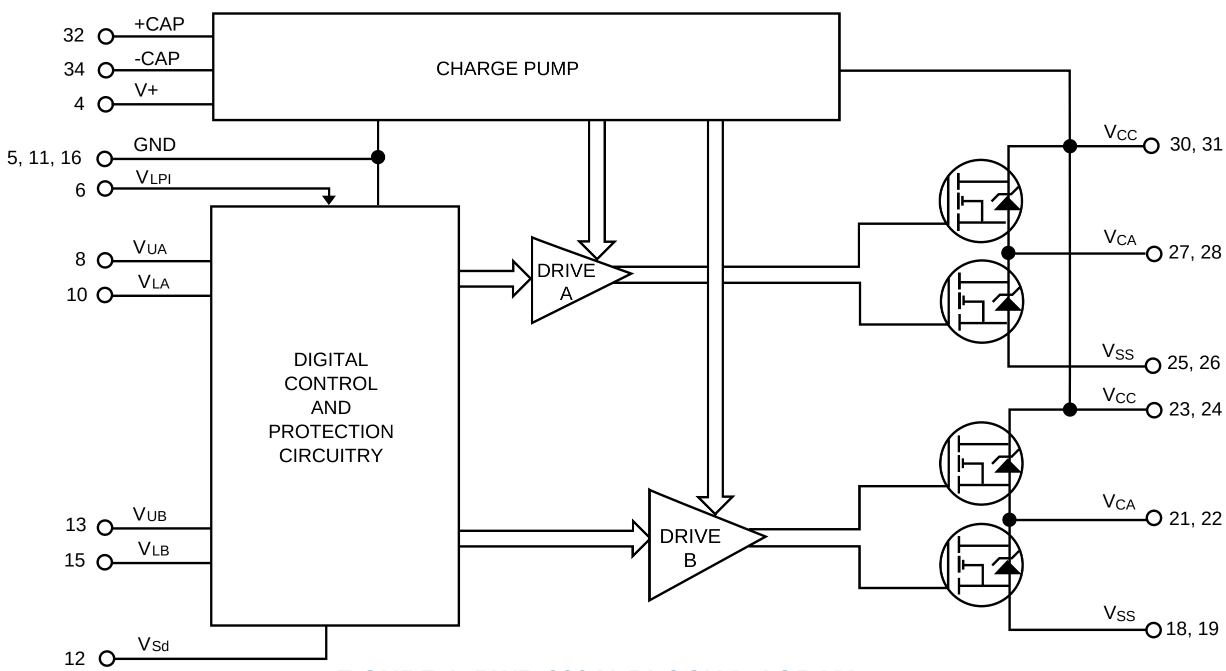


FIGURE 1. PWR-82341 BLOCK DIAGRAM

TABLE 1. PWR-82341 ABSOLUTE MAXIMUM RATINGS (Tc = +25°C Unless Otherwise Specified)			
PARAMETER	**SYMBOL**	**VALUE**	**UNITS**
SUPPLY VOLTAGE	V_{CC}	100	V
INPUT VOLTAGE	V+	18	V
LOGIC POWER-IN VOLTAGE	V_{LPI}	18	V
INPUT LOGIC VOLTAGE	V_U, V_L, VSd	V_{LPI} + 0.5	V
OUTPUT CURRENT			
Continuous	I_O	5	A
Peak	I_P	10	A
OPERATING FREQUENCY	f_O	50	kHz
CASE OPERATING TEMPERATURE	T_C	-55 to +125	°C
CASE STORAGE TEMPERATURE RANGE	T_{CS}	-55 to +150	°C

TABLE 2. PWR-82341 SPECIFICATIONS (TC=+25°C Unless Otherwise Specified)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
OUTPUT						
Output Current Continuous	I_o	See NOTE 1			5	A
Supply Voltage	V_{cc}	Ip=5A (See NOTE 2)		28	100	V
Output On-Resistance (each FET)	R_{ON}	Ip=5A (See NOTE 2)			0.13	Ω
Instant Forward Voltage (intrinsic diode)	V_F	Id=1A, di_d/dt=160A/µs			1.25	V
Reverse Recovery Time (intrinsic diode)	trr	See NOTE 3		160	500	nsec
Reverse Leakage Current	Ir				250	µA
INPUT POWER						
Input Voltage (T_C=-55°C to +125°C)	V+	V+ = 15V, f_o = 20kHz	12	15	18	V
Logic Power-in Voltage	V_{LPI}	V_{LPI} = 15 V	5		18	V
V+ Current	I+				35	mA
Logic Power Input Current	I_{LPI}				5	mA
INPUT SIGNALS		**Pin Connections**				
Positive Trigger Threshold Voltage	V_P	V_{LPI} = 15 V	6.8		10	V
Negative Trigger Threshold Voltage	V_N	V_{LPI} = 15 V	4.0		7	V
Positive Trigger Threshold Voltage	V_P	V_{LPI} = 5 V	2.2		3	V
Negative Trigger Threshold Voltage	V_N	V_{LPI} = 5 V	0.9		2	V
SWITCHING CHARACTERISTICS (See FIGURE 2)						
Upper Drive:						
Turn-on Propagation Delay	td(on)				825	nsec
Turn-off Propagation Delay	td(off)	**Test 1 Conditions**			1100	nsec
Shut-down Propagation Delay (see FIGURE 5)	tsd	V_{LPI} = +15 V, V+ = 15 V			1000	nsec
Turn-on Rise Time	tr	V_{CC} = +28 V, I_p = 10 A			125	nsec
Turn-off Fall Time	tf				200	nsec
Lower Drive:						
Turn-on Propagation Delay	td(on)				825	nsec
Turn-off Propagation Delay	td(off)				1100	nsec
Shut-down Propagation Delay (see FIGURE 5)	tsd				1000	nsec
Turn-on Rise Time	tr				200	nsec
Turn-off Fall Time	tf				200	nsec
SWITCHING CHARACTERISTICS (Ssee FIGURE 2)						
Upper Drive:		**Test 2 Conditions**				
Turn-on Propagation Delay	td(on)	V_{LPI} = +5 V, V+ = 15 V			1150	nsec
Turn-off Propagation Delay	td(off)	V_{CC} = +28 V, I_p = 10 A			1400	nsec
Shut-down Propagation Delay (see FIGURE 5)	tsd				1050	nsec
Turn-on Rise Time	tr				125	nsec
Turn-off Fall Time	tf				225	nsec

PWR-82341 Errata Sheet

This errata sheet replaces the section on INPUT SIGNALS in Table 2 on page 2.

TABLE 2. PWR-82340/82342 SPECIFICATION
(T_C = +25°C Unless Otherwise Specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SIGNALS (See Figure 7)		**Pin Connections**				
Positive Trigger Threshold Voltage	V_P	V_{LPI} = 15V			12.9	V
Negative Trigger Threshold Voltage	V_N	V_{LPI} = 15V	2.1			V
Hysteresis Voltage	V_H	V_{LPI} = 15V	1.6		10.8	V
Positive Trigger Threshold Voltage	V_P	V_{LPI} = 5V			4.3	V
Negative Trigger Threshold Voltage	V_N	V_{LPI} = 5V	0.9			V
Hysteresis Voltage	V_H	V_{LPI} = 5V	0.3		3.6	V

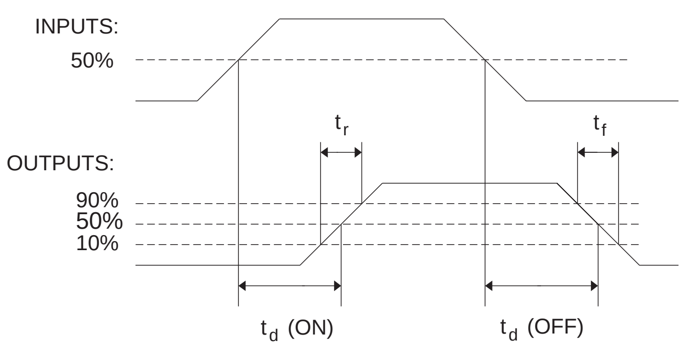
TABLE 2. PWR-82341 SPECIFICATIONS (continued) (T_C= +25°C Unless Otherwise Specified)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
SWITCHING CHARACTERISTICS (continued) **Lower Drive:** Turn-on Propagation Delay Turn-off Propagation Delay Shut-down Propagation Delay (see FIGURE 5.) Turn-on Rise Time Turn-off Fall Time	 td(on) td(off) tsd tr tf	**Test 2 Conditions** V_{LPI} = +5 V, V+ = 15 V V_{CC} = +28 V, I_P = 10 A			 1150 1400 1050 125 225	 nsec nsec nsec nsec nsec
DEAD TIME	t_{dt}		400			nsec
MINIMUM PULSE WIDTH	t_{pw}		150			nsec
THERMAL Maximum Thermal Resistance Junction Temperature Range Case Operating Temperature Case Storage Temperature	 θjc Tj T_{CO} T_{CS}	 each transistor	 -55 -55 -55		 7.5 150 125 150	 °C/W °C °C °C
WEIGHT					1.05 (30)	0z (g)

NOTES:
1. For Hi-Reliability applications, derating per MIL-S-19500 should be observed. (Derate V_{CC} to 70%.)
2. Pulse Width ≤ 300 µs, duty cycle ≤ 2%
3. V_{CC} = 70 V, V_U, V_L, = logic ‘0’

INTRODUCTION

The PWR-82341 is a 5 Amp, H-bridge motor drive hybrid which incorporates a 100 Vdc MOSFET output stage for high-speed and high-efficiency operation. This motor drive is ideal for use in high-performance motion control systems, servo amplifiers, and motor speed control designs. Furthermore, Multi-axis systems requiring multiple drive stages can benefit from the small size of this power drive.

The PWR-82341 can be driven directly from a PWM, DSP, or a custom ASIC that supplies digital signals to control the upper and lower transistors of each phase. This highly integrated drive stage has Schmitt Trigger digital inputs that control the high and low side of each phase. Digital protection of each phase eliminates an in-line firing condition, by preventing simultaneous turn-on of both the upper and lower transistors. This logic also controls the high and low-side gate drivers. Operation from +5 to +15 V logic levels can be programmed by applying the appropriate voltage to the VLpi pin . The PWR-82341 has a ground referenced low-side gate drive. An internal charge pump circuit supplies the required drive voltage to the two high-side transistors. This provides a continuous high-side gate drive; even during motor stall. The high and low-side gate drivers control the N-channel MOS-FET output stage. The MOSFETs used in the PWR-82341 allow output switching up to 50 kHz. The PWR-82341 does not have internal short-circuit or overcurrent protection; which if required, must be added externally to the hybrid.



(REFERENCE TABLE 2. ALSO)

FIGURE 2. INPUT/OUTPUT TIMING RELATIONSHIPS

DIGITALLY CONTROLLED INPUTS

The PWR-82341 uses Schmitt Trigger digital inputs (with hysteresis) to ensure high noise immunity. The trigger switches at different points for positive and negative going signals. Hysteresis voltage (V_H) is the difference between the positive going voltage (V_P) and the negative going voltage (V_N) (see FIGURE 3).

The digital inputs have programmable logic levels, which allows the hybrid to be used with different types of control logic with an input voltage range of +5 to +15 V, such as TTL or CMOS logic. The Vlpi pin is the logic power input for the digital circuitry inside the hybrid. **A 0.01 µF, 50 V ceramic capacitor must be placed between VLpi pin and GND as close to the hybrid as possible.** When using 5 V control circuitry, an external +5 Vdc power supply must be connected between the Vlpi pin of the hybrid, and GND. The control circuitry can be as simple as a PWM, or as sophisticated as a microprocessor or custom ASIC, depending on the system requirements. FIGURE 4 illustrates a typical interface of the PWR-82341 with a motor and PWM in a Servo-Amp System.

SHUT-DOWN INPUT (V_{Sd})

The V_{Sd} pin provides a digital shut-down input, which allows the user to completely turn off both the upper and lower-output transistors in all three phases. Application of a logic “1” to the V_{Sd} input will latch the Digital Control/Protection circuitry thereby turning off all output transistors. The Digital Control/Protection circuitry remains latched in the off state and will not respond to signals on the V_L or V_U inputs while the V_{Sd} has a logic “1” applied. When the user or the sense circuitry (as in FIGURE 6) returns the V_{Sd} input to a logic “0”, and then the user sets the V_L and V_U inputs to a logic “0” the output of the Digital Control/Protection circuitry will clear the internal latch. When the next rising edge (see FIGURE 5) occurs on the V_L or V_U digital inputs, the outputs transistors will respond to the corresponding digital input. This feature can be used with external current limit or temperature sense circuitry to disable the drive if a fault condition occurs (see FIGURE 6).

INTERNAL PROTECTION CIRCUITRY

The hybrid contains digital protection circuitry, which prevents in-line transistors from conducting simultaneously. This, in effect, would short circuit the power supply and would damage the output stage of the hybrid. This circuit permits only proper input signal patterns to produce output conduction. TABLE 3 lists the input/output timing relationships. If an improper input requested that the upper and lower transistors of the same phase conduct together, the output would be a high impedance until removal of the illegal code from the input of the PWR-82341. **A dead time of 400 nsec minimum should still be maintained between the signals at the Vu and VL pins;** this ensures the complete turn-off of any transistor before turning on its associated in-line transistor.

TABLE 3. INPUT-OUTPUT TRUTH TABLE

INPUTS					OUTPUTS	
UPPERS		LOWERS		CONTROL		
V_{UA}	V_{UB}	V_{LA}	V_{LB}	V_{SD}	V_{OA}	V_{OB}
0	0	1	1	0	L	L
0	1	1	0	0	L	H
1	1	0	0	0	H	H
1	X	1	X	0	Z	X
X	1	X	1	0	X	Z
0	0	0	0	0	z	z
x	x	x	x	1	z	z

H = High Level L = Low Level
X = Don’t Care Z = High Impedance State (off)

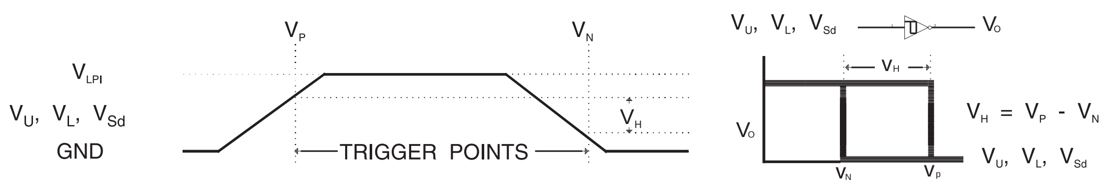


FIGURE 3. HYSTERESIS DEFINITION AND CHARACTERISTICS

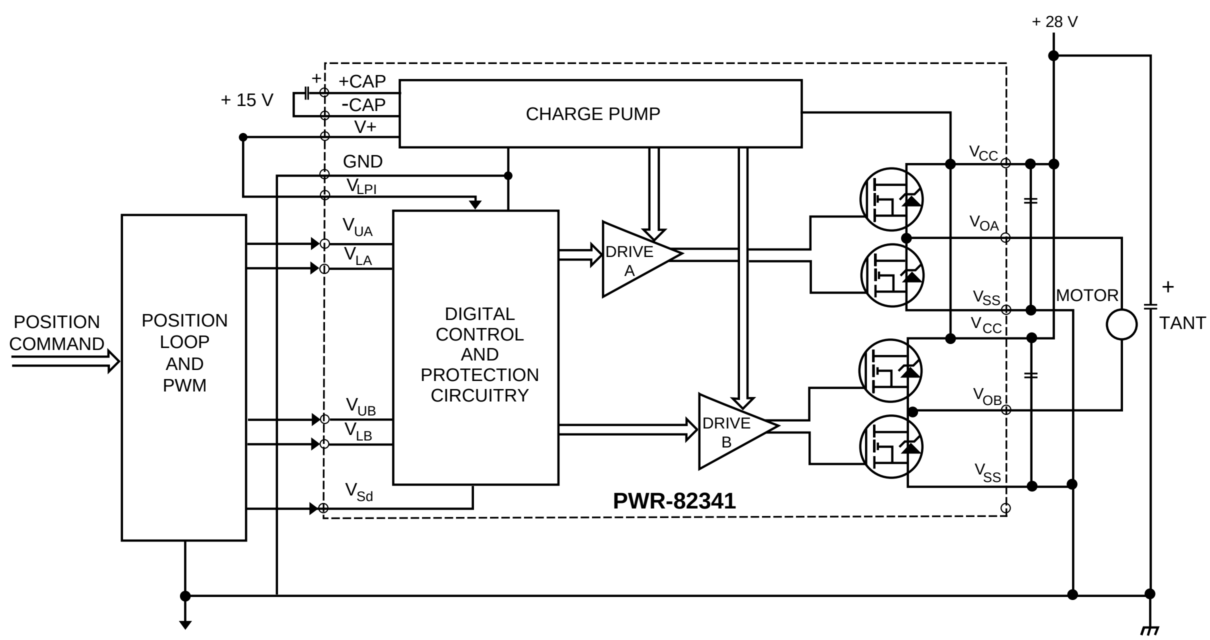


FIGURE 4. TYPICAL INTERFACE WITH A MOTOR AND PWM

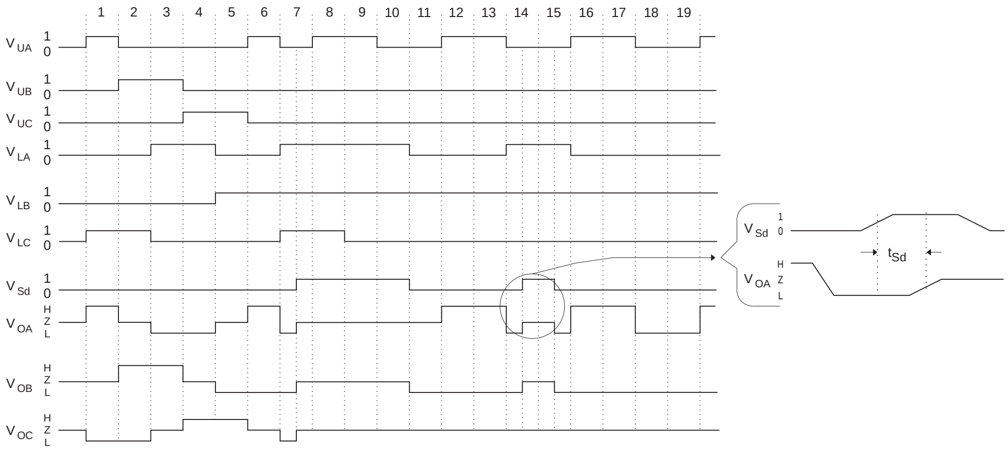


FIGURE 5. SHUT-DOWN (VSD) TIMING RELATIONSHIPS

CHARGE PUMP

The PWR-82341 has an internal charge pump circuit to generate the drive voltage for the high side N-channel MOSFETs (see Figure 4). The charge pump uses an oscillator to charge an external charge pump capacitor, Cc, from the Vcc supply. This oscillator will pump the voltage at the +cap pin (48) of the hybrid higher than Vcc. The hybrid high side drivers use this voltage to ensure proper gate drive.

An external 1 µF, 20% capacitor (Cc) is required between the +cap pin and the -cap pin (50) on the hybrid. If a polarized capacitor is used, the positive terminal must be connected to the +cap pin. The voltage rating of Cc must be 2x the maximum value of Vcc.

PWR-82341 POWER DISSIPATION (SEE FIGURE 7)

There are three major contributors to power dissipation in the motor driver: conduction losses, switching losses, and intrinsic diode losses.

V_{CC} = +28 V (Bus Voltage)

I_{OA} = 3 A, I_{OB} = 7 A (see FIGURE 7)

ton = 20 µs, T = 40 µs (period) (see FIGURE 7)

Ron = 0.13 Ω (on-resistance, see TABLE 2, Io = 5 A, Tc= +25°C)

ts1 = 325 ns, ts2 = 325 ns (see FIGURE 7)

fo = 25 kHz (switching frequency)

V_F is an intrinsic diode forward voltage, TABLE 2, Io = 5 A

1. Conduction Losses (P_C)

Pc = (Imotor rms)^2 x Ron

Pc = (Imotor rms)^2 x Ron

$$I_{\text{motor rms}} = \sqrt{\left(I_{OB}^{2} - I_{OB}\,(I_{OB} - I_{OA}) + \frac{(I_{OB} - I_{OA})^{2}}{3}\right)\left(\frac{ton}{T}\right)}$$

$$I_{\text{motor rms}} = \sqrt{\left(7A^{2} - 7A\,(7A - 3A) + \frac{(7A - 3A)^{2}}{3}\right)\left(\frac{20us}{40us}\right)}$$

Pc = (3.63 A)^2 x (0.13 Ω)

Pc = 1.71 Watts

2. Switching Losses (P_S)

Ps = [Vcc (I_{OA} (ts1) +I_{OB} (ts2)) fo] / 2

Ps = [28 V (3 A (325 ns) +7 A (325 ns)) 25 kHz] / 2

Ps = 1.14 Watts

3. Intrinsic Diode Losses (P_d)

Pd= Id (avg) x Vd (avg)

Id(avg) = [(I_{OB} + I_{OA}) / 2] / 2 = [(7 A +3 A) / 2] / 2 = 2.5 A

Pd = 2.5 A x 1.25 V

Pd = 3.125 Watts

TRANSISTOR POWER DISSIPATION (P_Q)

To calculate the maximum power dissipation of the output transistor as a function of the case temperature use the following equation. (Reference FIGURE 9 to ensure you don't exceed the maximum allowable power dissipation of each transistor.

P_Q = Pc + Ps + Pd

TOTAL HYBRID POWER DISSIPATION (P_{TOTAL})

To calculate Total Power dissipated in the hybrid use:

$$P_{TOTAL} = \sum_{i=1}^{6} [PQi] \text{ where i = each transistor}$$

LAYOUT AND EXTERNAL COMPONENTS

Important Information – The following layout guidelines and required external components are critical to the proper operation of these motor drives.

Permanent damage will result to the motor drive if the user does not make the following recommended ground connections that will ensure the proper operation of the hybrid.

To prevent damage to the internal drive circuitry, the differential voltage between GND and Vss must not exceed ±3 V max, dc or peak. This includes the combined voltage drop of the associated ground paths and the voltage drop across Rsense (see FIGURE 8). For example, a value for Rsense of 0.1 Ω will give a voltage drop of 1.00 V at 10 A and allow enough margin for the voltage drop in the ground conductors. Locate Rsense 1"–2" maximum from the hybrid. **It is critical that all ground connections be as short, and of lowest impedance, as the system allows.**

C1 and C2 are 0.1 µF ceramic bypass capacitors that suppress high frequency spiking. The voltage rating should be 2x the maximum system voltage. Locate them as close to the hybrid as possible. Please note, on FIGURE 8, that C1 and C2 must go directly from terminal-to-terminal on the hybrid – **do not daisy chain along the power ground return.**

C3 and C4 are 0.01 µF, 50 V ceramic capacitors for power supply decoupling. Locate them as close to the hybrid as possible. Cc is a 1 µF, 20% capacitor (either polarized or nonpolarized). If a polarized cap is used, the positive terminal must be connected to the +cap pin of the hybrid. Voltage rating should be 2x the maximum system voltage.

Care must be taken to control the regenerative energy produced by the motor in order to prevent excessive voltage spiking on the V_{CC} line. This can be accomplished by placing a capacitor or clamping diode between V_{CC} and the high power ground return.

TABLE 4. PIN ASSIGNMENT TABLE

PIN	FUNCTION	PIN	FUNCTION
1	NC	34	-CAP
2	NC	33	NC
3	NC	32	+CAP
4	V+	31	V_{CC}
5	GND	30	V_{CC}
6	V_{LPI}	29	NC
7	NC	28	V_{OA}
8	V_{UA}	27	V_{OA}
9	NC	26	V_{SSA}
10	V_{LA}	25	V_{SSA}
11	GND	24	V_{CC}
12	V_{SD}	23	V_{CC}
13	V_{UB}	22	V_{OB}
14	NC	21	V_{OB}
15	V_{LB}	20	NC
16	GND	19	V_{SSB}
17	NC	18	V_{SSB}

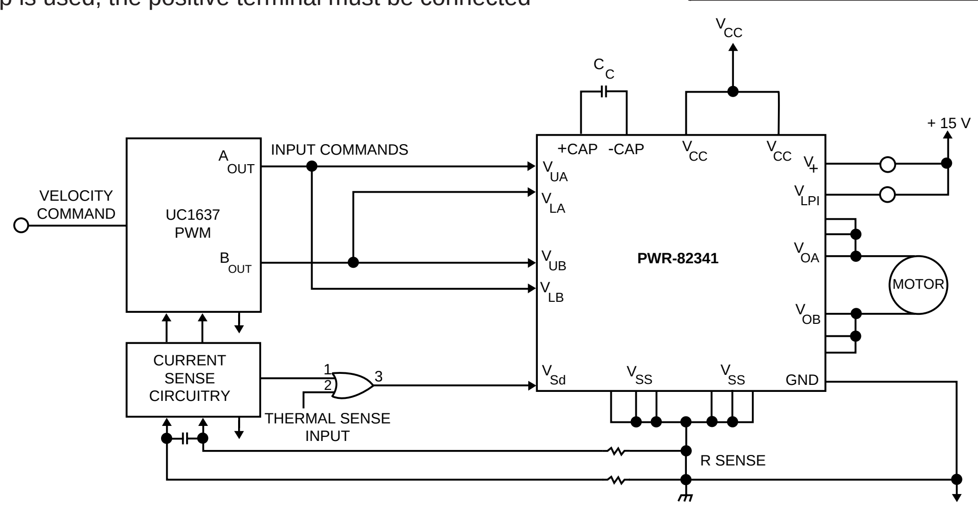


FIGURE 6. SHUT-DOWN INPUT USED WITH CURRENT-SENSING CIRCUITRY

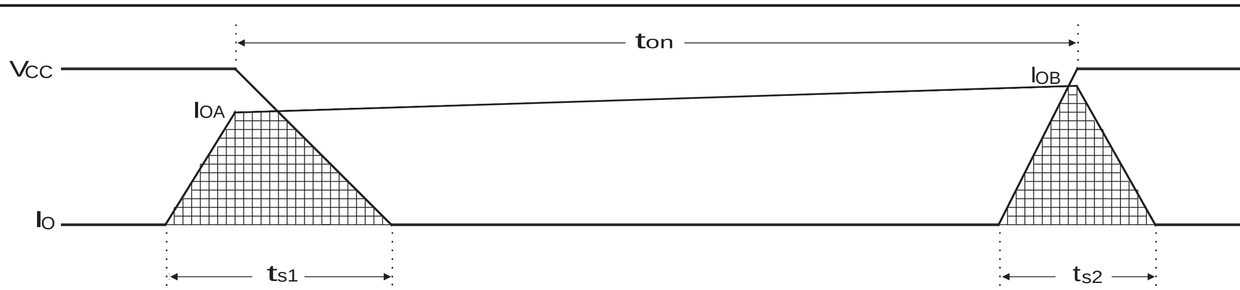


FIGURE 7. OUTPUT CHARACTERISTICS

MOUNTING

The PWR-82341 package is designed for direct insertion to a printed wiring board. The heat transfer in a hybrid is from semi-conductor junction to the bottom of the hybrid case. The flatness and maximum temperature of this mounting surface are critical to the performance and reliability, because this is the only method of dissipating the power generated in the hybrid. Use a mounting surface flatness of 0.004 inches/inch maximum. This interface can be improved with the use of a thermal compound or pad.

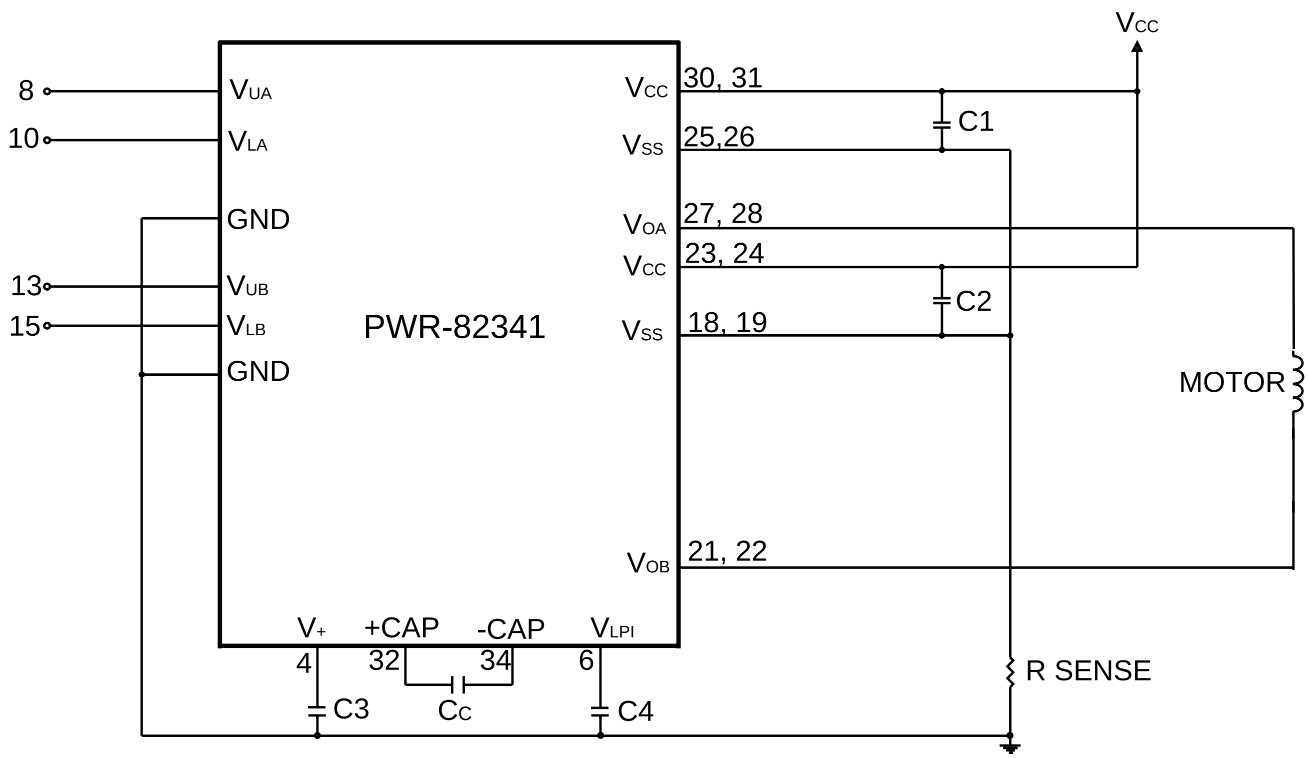


FIGURE 8. GROUNDING CONNECTIONS

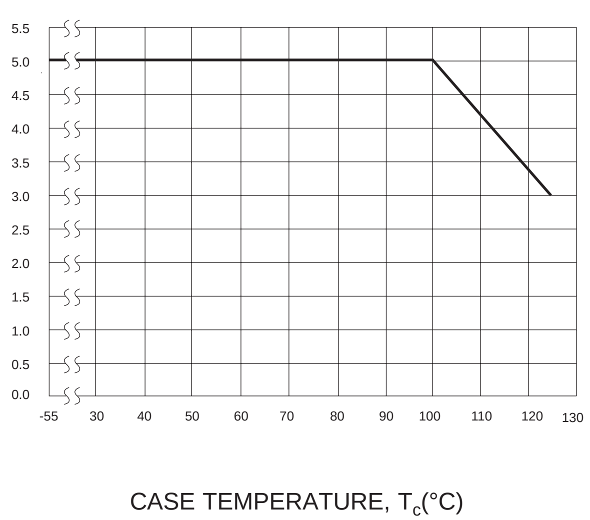
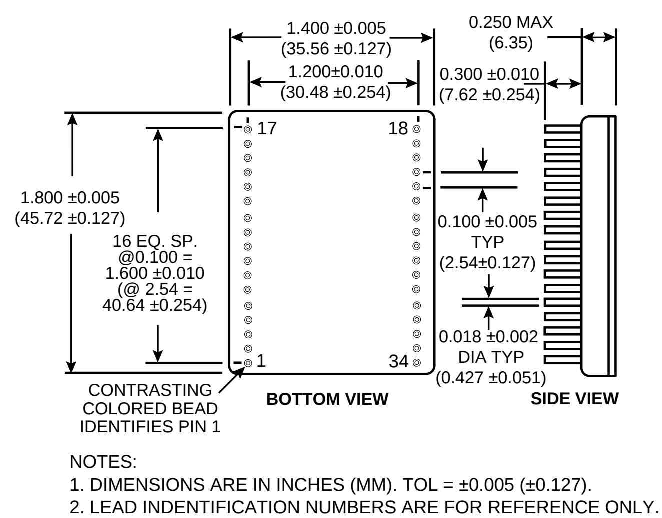


FIGURE 9. MAXIMUM ALLOWABLE CONTINUOUS OUTPUT CURRENT VS. CASE TEMPERATURE



NOTES:
1. Dimension in Inches (MM), Tolerance = ±0.005 (0.127)
2. Lead Identification Numbers are for reference only.

FIGURE 10. MECHANICAL LAYOUT

ORDERING INFORMATION

PWR-82341-XX0X

Supplemental Process Requirements:
- S = Pre-Cap Source Inspection
- L = Pull Test
- Q = Pull Test and Pre-Cap Inspection
- Blank = None of the Above

Process Requirements:
- 0 = Standard DDC Processing, no Burn-In (See table below.)
- 1 = MIL-PRF-38534 Compliant
- 2 = B*
- 3 = MIL-PRF-38534 Compliant with PIND Testing
- 4 = MIL-PRF-38534 Compliant with Solder Dip
- 5 = MIL-PRF-38534 Compliant with PIND Testing and Solder Dip
- 6 = B* with PIND Testing
- 7 = B* with Solder Dip
- 8 = B* with PIND Testing and Solder Dip
- 9 = Standard DDC Processing with Solder Dip, no Burn-In (See table below.)

Temperature Grade/Data Requirements:
- 1 = -55°C to +125°C
- 2 = -40°C to +85°C
- 3 = 0°C to +70°C
- 4 = -55°C to +125°C with Variables Test Data
- 5 = -40°C to +85°C with Variables Test Data
- 8 = 0°C to +70°C with Variables Test Data

*Standard DDC Processing with burn-in and full temperature test — see table below.

STANDARD DDC PROCESSING		
TEST	MIL-STD-883	
	METHOD(S)	CONDITION(S)
INSPECTION	2009, 2010, 2017, and 2032	—
SEAL	1014	A and C
TEMPERATURE CYCLE	1010	C
CONSTANT ACCELERATION	2001	A
BURN-IN	1015, Table 1	—

®Data Device Corporation

105 Wilbur Place, Bohemia, New York 11716-2482

For Technical Support - 1-800-DDC-5757 ext. 7420

Headquarters - Tel: (631) 567-5600 ext. 7420, Fax: (631) 567-7358
Southeast - Tel: (703) 450-7900, Fax: (703) 450-6610
West Coast - Tel: (714) 895-9777, Fax: (714) 895-4988
Europe - Tel: +44-(0)1635-811140, Fax: +44-(0)1635-32264
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