PROTEK DEVICES
ANALOG PRODUCTS DIVISION

PA4684
Dual SPDT Analog Switch

Features

- CMOS Technology for Bus and Analog Applications
- Low On-Resistance: 0.5Ω.
- Wide V_{CC} Range: 1.65V to 5.5V
- Rail-to-Rail Signal Range
- Control Input Over voltage Tolerance: 5.5V min.
- High Off Isolation: -42dB
- Crosstalk Rejection Reduces Signal Distortion: -70dB
- Low THD (0.05% @ V_{CC} = 2.7V)
- Break-Before-Make Switching
- Extended Industrial Temperature Range: –40°C to 85°C

Applications

- Cell Phones
- PDA's
- MP3 players
- Portable Instrumentation
- Speaker Headset Switching
- Power Routing
- Relay Replacement
- Audio and Video Signal Routing
- PCMCIA Cards
- Modems
- USB1.1

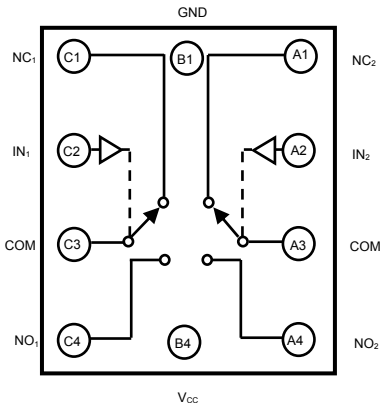
Description

ProTek Analog's PA4684 is a dual high-bandwidth, fast single-pole double throw (SPDT) CMOS switch. It can be used as an analog switch or as a low-delay bus switch. Specified over a wide operating power supply voltage, 1.65V to 5.5V, the PA4684 has a maximum On-Resistance of 0.5Ω at +2.7V.

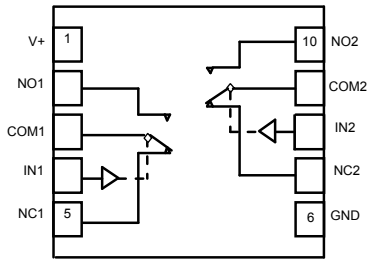
Break-before-make switching prevents both switches being enabled simultaneously. This eliminates signal disruption during switching.

The control input, INX, tolerates input drive signals up to 6.0V, independent of supply voltage.

Pin Configuration,



Flip Chip



DFN-10

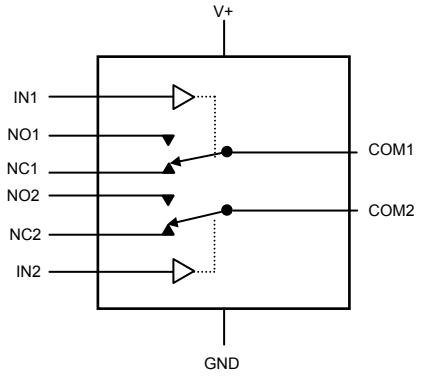
Pin Description

Pin # DFN	Pin # CSP	Name	Description
2,10	A4, C4	NOX	Data Port (Normally open)
6	B1	GND	Ground
5,7	A1, C1	NCX	Data Port (Normally closed)
3,9	A3, C3	COMX	Common Output / Data Port
1	B4	VCC	Positive Power Supply
4,8	A2, C2	INX	Logic Control

Logic Function Table

Logic Input (INX)	Function
0	NCX Connected to COMX
1	NOX Connected to COMX

Functional Diagram



Ordering Information

Temp Range	Package	Part Number
-40 to +85°C	Flip Chip 10 Bump	PA4684-T7
	DFN-10	PA4684DN

Absolute Maximum Ratings (1)

Supply Voltage VCC ..... –0.5V to +7V DC
Switch Voltage (VS)(2) .....–0.5V to VCC +0.5V DC Input Voltage (VIN)(2) ..... –0.5V to +7.0V
Continuous Current NO_NC_COM_ ..... ±500mA
Peak Current NO_NC_COM_ (pulsed at 1ms 50% duty cycle) .....±650mA
Peak Current NO_NC_COM_ (pulsed at 1ms 10% duty cycle) .....±800mA
Storage Temperature Range (TSTG) ....–65°C to +150°C
Junction Temperature under Bias (TJ) .....150°C
Junction Lead Temperature (TL) (Soldering, 10 seconds) .....260°C
Power Dissipation (PD) @ +85°C 250mW

Recommended Operating Conditions (3)

Supply Voltage Operating (V_{CC}) . . . .1.65V to 5.5V
Control Input Voltage (V_{IN}) . . . . . .0V to V_{CC}
Switch Input Voltage (V_{IN}) . . . . . .0V to V_{CC}
Output Voltage (V_{OUT}) . . . . . 0V to V_{CC}
Operating Temperature (T_A) . . . . . .–40°C to +85°C
Input Rise and Fall Time (t_r,t_f)
Control Input V_{CC} = 2.3V - 3.6V. . . . 0ns/V to 10ns/V
Control Input V_{CC} = 4.5V - 5.5V. . . . . 0ns/V to 5ns/V
Thermal Resistance (Θ_{JA}) . . . . 350°C/W
Lead Temperature (soldering 10s) . . . . . +300°C
Bump Temperature (soldering notes)
Infared (15s). . . . . +220°C
Vapor Phase (60ns) . . . . . +215°C

Notes:

1. "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.
2. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.
3. Control input must be held HIGH or LOW; it must not float.

DC Electrical Characteristics +3V Supply

(V_{CC} = 2.7V to 3.3V, T_A = -40 C to + 85 C, unless otherwise noted. Typical values are at 3V and +25°C.)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Analog Switch						
Analog Signal Range	V_{NO} , V_{NC} , V_{COM}		0		V_{CC}	V
NC On-Resistance	$R_{ON(NC)}$	V_{CC} = 2.7V, I_{COM} = 100mA, V_{NC} = 0 to V_{CC}		0.5	0.6	Ω
NO On-Resistance	$R_{ON(NO)}$	V_{CC} = 2.7V, I_{COM} = 100mA, V_{NC} = 0 to V_{CC}		0.4	0.5	
On-Resistance Match Between Channels	ΔR_{ON}	V_{CC} = 2.7V, I_{COM} = 100mA, V_{NO} or VNC = 1.5V		0.01	0.06	
NC On-Resistance Flatness	$R_{ONF(NC)}$	V_{CC} = 2.7V, I_{COM} = 100mA, V_{NC} = 0 to V_{CC}			0.25	
NO On-Resistance Flatness	$R_{ONF(NO)}$	V_{CC} = 2.7V, I_{COM} = 100mA, V_{NO} = 0 to V_{CC}			0.15	
NO or NC Off Leakage Current	$I_{OFF (NO)}$ or $I_{OFF (NC)}$	V_{CC} = 3.3V, V_{NO} or V_{NC} = 3V, 0.3V, V_{COM} = 0.3V, 3V	-80		80	nA
COM On Leakage Current	$I_{COM (ON)}$	V_{CC} = 3.3V, V_{NO} or V_{NC} = 3V, 0.3V, V_{COM} = 0.3V, 3V, or floating	-160		160	
Digital I/O						
Input Logic High	V_{IH}		1.3			V
Input Logic Low	V_{IL}				0.6	
Input Hysteresis	V_H	V_{CC} = 3.3V		200		mV
IN Input Leakage Current	I_{IN}	V_{IN} = 0 or V_{CC}	-1		1	µA
Power Supply						
Power-Supply Range	V_{CC}		1.65		5.5	V
Supply Current	I_{CC}	V_{CC} = 5.5V, V_{IN} = 0 or V_{CC}			200	nA

Switch and AC Characteristics

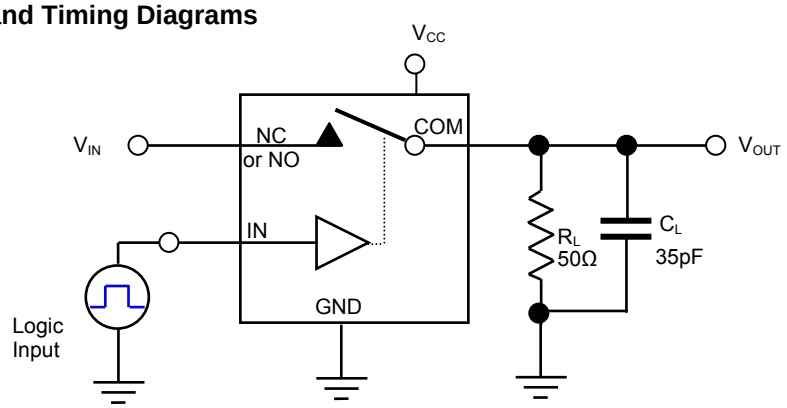
(Vcc = 2.7V to 3.3V, Ta = -40 C to +85 C, unless otherwise noted. Typical values are at 3V and +25°C

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Turn-On Time	t_{ON}	V_{CC} = 2.7V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF, *See Test Circuit Figure 1 & 2.*		25	60	ns
Turn-Off Time	t_{OFF}	V_{CC} = 2.7V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF, *See Test Circuit Figure 1 & 2.*		7	20	
Break-Before-Make Delay	t_{BBM}	V_{CC} = 2.7V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF, *See Test Circuit Figure 3.*		25		
Charge Injection	Q	COM = 0, R_S = 0, C_L = 1nF, *See Test Circuit Figure 4.*		54		pC
Off-Isolation	O_{IRR}	C_L = 5pF, R_L = 50Ω, f = 100kHz, V_{COM} = 1 V_{RMS}, , *See Test Circuit Figure 5.*		-42		dB
Crosstalk	X_{TALK}	C_L = 5pF, R_L = 50Ω, f = 100kHz, V_{COM} = 1 V_{RMS}, *See Test Circuit Figure 6.*		-70		
3dB Bandwidth	f_{3dB}	*See Test Circuit Figure 9.*		27		MHz
Total Harmonic Distortion	THD	R_L = 32Ω, V_{IN} = 3.5V, V_{CC} = 4.5V f = 20Hz to 20kHz		0.07		%
		R_L = 32Ω, V_{IN} = 2.0V, V_{CC} = 3.4V f = 20Hz to 20kHz		0.06		
		R_L = 32Ω, V_{IN} = 1.5V, V_{CC} = 2.7V f = 20Hz to 20kHz		0.05		

Capacitance

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
NC Off Capacitance	$C_{NC (OFF)}$	f = 1MHz, *See Test Circuit Figure 7.*		84		pF
NO Off Capacitance	$C_{NO (OFF)}$	f = 1MHz, *See Test Circuit Figure 7.*		65		
NC On Capacitance	$C_{NC (ON)}$	f = 1MHz, *See Test Circuit Figure 8.*		240		
NO On Capacitance	$C_{NO (ON)}$	f = 1MHz, *See Test Circuit Figure 8.*		225		

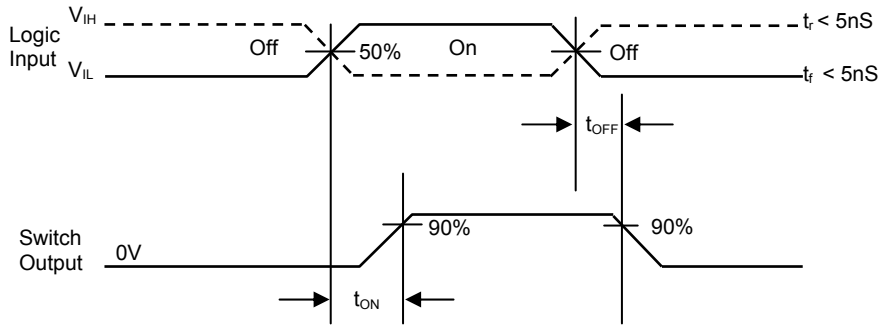
Test Circuits and Timing Diagrams



C_L includes fixture and stray capacitance

Figure 1. AC Test Circuit

Note1. Unused Input (NO or NC) must be grounded



Logic Input Waveforms inverted for Switches that have opposite logic

Figure2 AC Waveforms

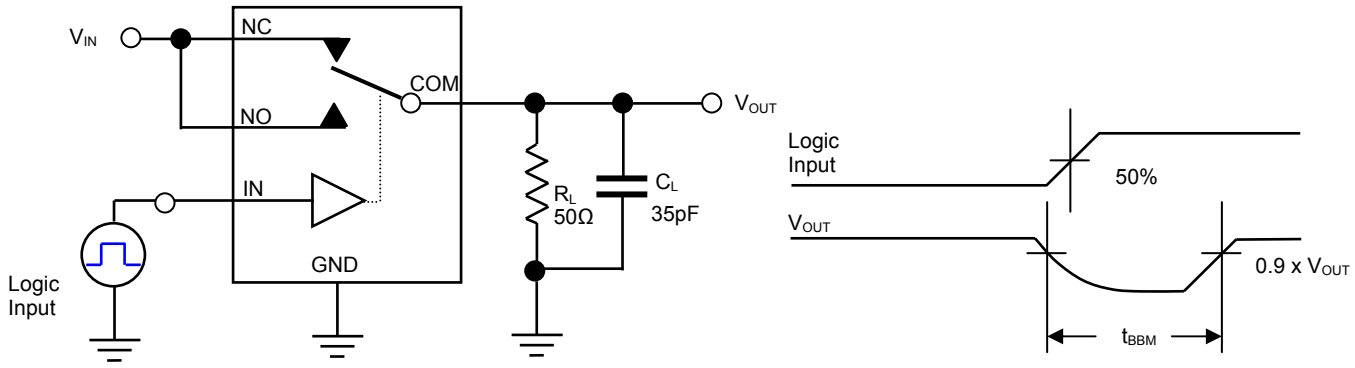


Figure 3. Break Before Make Interval Timing

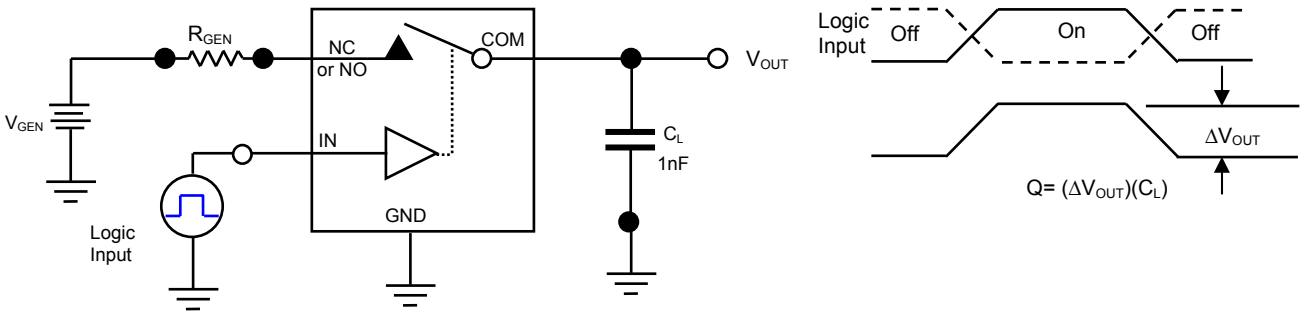


Figure 4. Charge Injection Test

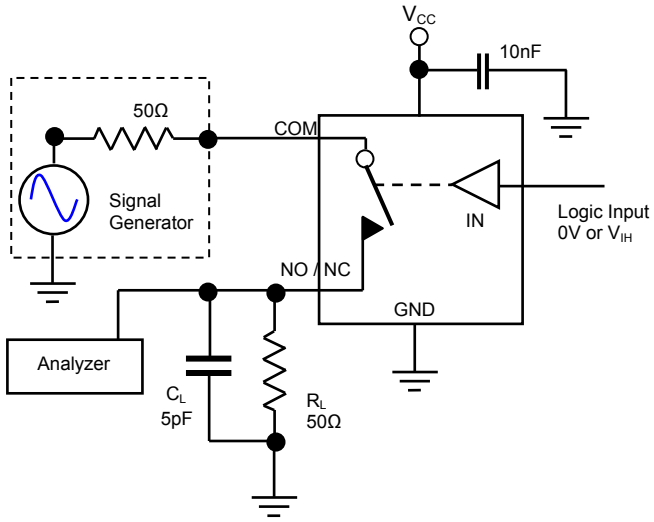


Figure 5. Off Isolation

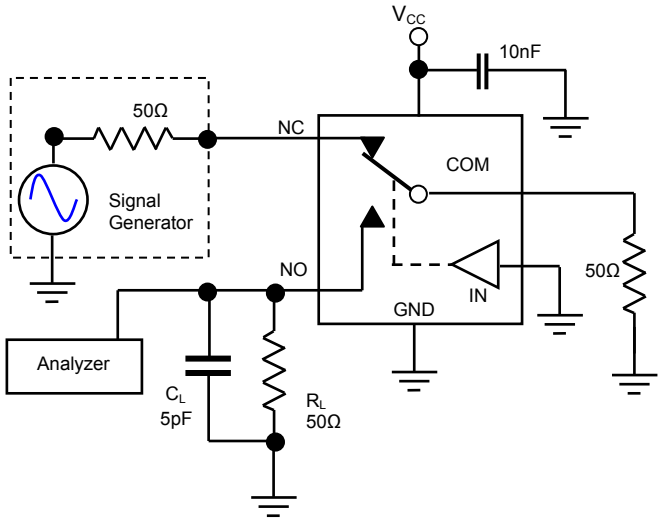


Figure 6. Crosstalk

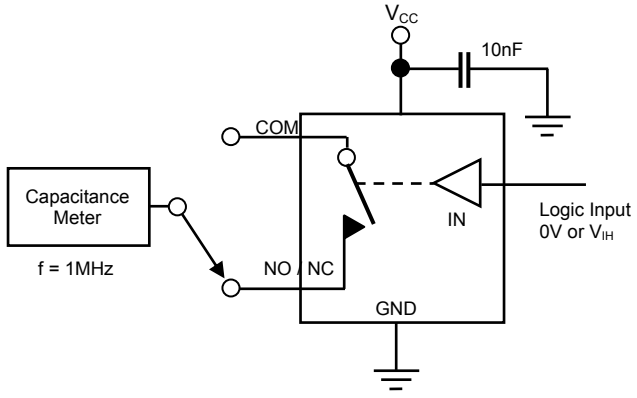


Figure 7. Channel Off Capacitance

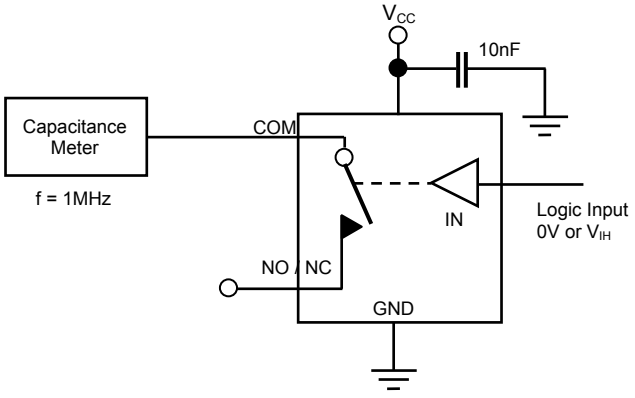


Figure 8. Channel On Capacitance

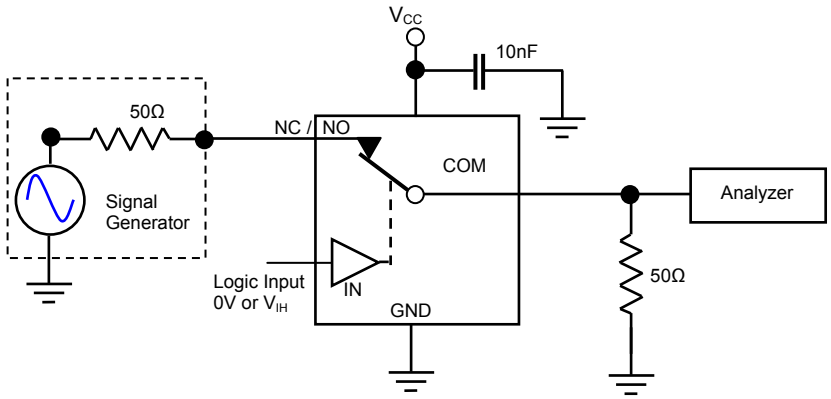
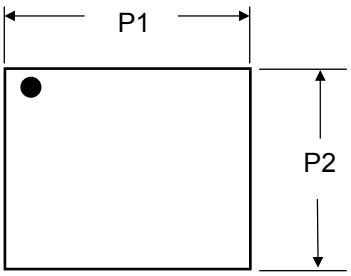
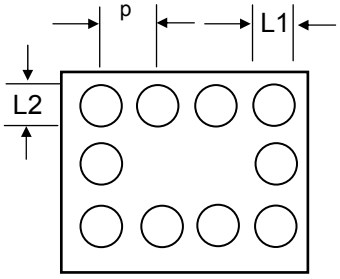


Figure 9. Bandwidth

Package Outline and Dimensions Flip-Chip 10-Bump

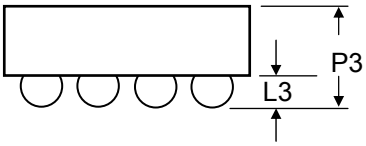


TOP VIEW

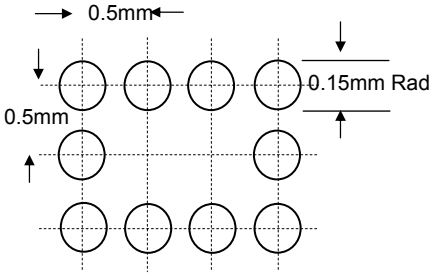


BOTTOM VIEW

Dim	MILLIMETERS		
	MIN	TYP	MAX
P1	1.98	2.00	2.02
P2	1.49	1.50	1.52
P3	0.68	0.71	0.75
L1	0.30	0.32	0.34
L2	0.30	0.32	0.34
L3	0.22	0.24	0.26
p	0.50	0.50	0.50

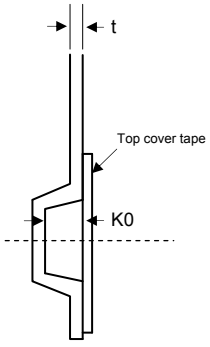


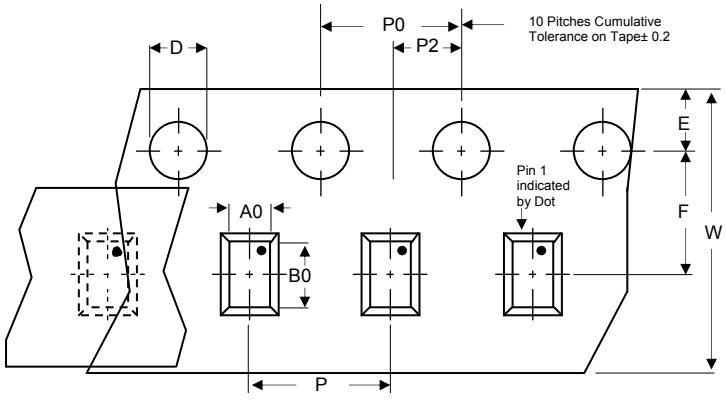
SIDE VIEW



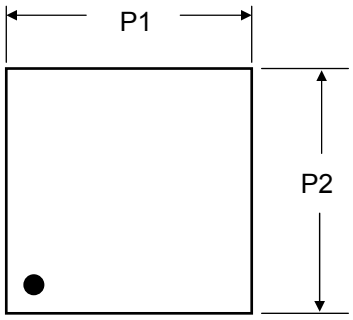
Tape and Reel Specifications

Reel Dia	A0	B0	K0	D	E	F	W	P0	P2	P	t-max
178 (7")	1.68±0.10	2.18±0.10	0.85±0.10	1.50±0.10	1.75±0.10	3.50±0.05	12.00±0.30	4.00±0.10	2.00±0.05	4.00±0.10	0.25

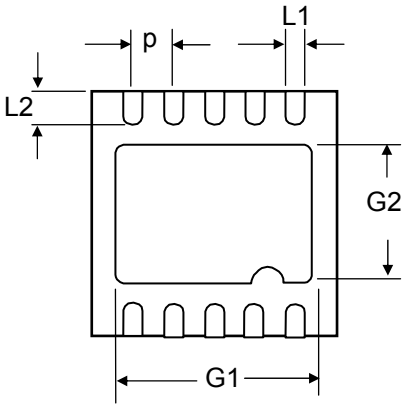




Package Outline and Dimensions DFN-10

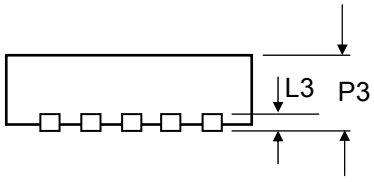


TOP VIEW

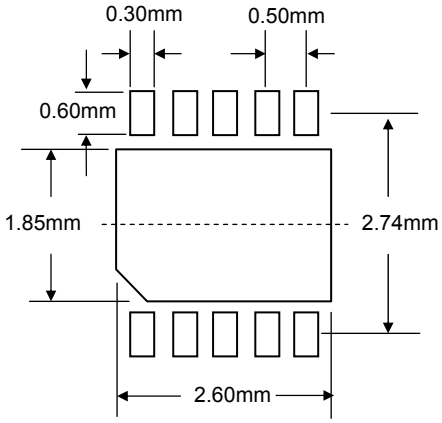


BOTTOM VIEW

Dim	MILLIMETERS		
	MIN	TYP	MAX
P1	2.95	3.00	3.05
P2	2.95	3.00	3.05
P3	0.80	0.85	0.85
L1	0.23	0.25	0.27
L2	0.35	0.40	0.45
L3	0.02	0.02	0.02
p	0.50	0.50	0.50
G1	2.35	2.40	2.45
G2	1.65	1.75	1.75



SIDE VIEW



Recommended Land Pattern

Tape and Reel Specifications

Reel Dia	A0	B0	K0	D	E	F	W	P0	P2	P	t-max
178 (7”)	3.00±0.10	3.00±0.10	0.85±0.10	1.50±0.10	1.75±0.10	3.50±0.05	12.00±0.30	4.00±0.10	2.00±0.05	4.00±0.10	0.25