# NCP5662, NCV5662

# Low Output Voltage, Ultra-Fast 2.0 A Low Dropout Linear Regulator with Enable

The NCP5662/NCV5662 is a high performance, low dropout linear regulator designed for high power applications that require up to 2.0 A current. It is offered in both fixed and adjustable output versions. With output voltages as low as 0.9 V and ultra−fast response times for load transients, the NCP5662/NCV5662 also provides additional features such as Enable and Error Flag (for the fixed output version), increasing the utility of these devices. A thermally robust, 5 pin $D^2PAK$ or DFN8 package, combined with an architecture that offers low ground current (independent of load), provides for a superior high−current LDO solution.

### Features

- Ultra−Fast Transient Response (Settling Time: 1−3 μs)
- Low Noise Without Bypass Capacitor (26 $\mu V_{rms}$)
- Low Ground Current Independent of Load (3.0 mA Maximum)
- Fixed/Adjustable Output Voltage Versions
- Enable Function
- Error Flag (Fixed Output Version)
- Current Limit Protection
- Thermal Shutdown Protection (160°C)
- 0.9 V Reference Voltage for Ultra−Low Output Operation
- Power Supply Rejection Ratio > 65 dB
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Controls
- These are Pb−Free Devices

### Applications

- Servers
- ASIC Power Supplies
- Post Regulation for Power Supplies
- Constant Current Source
- Networking Equipment
- Gaming and STB Modules

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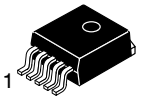
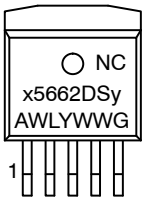
### MARKING DIAGRAMS AND PIN ASSIGNMENTS

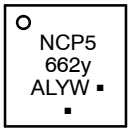



**$D^2PAK$**
**DS SUFFIX**
**CASE 936AA**




Tab = GND
Pin 1 = EN
2 = $V_{in}$
3 = GND
4 = $V_{out}$
5 = ADJ/EF


**DFN8**
**MN SUFFIX**
**CASE 488AF**




**Fixed Version**

Pin 1 = EF
2 = GND
3 = N/C
4 = EN
5, 6 = $V_{in}$
7, 8 = $V_{out}$

**Adjustable Version**

Pin 1 = ADJ
2 = GND
3 = N/C
4 = EN
5, 6 = $V_{in}$
7 = $V_{out}$
8 = N/C

x = P or V
y = A for Adjustable Version
B for Fixed 1.5 V Version
C for Fixed 3.3 V Version
D for Fixed 1.2 V Version
E for Fixed 1.8 V Version
F for Fixed 2.5 V Version
G for Fixed 2.8 V Version
H for Fixed 3.0 V Version
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G or ▪ = Pb−Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

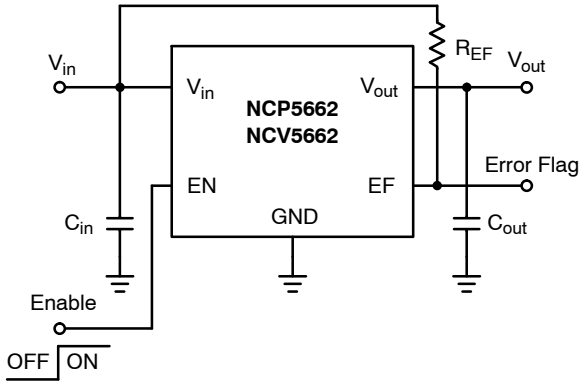



**Figure 1. Typical Application Schematic, Fixed Output**

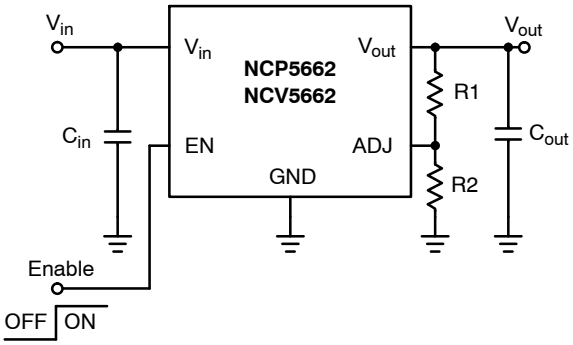



**Figure 2. Typical Application Schematic, Adjustable Output**

**PIN FUNCTION DESCRIPTION**

| Pin Adj/Fixed $D^2PAK$ | Pin Adj/Fixed DFN8 | Pin Name | Description |
|---|---|---|---|
| 1 | 4 | EN | Enable. This pin allows for on/off control of the regulator. To disable the device, connect to Ground. If this function is not in use, connect to $V_{in}$. |
| 2 | 5, 6* | $V_{in}$ | Positive Power Supply Input Voltage |
| 3, TAB | 2 | GND | Power Supply Ground |
| 4 | 7, 8 | $V_{out}$ | Regulated Output Voltage |
| 5 | 1 | ADJ (Adjustable Version) | This pin is connected to the resistor divider network and programs the output voltage. |
| 5 | 1 | EF (Fixed Version) | An Error Flag is triggered when the output voltage is out of regulation excluding transient signals that may occur. Requires a pullup resistor $\approx$ 100 kΩ. |
| – | 3, 8 | Pin 3 N/C on Fixed & ADJ Version while Pin 8 N/C on ADJ Version only | No connection. True no connect. PCB runs allowable. |
| – | EPAD | EPAD | Exposed thermal pad should be connected to ground. |

*Pins 5 and 6 must be connected together externally for output current full range operation.

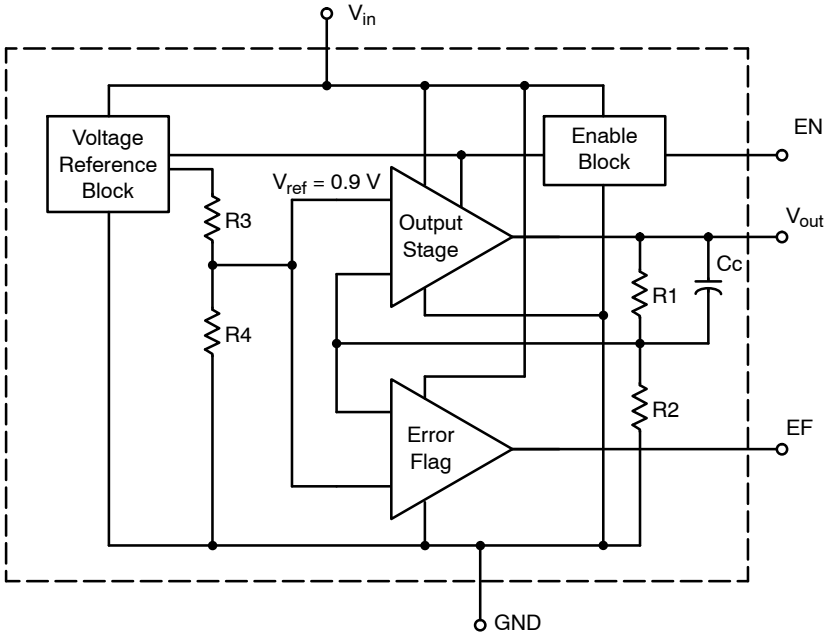



**Figure 3. Block Diagram, Fixed Output**

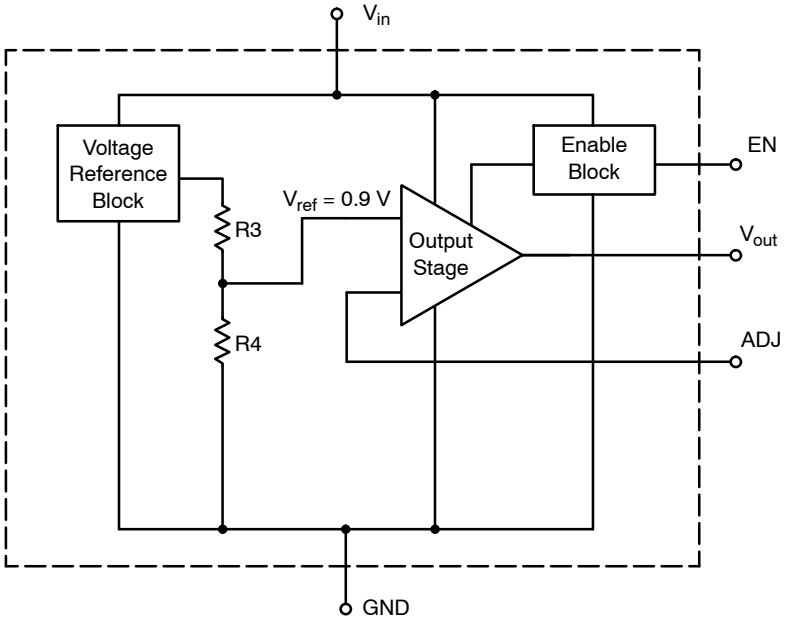



**Figure 4. Block Diagram, Adjustable Output**

## ABSOLUTE MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Input Voltage (Note 1) | $V_{in}$ | 18 | V |
| Output Pin Voltage | $V_{out}$ | −0.3 to (Vin +0.3) | V |
| Adjust Pin Voltage | $V_{ADJ}$ | −0.3 to (Vin +0.3) | V |
| Enable Pin Voltage | $V_{EN}$ | −0.3 to (Vin +0.3) | V |
| Error Flag Voltage | $V_{EF}$ | −0.3 to (Vin +0.3) | V |
| Error Flag Current | $I_{EF}$ | 3.0 | mA |
| Maximum Junction Temperature | $T_{J(max)}$ | 150 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTE: This device series contains ESD protection and exceeds the following tests:
Human Body Model (HBM), Class 3A, 2000 V
Machine Model (MM), Class C, 200 V
Charge Device Model (CDM), Class IV, 2000 V.

1. Refer to Electrical Characteristics and Application Information for Safe Operating Area.

## THERMAL CHARACTERISTICS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Characteristics, $D^2PAK$ (Notes 1 and 2)<br>Thermal Resistance, Junction−to−Ambient<br>Thermal Resistance, Junction−to−Case<br>Thermal Reference, Junction−to−Lead | <br>$R_{\theta JA}$<br>$R_{\theta JC}$<br>$R_{\Psi JL}$ | <br>45<br>5.0<br>7.0 | °C/W |
| Thermal Characteristics, DFN8 (Notes 1 and 2)<br>Thermal Resistance, Junction−to−Ambient<br>Thermal Reference, Junction−to−Lead (Note 3) | <br>$R_{\theta JA}$<br>$R_{\Psi JL}$ | <br>78<br>14 | °C/W |

2. As measured using a copper heat spreading area of 1 sq in copper, 1 oz copper thickness.
3. Lead 6.

## OPERATING RANGES

| Rating | | Symbol | Value | Unit |
|---|---|---|---|---|
| Operating Input Voltage (Note 1) | | $V_{in}$ | ($V_{out}$+$V_{DO}$), 2 to 9 (Note 4) | V |
| Operating Ambient Temperature Range | NCP5662<br>NCV5662 | $T_A$ | −40 to +85<br>−40 to +125 | °C |
| Storage Temperature Range | | $T_{stg}$ | −55 to +150 | °C |

4. Minimum $V_{in}$ = ($V_{out}$ + $V_{DO}$) or 2 V, whichever is higher.

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = $V_{out}$ + 1.5 V, for typical values $T_A$ = 25°C, for min/max values $T_A$ = −40°C to 85°C (NCP version), $T_A$ = −40°C to 125°C (NCV version), $C_{in}$ = $C_{out}$ = 150 μF unless otherwise noted. (Note 5))

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **ADJUSTABLE OUTPUT VERSION** | | | | | |
| Output Noise Voltage | $V_n$ | – | 26 | – | $\mu V_{rms}$ |
| Output Voltage<br>$T_A$ = 25°C ($V_{in}$ = $V_{out}$ +1.5 V to 7.0 V, $I_{out}$ = 10 mA to 2.0 A)<br>$T_A$ = −20 to +125°C ($V_{in}$ = $V_{out}$ +1.5 V to 7.0 V, $I_{out}$ = 10 mA to 2.0 A)<br>$T_A$ = −40 to +150°C ($V_{in}$ = $V_{out}$ +1.5 V to 7.0 V, $I_{out}$ = 10 mA to 2.0 A) | $V_{out}$ | <br>(−1%)<br>(−1.5%)<br>(−2%) | <br>–<br>0.9<br>– | <br>(+1%)<br>(+1.5%)<br>(+2%) | V |
| Adjustable Pin Input Current | $I_{ADJ}$ | – | 40 | – | nA |
| Line Regulation ($I_{out}$ = 10 mA, $V_{out}$+1.5 V < $V_{in}$ < 7.0 V) | $REG_{line}$ | – | 0.03 | – | % |
| Load Regulation (10 mA < $I_{out}$ < 2.0 A) | $REG_{load}$ | – | 0.03 | – | % |
| Dropout Voltage ($I_{out}$ = 2.0 A) | $V_{DO}$ | – | 1.0 | 1.3 | V |
| Peak Output Current Limit | $I_{out(peak)}$ | 2.0 | – | – | A |
| Internal Current Limitation | $I_{LIM}$ | – | 3.0 | – | A |
| Ripple Rejection (120 Hz)<br>Ripple Rejection (1 kHz) | RR | –<br>– | 70<br>65 | –<br>– | dB |
| Ground Current<br>$I_{out}$ = 2.0 A<br>Disabled State | <br>$I_{GND}$<br>$I_{GND(DIS)}$ | <br>–<br>– | <br>1.3<br>10 | <br>3.0<br>300 | <br>mA<br>μA |
| Enable Input Threshold Voltage<br>Voltage Increasing, On state, Logic High<br>Voltage Decreasing, Off state, Logic Low | $V_{EN}$ | <br>1.3<br>– | <br>–<br>– | <br>–<br>0.3 | V |
| Enable Input Current<br>Enable Pin Voltage = 0.3 $V_{max}$<br>Enable Pin Voltage = 1.3 $V_{min}$ | $I_{EN}$ | <br>–<br>– | <br>0.5<br>0.5 | <br>–<br>– | μA |

5. Performance guaranteed over specified operating conditions by design, guard banded test limits, and/or characterization, production tested at $T_J$ = $T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = $V_{out}$ + 1.5 V, for typical values $T_A$ = 25°C, for min/max values $T_A$ = −40°C to 85°C (NCP version), $T_A$ = −40°C to 125°C (NCV version), $C_{in}$ = $C_{out}$ = 150 μF unless otherwise noted. (Note 6))

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **FIXED OUTPUT VOLTAGE** | | | | | |
| Output Noise Voltage ($V_{out}$ = 0.9 V) | $V_n$ | – | 26 | – | $\mu V_{rms}$ |
| Output Voltage (Note 7)<br>$T_A$ = 25°C ($V_{in}$ = $V_{out}$ +1.5 V to 7.0 V, $I_{out}$ = 10 mA to 2.0 A)<br>$T_A$ = −20 to +125°C ($V_{in}$ = $V_{out}$ +1.5 V to 7.0 V, $I_{out}$ = 10 mA to 2.0 A)<br>$T_A$ = −40 to +150°C ($V_{in}$ = $V_{out}$ +1.5 V to 7.0 V, $I_{out}$ = 10 mA to 2.0 A) | $V_{out}$ | <br>(−1%)<br>(−1.5%)<br>(−2%) | <br>–<br>$V_{out(nom)}$<br>– | <br>(+1%)<br>(+1.5%)<br>(+2%) | V |
| Line Regulation ($I_{out}$ = 10 mA, $V_{out}$+1.5 V < $V_{in}$ < 7.0 V) | $REG_{line}$ | – | 0.03 | – | % |
| Load Regulation (10 mA < $I_{out}$ < 2.0 A) | $REG_{load}$ | – | 0.2 | – | % |
| Dropout Voltage ($I_{out}$ = 2.0 A) | $V_{DO}$ | – | 1.0 | 1.3 | V |
| Peak Output Current Limit | $I_{out(peak)}$ | 2.0 | – | – | A |
| Internal Current Limitation | $I_{LIM}$ | – | 3.0 | – | A |
| Ripple Rejection (120 Hz)<br>Ripple Rejection (1 kHz) | RR | –<br>– | 70<br>65 | –<br>– | dB |
| Ground Current<br>$I_{out}$ = 2.0 A<br>Disabled State | <br>$I_{GND}$<br>$I_{GND(DIS)}$ | <br>–<br>– | <br>1.3<br>30 | <br>3.0<br>300 | <br>mA<br>μA |
| Enable Input Threshold Voltage<br>Voltage Increasing, On state, Logic High<br>Voltage Decreasing, Off state, Logic Low | $V_{EN}$ | <br>1.3<br>– | <br>–<br>– | <br>–<br>0.3 | V |
| Enable Input Current<br>Enable Pin Voltage = 0.3 $V_{max}$<br>Enable Pin Voltage = 1.3 $V_{min}$ | $I_{EN}$ | <br>–<br>– | <br>0.5<br>0.5 | <br>–<br>– | μA |
| Error Flag Voltage Threshold (Fixed Output) | $V_{EF(VT)}$ | 91 | 94 | 97 | % of $V_{out}$ |
| Error Flag Output Low Voltage Saturation ($I_{EF}$ = 1.0 mA) | $V_{EF(SAT)}$ | – | 200 | – | mV |
| Error Flag Leakage | $I_{EF(leakage)}$ | – | 1.0 | – | μA |
| Error Flag Blanking Time (Note 8) | $t_{EF}$ | – | 50 | – | μs |

6. Performance guaranteed over specified operating conditions by design, guard banded test limits, and/or characterization, production tested at $T_J$ = $T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
7. Fixed output voltage available at 0.9 V per request.
8. Can be disabled per customer request.

## TYPICAL CHARACTERISTICS

(Typical characteristics were measured with the same conditions as electrical characteristics, unless otherwise noted)

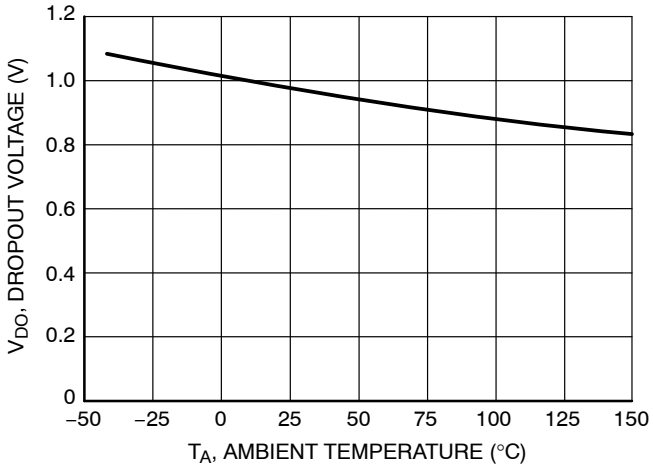



**Figure 5. Dropout Voltage vs. Temperature**

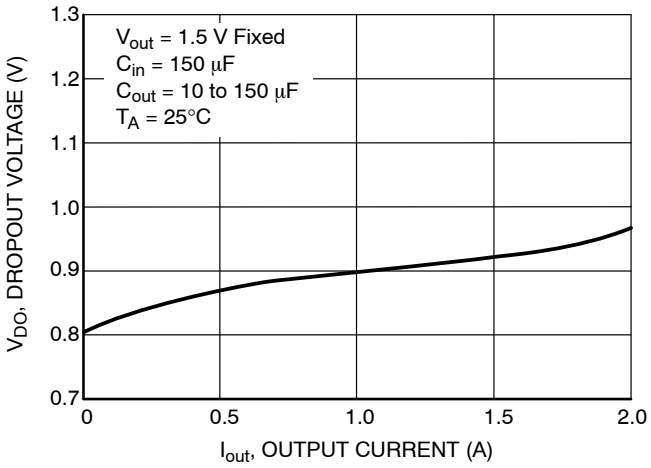



**Figure 6. 1.5 V Dropout Voltage vs. Output Current**

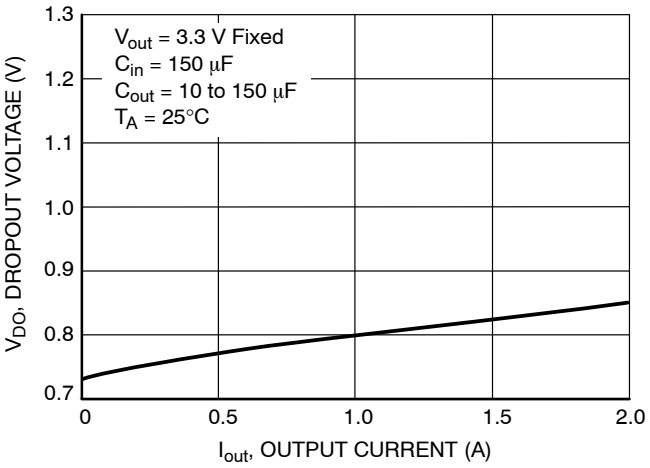



**Figure 7. 3.3 V Dropout Voltage vs. Output Current**

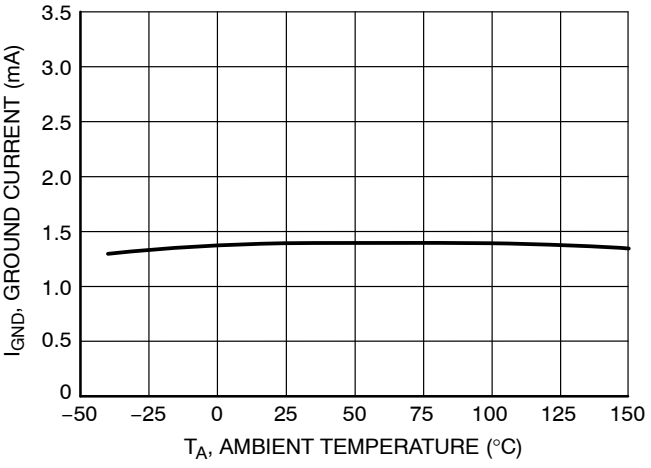



**Figure 8. Ground Current vs. Temperature**

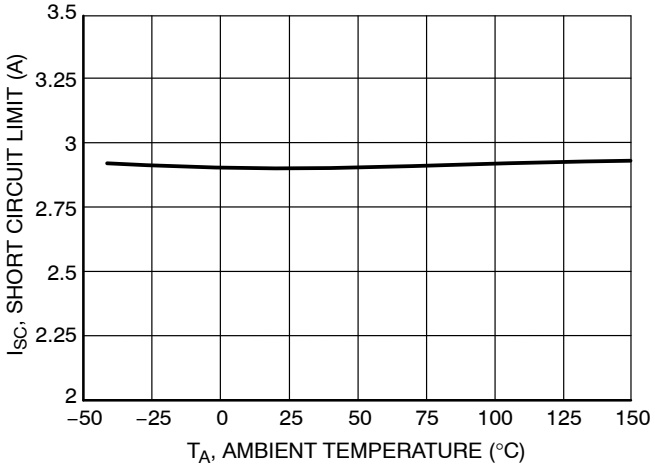



**Figure 9. Short Circuit Current Limit vs. Temperature**

## TYPICAL CHARACTERISTICS

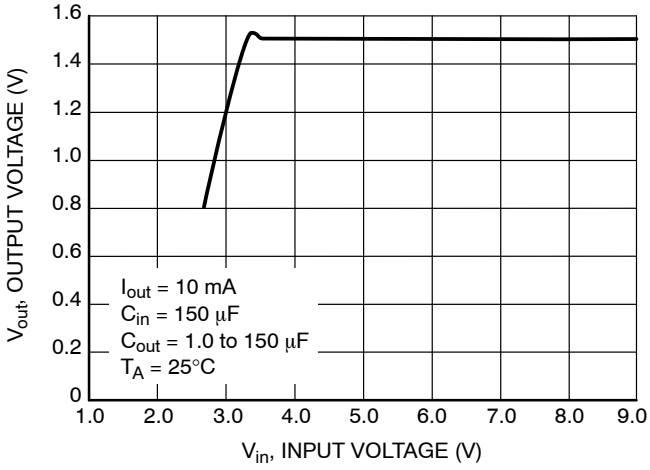



**Figure 10. 1.5 V Output Voltage vs. Input Voltage**

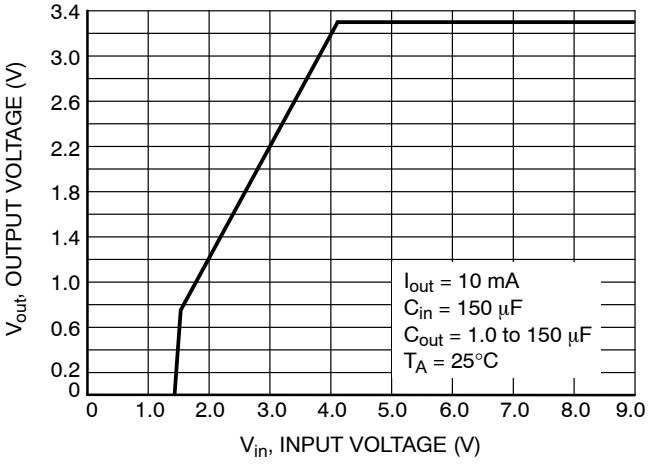



**Figure 11. 3.3 V Output Voltage vs. Input Voltage**

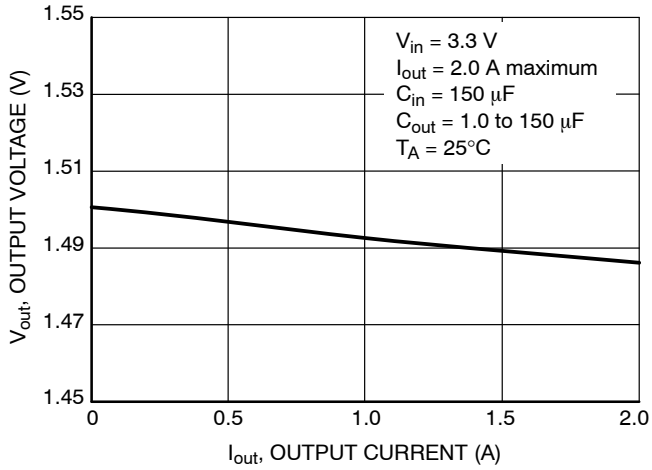



**Figure 12. 1.5 V Output Voltage vs. Output Load Current**

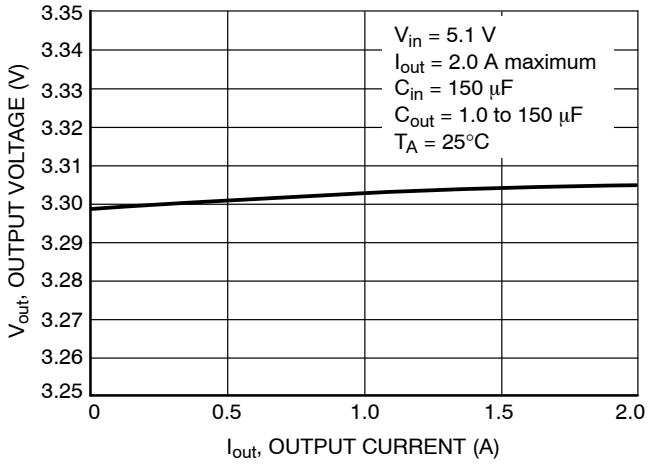



**Figure 13. 3.3 V Output Voltage vs. Output Load Current**

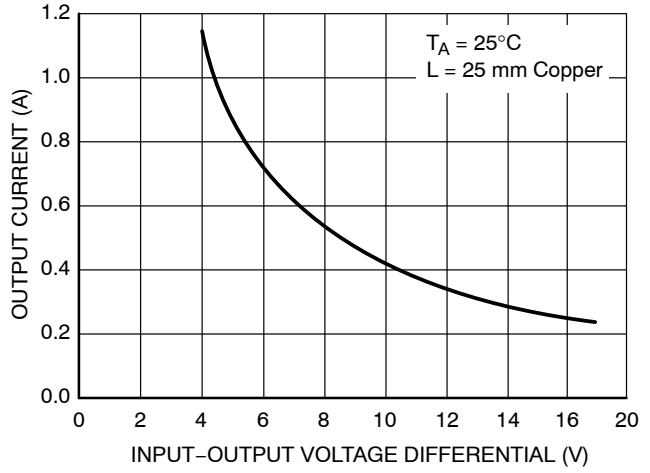



**Figure 14. Output Current vs. Input−Output Voltage Differential**

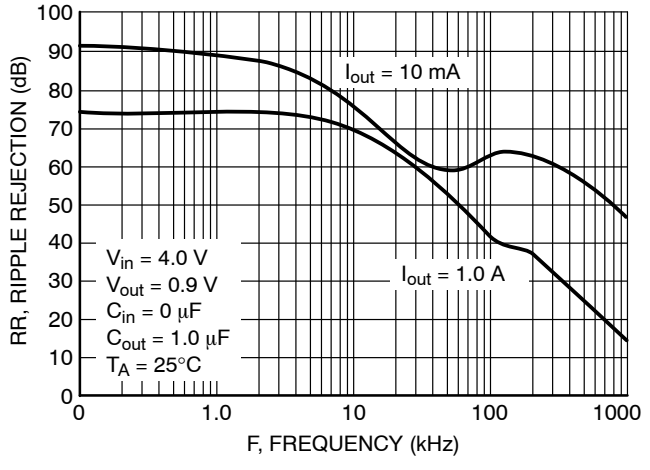



**Figure 15. Ripple Rejection vs. Frequency**

## TYPICAL CHARACTERISTICS

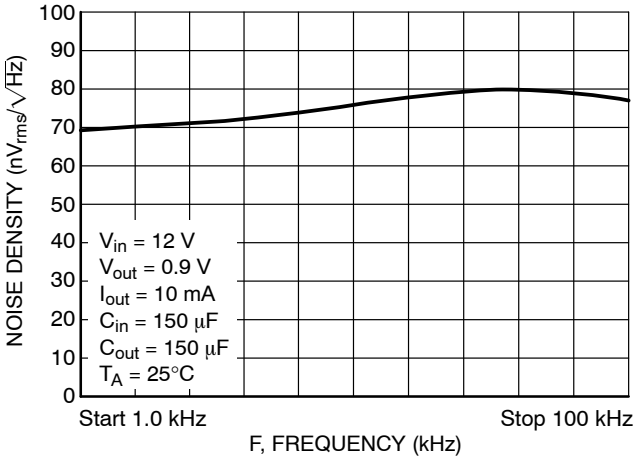



**Figure 16. Noise Density vs. Frequency**

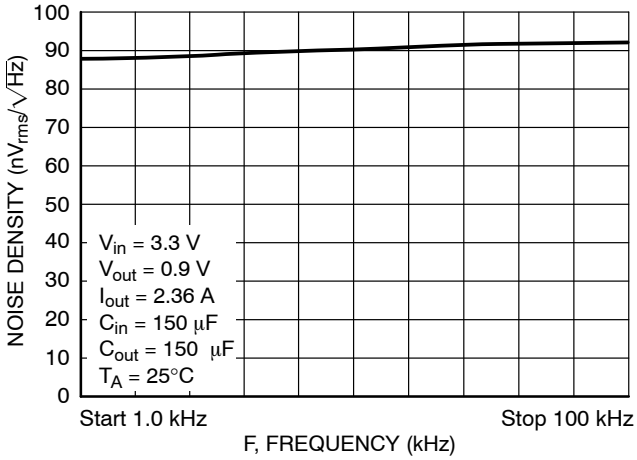



**Figure 17. Noise Density vs. Frequency**

## TYPICAL CHARACTERISTICS

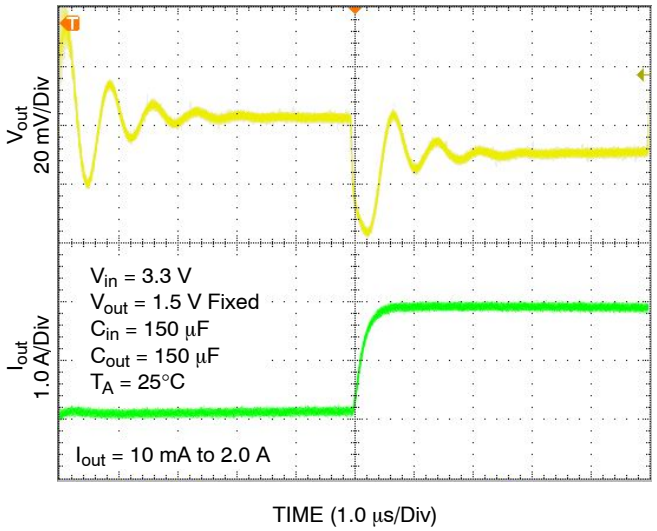



**Figure 18. Load Transient Response**

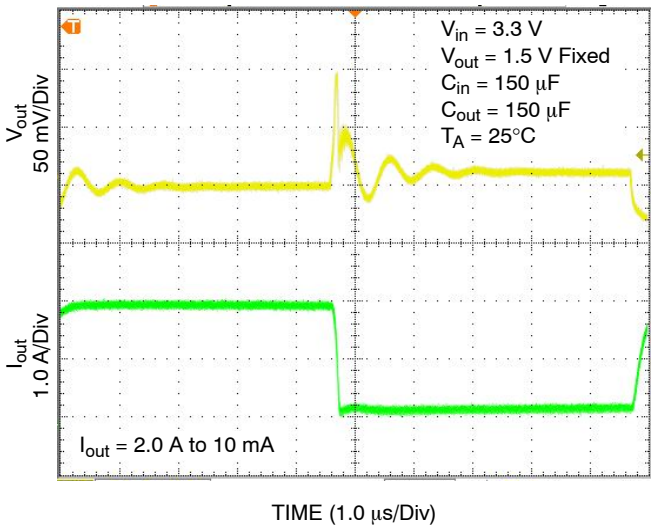



**Figure 19. Load Transient Response**

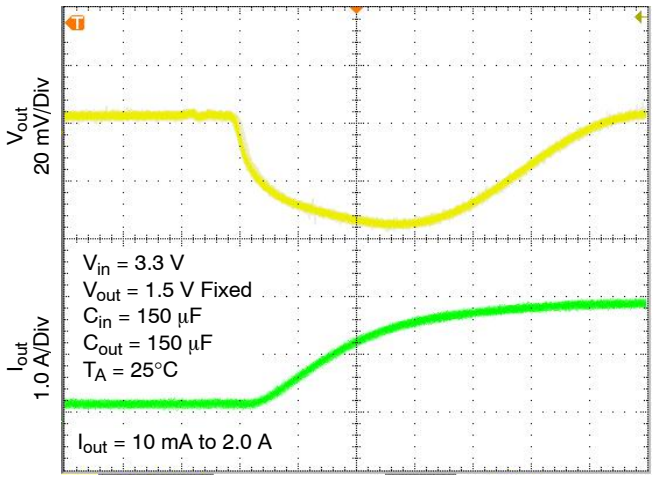



**Figure 20. Load Transient Response**

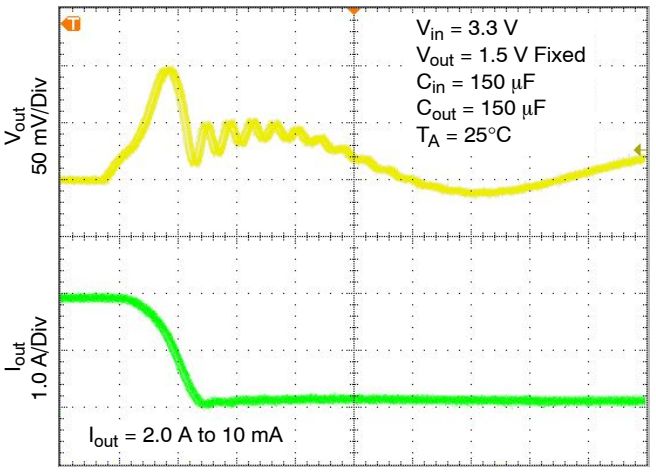



**Figure 21. Load Transient Response**

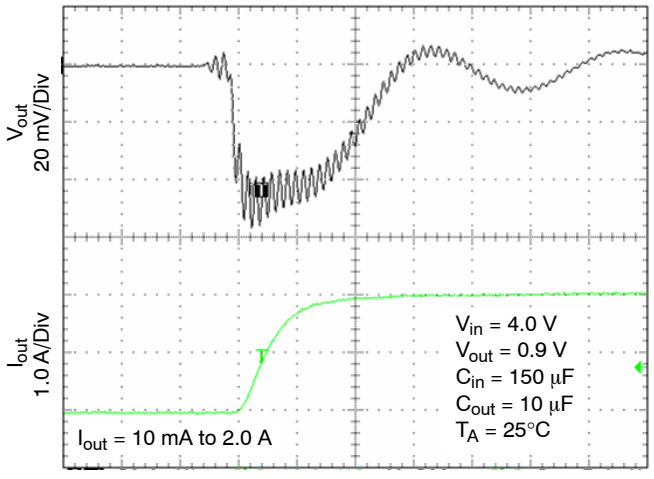



**Figure 22. Load Transient Response**

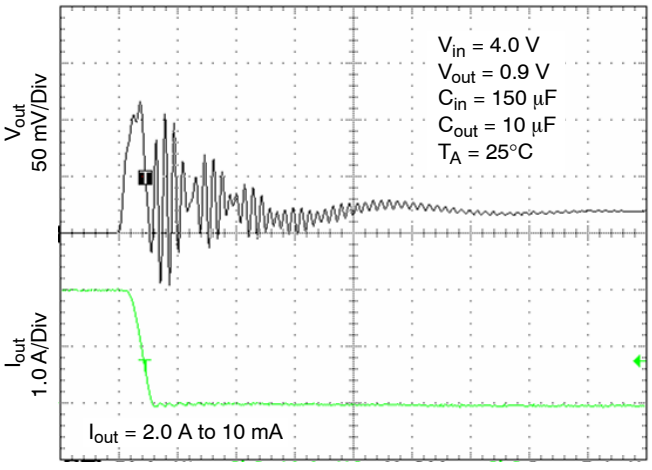



**Figure 23. Load Transient Response**

## APPLICATION INFORMATION

The NCP5662 is a high performance low dropout 2.0 A linear regulator suitable for high power applications, featuring an ultra−fast response time and low noise without a bypass capacitor. It is offered in both fixed and adjustable output versions with voltages as low as 0.9 V. Additional features, such as Enable and Error Flag (fixed output version) increase the utility of the NCP5662. It is thermally robust and includes the safety features necessary during a fault condition, which provide for an attractive high current LDO solution for server, ASIC power supplies, networking equipment applications, and many others.

### Input Capacitor

The recommended input capacitor value is a 150 μF OSCON with an Equivalent Series Resistance (ESR) of 50 mΩ. It is especially required if the power source is located more than a few inches from the NCP5662. This capacitor will reduce device sensitivity and enhance the output transient response time. The PCB layout is very important and in order to obtain the optimal solution, the Vin and GND traces should be sufficiently wide to minimize noise and unstable operation.

### Output Capacitor

Proper output capacitor selection is required to maintain stability. The NCP5662 is guaranteed to be stable at an output capacitance of, $C_{out}$ > 10 μF with an ESR < 300 mΩ over the output current range of 10 mA to 2.0 A. For PCB layout considerations, place the recommended ceramic capacitor close to the output pin and keep the leads short. This should help ensure ultra−fast transient response times.

### Adjustable Output Operation

The application circuit for the adjustable output version is shown in Figure 2. The reference voltage is 0.9 V and the adjustable pin current is typically 40 nA. A resistor divider network, R1 and R2, is calculated using the following formula:

$$R1 = R2\left(\frac{V_{out}}{V_{ref}} - 1\right)$$

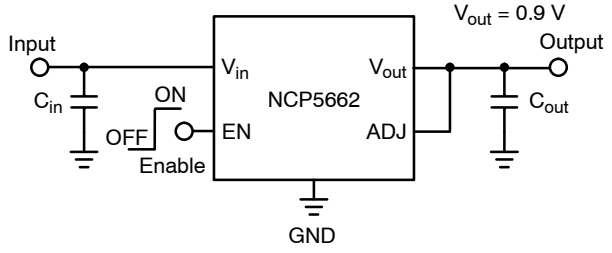



**Figure 24. To achieve the minimum output voltage, ADJ to $V_{out}$ has to be connected together**

### Current Limit Operation

As the peak output current increases beyond its limitation, the device is internally clampled to 3.0 A, thus causing the output voltage to decrease and go out of regulation. This allows the device never to exceed the maximum power dissipation.

### Error Flag Operation

The Error Flag pin on the NCP5662 will produce a logic Low when it drops below the nominal output voltage. Refer to the electrical characteristics for the threshold values at which point the Error Flag goes Low. When the NCP5662 is above the nominal output voltage, the Error Flag will remain at logic High.

The external pullup resistor needs to be connected between $V_{in}$ and the Error Flag pin. A resistor of approximately 100 kΩ is recommended to minimize the current consumption. No pullup resistor is required if the Error Flag output is not being used.

### Thermal Consideration

The maximum package power dissipation is:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The bipolar process employed for this IC is fully characterized and rated for reliable 18 V operation. To avoid damaging the part or degrading it's reliability, power dissipation transients should be limited to under 30 W for $D^2PAK$. For open−circuit to short−circuit transient, $P_{DTransient} = V_{in(operating\ max)} * I_{SC}$.

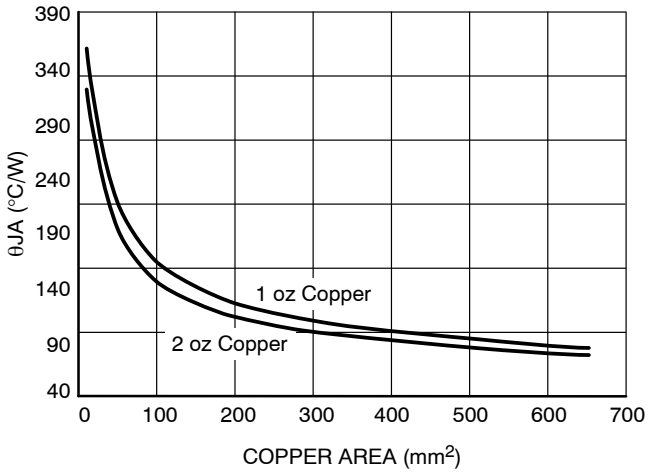



**Figure 25. DFN8 Thermal Resistance vs. Copper Area**

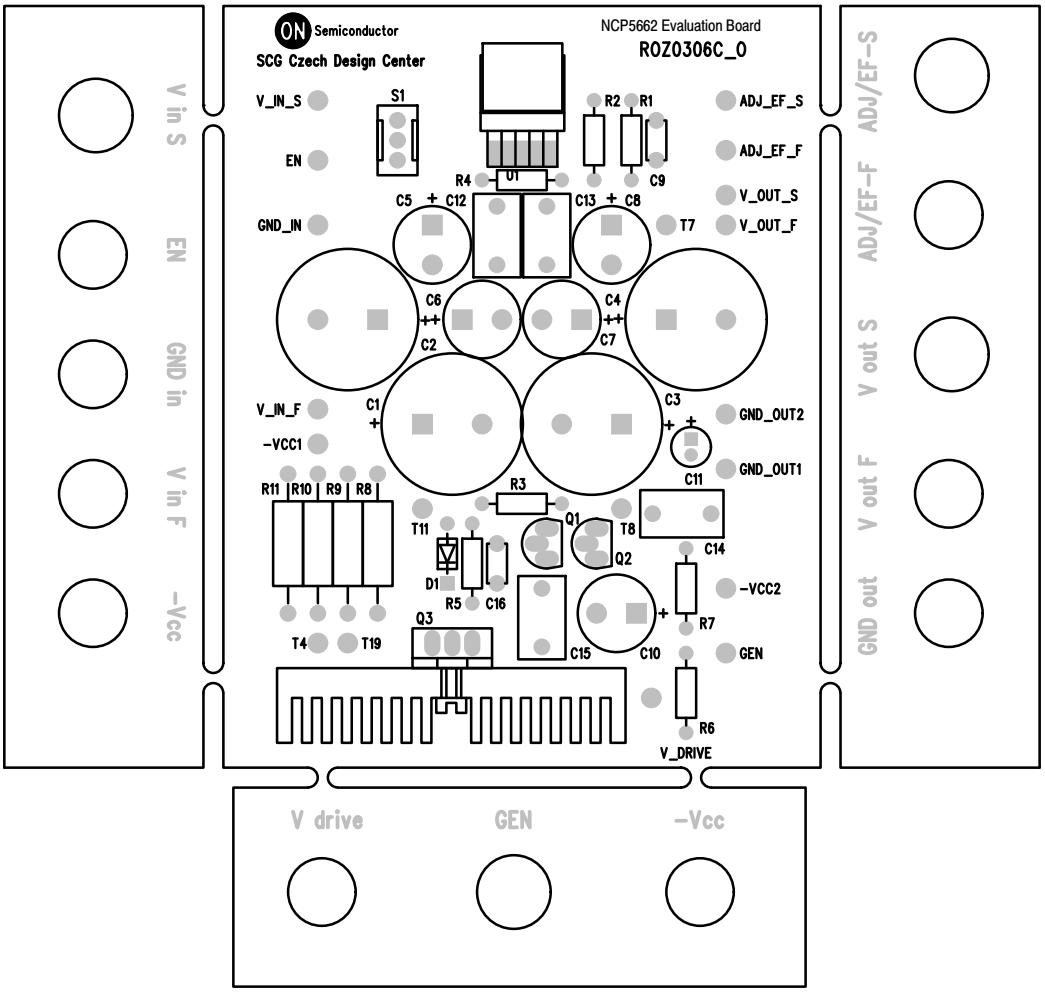



**Figure 26. Test Board used for Evaluation**

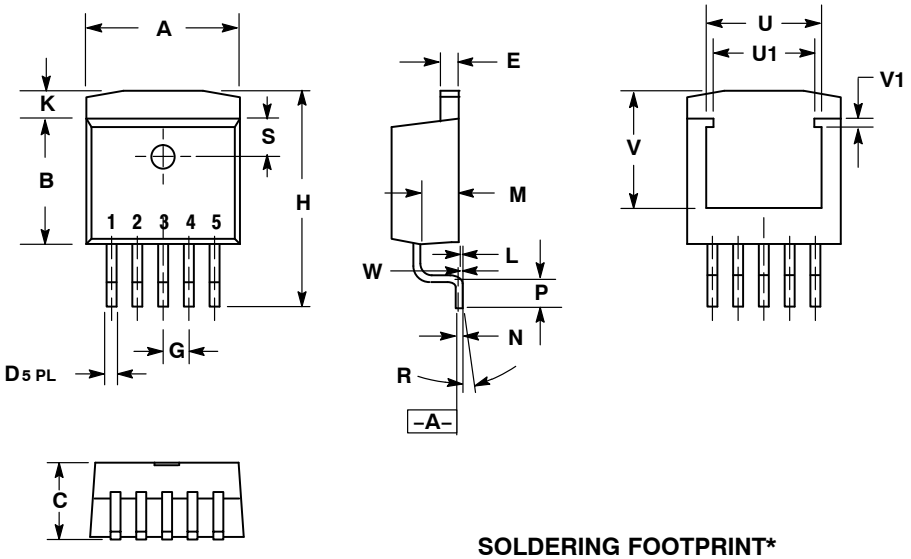
**ORDERING INFORMATION**

| Device | Nominal Output Voltage | Package | Shipping† |
|---|---|---|---|
| NCP5662DSADJR4G | Adj (Pb−Free) | D$^2$PAK | 800/Tape & Reel |
| NCP5662DS12R4G | Fixed, 1.2 V (Pb−Free) | | |
| NCP5662DS15R4G | Fixed, 1.5 V (Pb−Free) | | |
| NCP5662DS18R4G | Fixed, 1.8 V (Pb−Free) | | |
| NCP5662DS25R4G | Fixed, 2.5 V (Pb−Free) | | |
| NCP5662DS28R4G | Fixed, 2.8 V (Pb−Free) | | |
| NCP5662DS30R4G | Fixed, 3.0 V (Pb−Free) | | |
| NCP5662DS33R4G | Fixed, 3.3 V (Pb−Free) | | |
| NCV5662DSADJR4G | Adj (Pb−Free) | | |
| NCV5662DS15R4G | Fixed, 1.5 V (Pb−Free) | | |
| NCP5662MNADJR2G | Adj (Pb−Free) | DFN8 | 3000/Tape & Reel |
| NCP5662MN15R2G | Fixed, 1.5 V (Pb−Free) | | |
| NCP5662MN33R2G | Fixed, 3.3 V (Pb−Free) | | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## PACKAGE DIMENSIONS

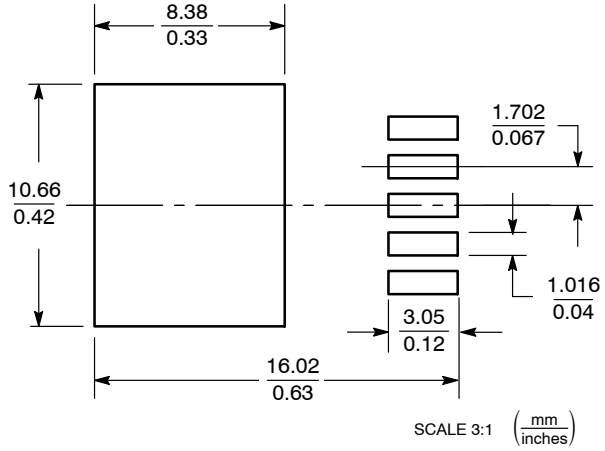
**D²PAK 5−LEAD**
CASE 936AA−01
ISSUE B




NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH AND METAL BURR.
4. PACKAGE OUTLINE EXCLUSIVE OF PLATING THICKNESS.
5. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A AND LEAD SURFACE.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.396 | 0.406 | 10.05 | 10.31 |
| B | 0.330 | 0.340 | 8.38 | 8.64 |
| C | 0.170 | 0.180 | 4.31 | 4.57 |
| D | 0.026 | 0.035 | 0.66 | 0.91 |
| E | 0.045 | 0.055 | 1.14 | 1.40 |
| G | 0.067 BSC | | 1.70 BSC | |
| H | 0.539 | 0.579 | 13.69 | 14.71 |
| K | 0.055 | 0.066 | 1.40 | 1.68 |
| L | 0.000 | 0.010 | 0.00 | 0.25 |
| M | 0.098 | 0.108 | 2.49 | 2.74 |
| N | 0.017 | 0.023 | 0.43 | 0.58 |
| P | 0.058 | 0.078 | 1.47 | 1.98 |
| R | 0 ° | 8 ° | 0 ° | 8 ° |
| S | 0.095 | 0.105 | 2.41 | 2.67 |
| U | 0.296 | 0.304 | 7.52 | 7.72 |
| U1 | 0.265 | 0.272 | 6.72 | 6.92 |
| V | 0.296 | 0.300 | 7.53 | 7.63 |
| V1 | 0.040 | 0.044 | 1.01 | 1.11 |
| W | 0.010 | | 0.25 | |

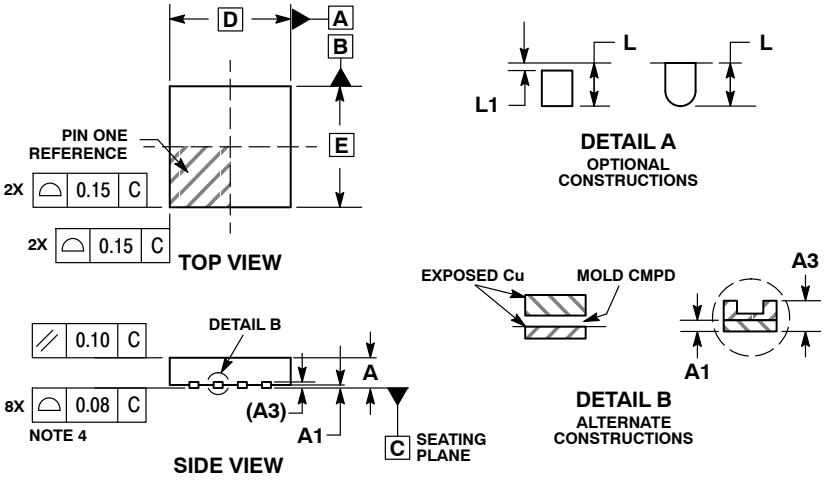
### SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

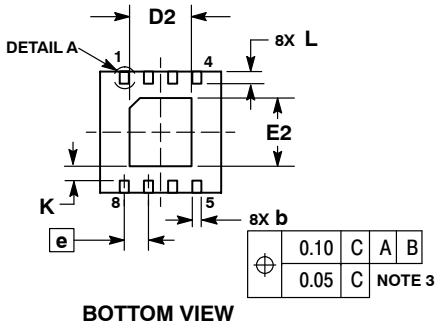
## PACKAGE DIMENSIONS

**8 PIN DFN, 4x4**
CASE 488AF−01
ISSUE C

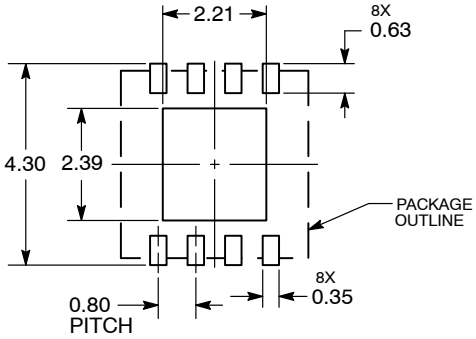



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DETAILS A AND B SHOW OPTIONAL CONSTRUCTIONS FOR TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.25 | 0.35 |
| D | 4.00 BSC | |
| D2 | 1.91 | 2.21 |
| E | 4.00 BSC | |
| E2 | 2.09 | 2.39 |
| e | 0.80 BSC | |
| K | 0.20 | −−− |
| L | 0.30 | 0.50 |
| L1 | −−− | 0.15 |




### SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

The products described herein (NCP5662/NCV5662), may be covered by one or more of the following U.S. patents: 5,920,184; 5,834,926. There may be other patents pending.



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