

MB86H01

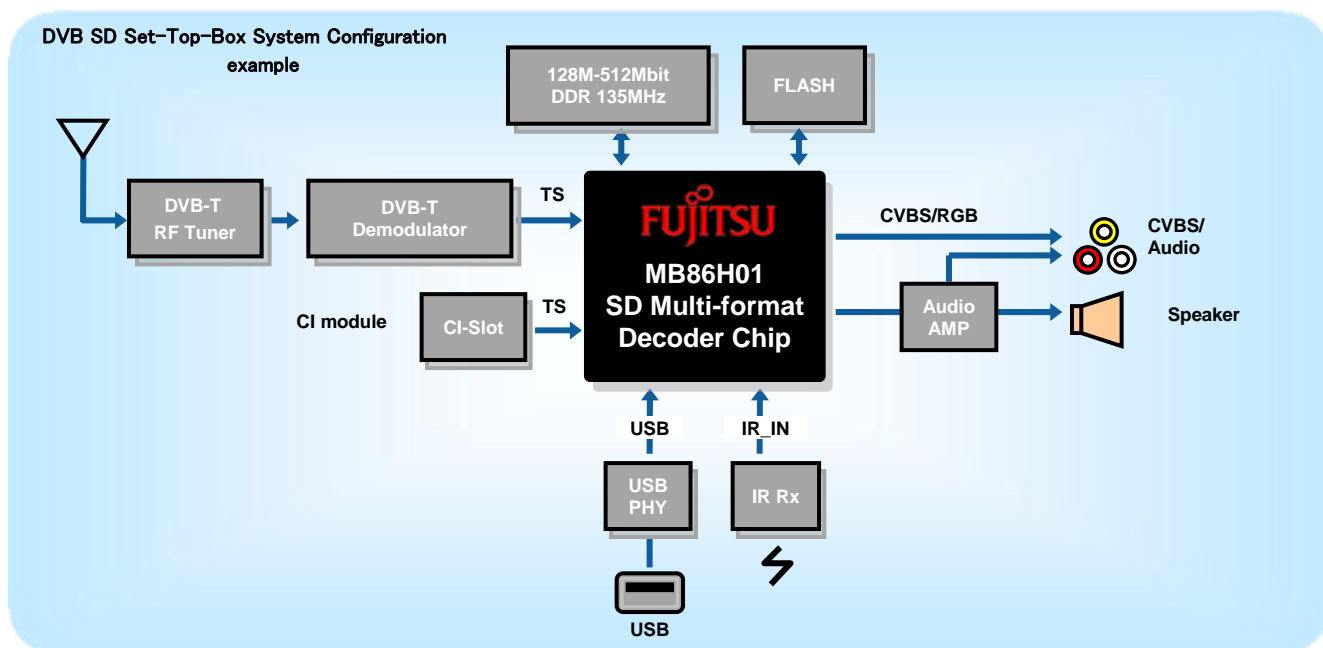
SD Multi-Standard Decoder for Set-Top-Box and iDTV

■ Introduction

The MB86H01 is an advanced set-top-box decoder designed to meet the needs of tomorrow's set-top-box market. This LSI supports the Digital Broadcasting (DVB) standard adopted in many countries in Europe, Asia and others, with the advanced features to support multi-standard decoding of a H.264 and two MPEG-2 decoders integrated into a single chip. This LSI has a 202.5MHz ARC Tangent-A4 CPU inside as well as video/audio decoder function, and other functions needed to receive digital broadcasts.

This LSI is suitable for various applications such as SD set-top-box or iDTV for H.264 broadcasting regions, PVR applications with two MPEG-2 decoders.

The MB86H01 comes with the Fujitsu Driver Application Programming Interface (FAPI) to help customers achieve the shortest possible development cycle. FAPI is a complete driver set allowing fast and efficient customer software design



■ Features

● MPEG-2 dual decoders and H.264 decoder

Fujitsu's new multi-standard decoders include the necessary functionality for TVs and STBs to process SD digital broadcasts, including two (dual) MPEG-2 decoders and one H.264 decoder. The dual MPEG-2 decoders enable the processing of two video streams that can be used in digital video recorders (DVR) with twin tuners. It also allows viewing of two programs at the same time with picture-in-picture, and is suited to DVRs with twin tuners.

● Functions necessary for processing SD broadcasts integrated on a single chip

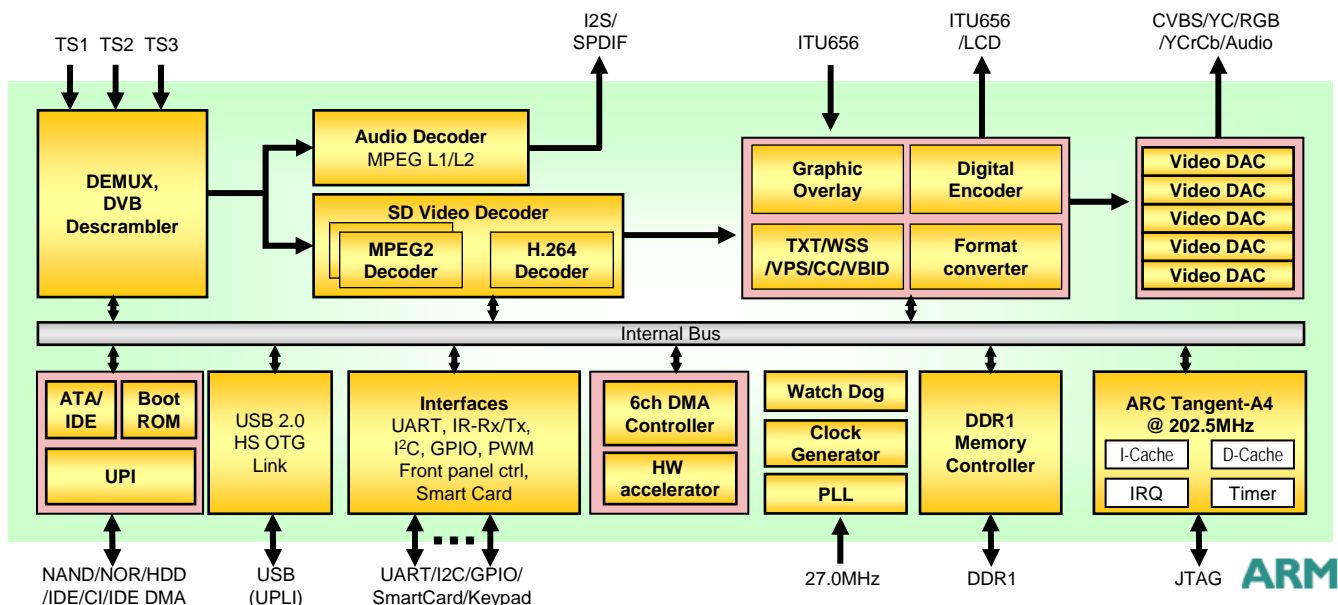
The devices integrate into a single chip a 202.5MHz ARC Tangent-A4 CPU together with the necessary video and audio decode functions, and screen display functionality needed to receive digital broadcast. This enables easy system creation by customers.

● Small form-factor necessary for portable devices

Using proprietary H.264 decoder technology, the power consumption for the H.264 decoder is reduced to a low level. The MB86H01 series offers a 27 x 27mm package (PBGA 256-pin), as well as a small 10 x 10mm package (FBGA 240-pin) suited for use in portable or small form-factor devices. A high speed USB 2.0 OTG controller is also integrated, providing excellent connectivity to external devices, such as digital cameras.

● Succession to existing SmartMPEG series architecture

The new devices have package and pin compatibility with the existing SmartMPEG-C series, as well as maintaining architectural compatibility. This enables existing SmartMPEG users to easily upgrade or develop their systems.



Specifications

CPU core	ARC Tangent-A4 CPU @ 202.5MHz with 4K-I/2K-D cache ARM7TDMI-S™* (67.5MHz): for H.264 video decoder	
Video	Spec	H.264 Main profile / Level 3.0 Decoder, MPEG-2 Video Main profile / Main Level Decoders
	Video Encoder	PAL/NTSC/SECAM, 5ch Video DAC embedded, Teletext/WSS/PDC/CC/VBID
	Interface	Digital RGB output, ITU-R 656 video input/output, YCrCb analog SD output
Audio	Format	MPEG-1/2 Layer I/II
	Channels	2 channels
	Interface	L/R serial, I2S, S/P-DIF
TS Processing	Format	MPEG-2 TS standard
	Channels	3 input streams, Built-in DVB descrambler
	Encryption	3DES encryption/decryption
DDR memory interface	16-bit width DDR-SDRAM135MHz / Supports 128Mbit to 512Mbit SDRAM	
USB	USB 2.0 high Speed OTG Controller (ULPI Interface)	
Input clock frequency	27MHz	
Supply Voltage	1.2V core, 2.5/3.3V I/O	
Operating clock frequency	Internal: 135MHz / DDR memory interface: 135MHz	
Packaging	MB86H01AA: 256-pin PBGA, 27sq.mm (1.27-mm pitch)	
	MB86H01AB: 240-pin FBGA, 10sq.mm (0.5-mm pitch)	

* ARM7TDMI-S is a trademark of ARM Limited.

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