National Semiconductor

MICROCIRCUIT DATA SHEET

MJLM124-X REV 1B1

Original Creation Date: 07/19/95
Last Update Date: 03/28/02
Last Major Revision Date: 03/16/00

QUAD OPERATIONAL AMPLIFIER, SINGLE SUPPLY, LOW POWER

General Description

The LM124 consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 can be directly operated off of the standard +5 VDC power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15 VDC power supplies.

Industry Part Number

LM124

Prime Die

LM124

NS Part Numbers

JL124BCA
JL124BDA
JL124BZA
JL124SCA
JL124SDA

Controlling Document

38510/11005,AMEND.2 CIR.F REV B

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

(Absolute Maximum Ratings)
(Note 1)

Power Dissipation		
CERDIP		400mW
CERPACK		350mW
CERAMIC SOIC		350mW
Supply Voltage		
V+		36Vdc or ±18Vdc
Input Voltage Differential		30Vdc
Input Voltage		-0.03Vdc to +32Vdc
Input Current (Note 3)		
(Vin < -0.3 Vdc)		10 to 0.1mA
Output Short-Circuit to GND (Note 4)		
(One Amplifier)		
V+ ≤ 15Vdc and TA = 25 C		Continuous
Operating Temperature Range		-55 C ≤ Ta ≤ +125 C
Maximum Junction Temperature (Note 2)		175 C
Storage Temperature Range		-65 C ≤ Ta ≤ +150 C
Lead Temperature		
(Soldering, 10 seconds)		260 C
Thermal Resistance		
ThetaJA		
CERDIP	(Still Air)	120 C/W
	(500LF/Min Air Flow)	51 C/W
CERPACK	(Still Air)	140 C/W
	(500LF/Min Air Flow)	116 C/W
CERAMIC SOIC	(Still Air)	140 C/W
	(500LF/Min Air Flow)	116 C/W
ThetaJC		
CERDIP		35 C/W
CERPACK		60 C/W
CERAMIC SOIC		60 C/W
Package Weight		
CERDIP		TBD
CERPACK		460mg
CERAMIC SOIC		410mg
ESD Tolerance (Note 5)		250 V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maxium allowable power dissipation at any temperature is Pdmax = (Tjmax - TA) /ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

(Continued)

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3 VDC (at 25 C).

Note 4: Short circuits from the output to V+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V+. At values of supply voltage in excess of +15 VDC, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 5: Human body model, 1.5K ohms in series with 100 pF.

Electrical Characteristics

DC PARAMETERS

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage	Vcc+ = 30V, Vcc- = Gnd, Vcm = -15V			-5	5	mV	1
					-7	7	mV	2, 3
		Vcc+ = 2V, Vcc- = -28V, Vcm = 13V			-5	5	mV	1
					-7	7	mV	2, 3
		Vcc+ = 5V, Vcc- = Gnd, Vcm = -1.4V			-5	5	mV	1
					-7	7	mV	2, 3
		Vcc+ = 2.5V, Vcc- = -2.5V, Vcm = 1.1V			-5	5	mV	1
					-7	7	mV	2, 3
Iio	Input Offset Current	Vcc+ = 30V, Vcc- = Gnd, Vcm = -15V			-30	30	nA	1, 2
					-75	75	nA	3
		Vcc+ = 2V, Vcc- = -28V, Vcm = 13V			-30	30	nA	1, 2
					-75	75	nA	3
		Vcc+ = 5V, Vcc- = Gnd, Vcm = -1.4V			-30	30	nA	1, 2
					-75	75	nA	3
		Vcc+ = 2.5V, Vcc- = -2.5V, Vcm = 1.1V			-30	30	nA	1, 2
					-75	75	nA	3
+Iib	Input Bias Current	Vcc+ = 30V, Vcc- = Gnd, Vcm = -15V			-150	+0.1	nA	1, 2
					-300	+0.1	nA	3
		Vcc+ = 2V, Vcc- = -28V, Vcm = 13V			-150	+0.1	nA	1, 2
					-300	+0.1	nA	3
		Vcc+ = 5V, Vcc- = Gnd, Vcm = -1.4V			-150	+0.1	nA	1, 2
					-300	+0.1	nA	3
		Vcc+ = 2.5V, Vcc- = -2.5V, Vcm = 1.1V			-150	+0.1	nA	1, 2
					-300	+0.1	nA	3

Electrical Characteristics

DC PARAMETERS(Continued)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
-Iib	Input Bias Current	Vcc+ = 30V, Vcc- = Gnd, Vcm = -15V			-150	+0.1	nA	1, 2
					-300	+0.1	nA	3
		Vcc+ = 2V, Vcc- = -28V, Vcm = 13V			-150	+0.1	nA	1, 2
					-300	+0.1	nA	3
		Vcc+ = 5V, Vcc- = Gnd, Vcm = -1.4V			-150	+0.1	nA	1, 2
					-300	+0.1	nA	3
		Vcc+ = 2.5V, Vcc- = -2.5V, Vcm = 1.1V			-150	+0.1	nA	1, 2
					-300	+0.1	nA	3
+PSRR	Power Supply Rejection Ratio	Vcc- = Gnd, Vcm = -1.4V, 5V ≤ Vcc ≤ 30V			-100	100	uV/V	1, 2, 3
CMRR	Common Mode Rejection Ratio				76		dB	1, 2, 3
Ios+	Output Short Circuit Current	Vcc+ = 30V, Vcc - = Gnd, Vo = +25V			-70		mA	1, 2, 3
Icc	Power Supply Current	Vcc+ = 30V, Vcc - = Gnd				3	mA	1, 2
						4	mA	3
Delta Vio/Delta T	Input Offset Voltage Temperature Sensitivity	+25 C ≤ TA ≤ +125 C, +Vcc = 5V, -Vcc = 0V, Vcm = -1.4V	3		-30	30	uV/ C	2
		-55 C ≤ TA ≤ +25 C, +Vcc = 5V, -Vcc = 0V, Vcm = -1.4V	3		-30	30	uV/ C	3
Delta Iio/Delta T	Input Offset Current Temperature Sensitivity	+25 C ≤ TA ≤ +125 C, +Vcc = 5V, -Vcc = 0V, Vcm = -1.4V	3		-400	400	pA/ C	2
		-55 C ≤ TA ≤ +25 C, +Vcc = 5V, -Vcc = 0V, Vcm = -1.4V	3		-700	700	pA/ C	3
Vol	Logical "0" Output Voltage	Vcc+ = 30V, Vcc- = Gnd, Rl = 10K Ohms				35	mV	4, 5, 6
		Vcc+ = 30V, Vcc- = Gnd, Iol = 5mA				1.5	V	4, 5, 6
		Vcc+ = 4.5V, Vcc- = Gnd, Iol = 2uA				0.4	V	4, 5, 6
Voh	Logical "1" Output Voltage	Vcc+ = 30V, Vcc- = Gnd, Ioh = -10mA			27		V	4, 5, 6
		Vcc+ = 4.5V, Vcc- = Gnd, Ioh = -10mA			2.4		V	4, 5
					2.3		V	6

Electrical Characteristics

DC PARAMETERS(Continued)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Avs+	Voltage Gain	Vcc+ = 30V, Vcc- = Gnd, 1V ≤ Vo ≤ 26V, Rl = 10K Ohms	1		50		V/mV	4
			1		25		V/mV	5, 6
		Vcc+ = 30V, Vcc- = Gnd, 5V ≤ Vo ≤ 20V, Rl = 2K Ohms	1		50		V/mV	4
			1		25		V/mV	5, 6
Avs	Voltage Gain	Vcc+ = 5V, Vcc- = Gnd, 1V ≤ Vo ≤ 2.5V, Rl = 10K Ohms	1		10		V/mV	4, 5, 6
		Vcc+ = 5V, Vcc- = Gnd, 1V ≤ Vo ≤ 2.5V, Rl = 2K Ohms	1		10		V/mV	4, 5, 6
+Vop	Maximum Output Voltage Swing	Vcc+ = 30V, Vcc- = Gnd, Vo = +30V, Rl = 10K Ohms			27		V	4, 5, 6
		Vcc+ = 30V, Vcc- = Gnd, Vo = +30V, Rl = 2K Ohms			26		V	4, 5, 6
Vio(a)	Tempco Screen		4			2.3	mV	
Vio(b)	Tempco Screen		4			2.5	mV	
Iio(a)	Tempco Screen		4			20	nA	
Iio(b)	Tempco Screen		4			16	nA	
+Iib(a)	Tempco Screen		4			16	nA	
+Iib(b)	Tempco Screen		4			10	nA	
+Iib(c)	Tempco Screen		4			13	nA	
-Iib(a)	Tempco Screen		4			16	nA	
-Iib(b)	Tempco Screen		4			10	nA	
-Iib(c)	Tempco Screen		4			13	nA	
PSRR	Tempco Screen		4			17	uV	

Electrical Characteristics

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: +Vcc = 30V, -Vcc = 0V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
TR(tr)	Transient Response: Rise Time	+Vcc = 30V, -Vcc = Gnd				1	uS	7, 8A, 8B
TR(os)	Transient Response: Overshoot	+Vcc = 30V, -Vcc = Gnd				50	%	7, 8A, 8B
Sr+	Slew Rate: Rise	+Vcc = 30V, -Vcc = Gnd			0.1		V/uS	7, 8A, 8B
Sr-	Slew Rate: Fall	+Vcc = 30V, -Vcc = Gnd			0.1		V/uS	7, 8A, 8B
NI(BB)	Noise Broadband	+Vcc = 15V, -Vcc = -15V, BW = 10Hz to 5KHz	5			15	uV/rms	7
NI(PC)	Noise Popcorn	+Vcc = 15V, -Vcc = -15V, Rs = 20K Ohms	2			50	uV/pK	7
Cs	Channel Separation	+Vcc = 30V, -Vcc = Gnd	5		80		dB	7
		+Vcc = 30V, -Vcc = Gnd, Vin = 1V and 16V, Rl = 2K Ohms	5		80		dB	7
		Rl = 2K Ohms, Vin = 1V and 16V, A to B	5		80		dB	7
		Rl = 2K Ohms, Vin = 1V and 16V, A to C	5		80		dB	7
		Rl = 2K Ohms, Vin = 1V and 16V, A to D	5		80		dB	7
		Rl = 2K Ohms, Vin = 1V and 16V, B to A	5		80		dB	7
		Rl = 2K Ohms, Vin = 1V and 16V, B to C	5		80		dB	7
		Rl = 2K Ohms, Vin = 1V and 16V, B to D	5		80		dB	7
		Rl = 2K Ohms, Vin = 1V and 16V, C to A	5		80		dB	7
		Rl = 2K Ohms, Vin = 1V and 16V, C to B	5		80		dB	7
		Rl = 2K Ohms, Vin = 1V and 16V, C to D	5		80		dB	7
		Rl = 2K Ohms, Vin = 1V and 16V, D to A	5		80		dB	7
		Rl = 2K Ohms, Vin = 1V and 16V, D to B	5		80		dB	7
		Rl = 2K Ohms, Vin = 1V and 16V, D to C	5		80		dB	7

Electrical Characteristics

DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: "Delta calculations performed on JAN S and QMLV devices at group B, subgroup 5 only".

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage	Vcc+ = 30V, Vcc- = Gnd, Vcm = -15V			-1	1	mV	1
+Iib	Input Bias Current	Vcc+ = 30V, Vcc- = Gnd, Vcm = -15V			-15	15	nA	1
-Iib	Input Bias Current	Vcc+ = 30V, Vcc- = Gnd, Vcm = -15V			-15	15	nA	1

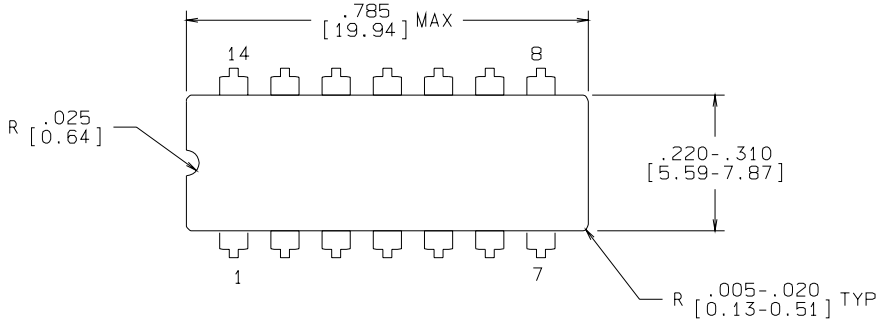
Note 1: V/mV = K.
Note 2: Test on either A360, J273 AC or bench test.
Note 3: Calculated parameters.
Note 4: Temp. Co. DLOG readings will print and MNET transfer will occur only in Test Mode 2 = 1. Bin 5 is a potential Temp. Co. failure.
Note 5: Tested on LTX Channel Separation and Noise test tape.

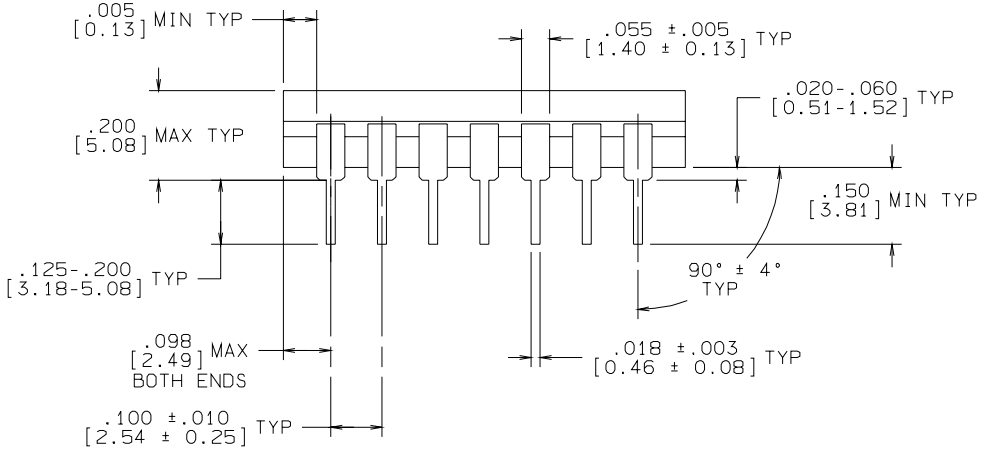
Graphics and Diagrams

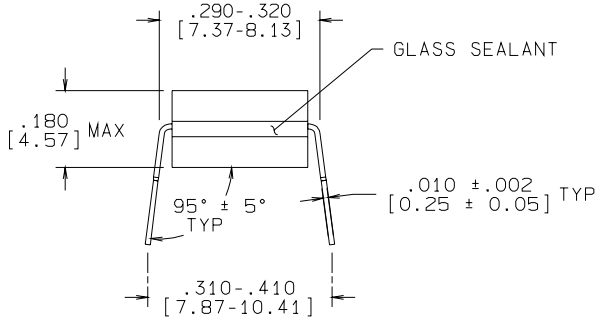
GRAPHICS#	DESCRIPTION
05275HRA4	CERPACK (W), 14 LEAD (B/I CKT)
09173HRA2	CERDIP (J), 14 LEAD (B/I CKT)
J14ARH	CERDIP (J), 14 LEAD (P/P DWG)
P000254B	CERAMIC SOIC (WG), 14 LEAD (PINOUT)
P000288A	CERDIP (J), 14 LEAD (PINOUT)
P000474A	CERPACK (W), 14 LEAD (PIN OUT)
W14BRN	CERPACK (W), 14 LEAD (P/P DWG)
WG14ARC	CERAMIC SOIC (WG), 14LD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
H	REVISE PER CURRENT STD; REDRAW	10001	09/15/93	TL/







CONTROLLING DIMENSION: INCH

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AB, DATED 04/1981.

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

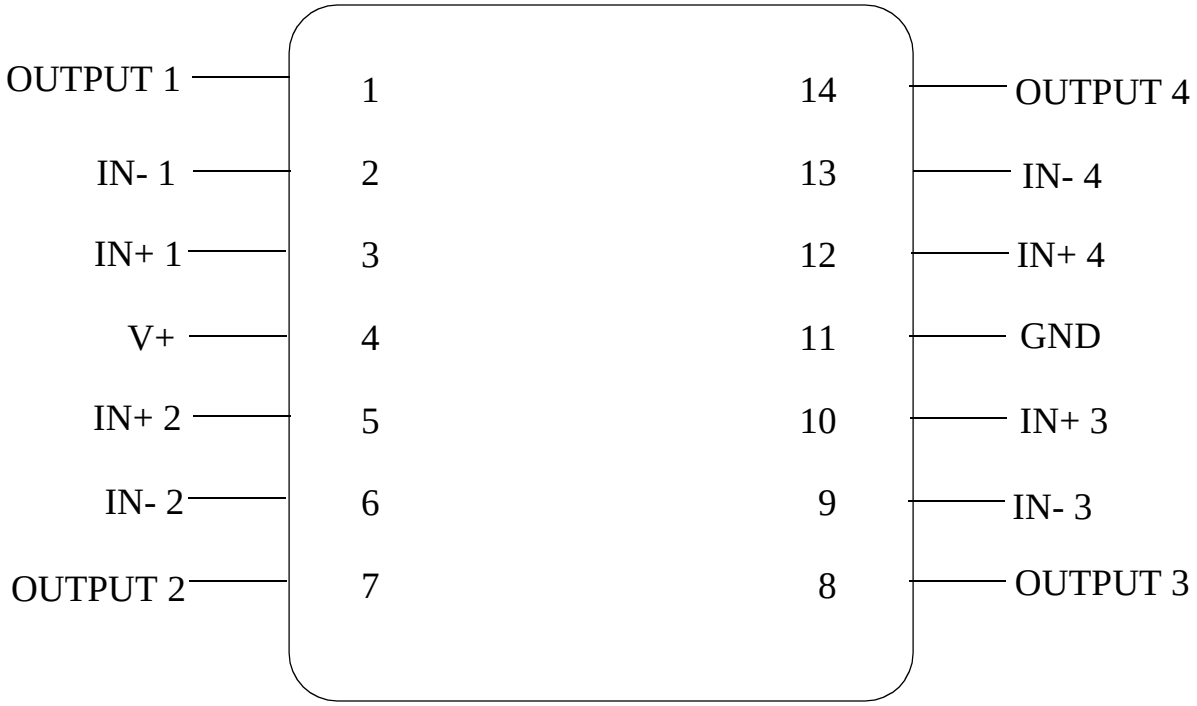
INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 14 LEAD,

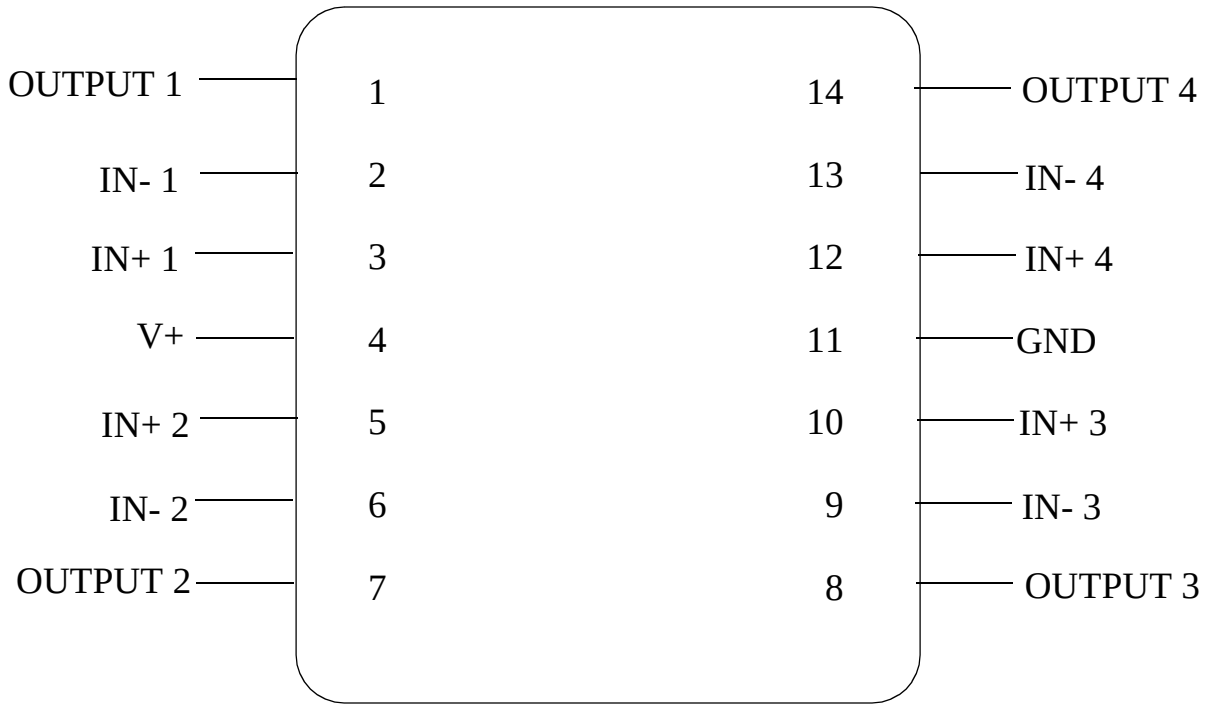
SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J14A	H

DO NOT SCALE DRAWING | SHEET 1 OF 1



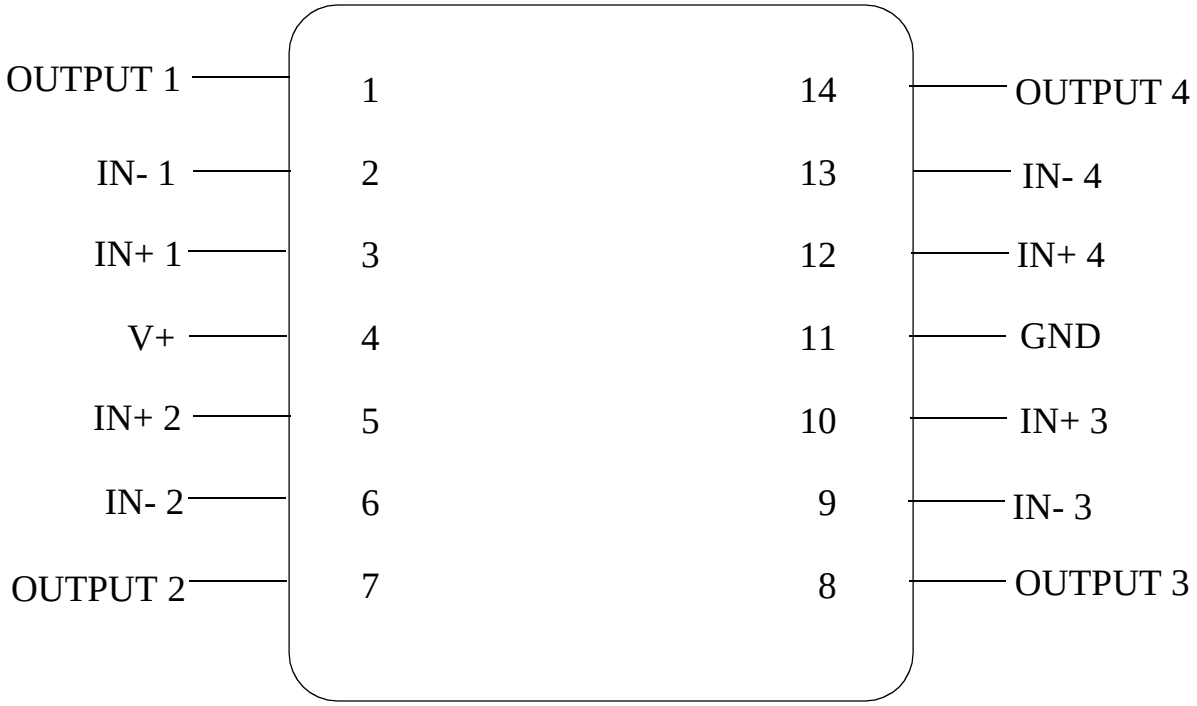
LM124AWG, LM124WG
14 - LEAD CERAMIC SOIC
CONNECTION DIAGRAM
TOP VIEW
P000254B

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM124AJ, LM124J
14 - LEAD DIP
CONNECTION DIAGRAM
TOP VIEW
P000288A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM124AW, LM124W

14 - LEAD CERAMIC CERPACK

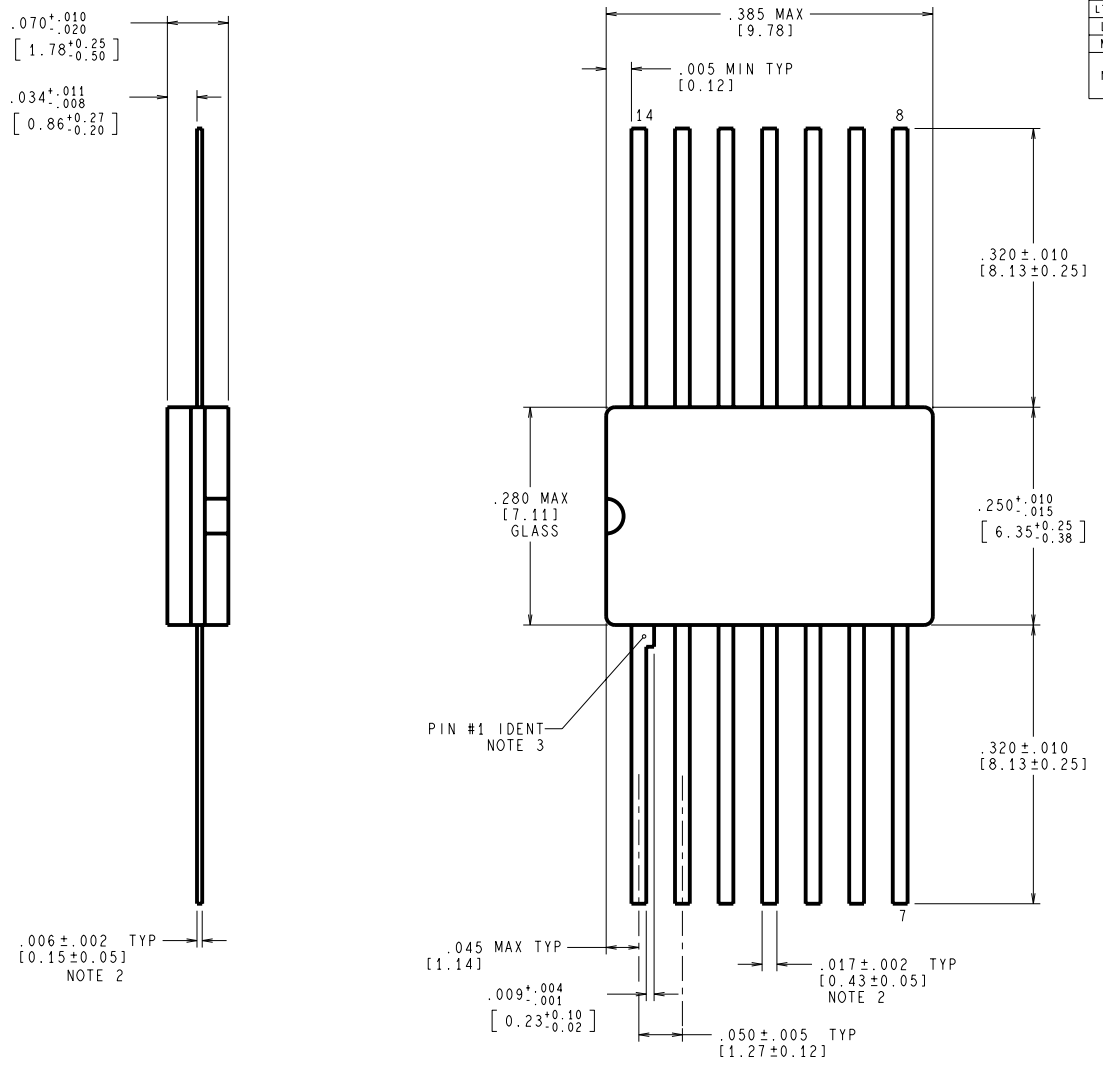
CONNECTION DIAGRAM

TOP VIEW

P000474A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE AND REDRAW PER NEW STANDARD.	10513	07/26/94	DEG/AEP
M	.017±.002 WAS .017±.020.	10655	10/21/94	DEG/CD
N	L/F THKS .006±.002 WAS .005±.001; UPDATE NOTES 1 & 2; REMOVE NOTE 4; UPDATE MILAERO STAMP; DUAL DIM'S WERE INCHES ONLY.	11005	06/08/95	MS/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-I-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. MAXIMUM LIMIT MAY BE INCREASED BY .003 INCHES/ 0.08 MILLIMETERS AFTER LEAD FINISH APPLIED.
3. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-I-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN D.E.Grady	07/26/94
DFTG. CHK.	
ENGR. CHK.	

PROJECTION INCH [MM]

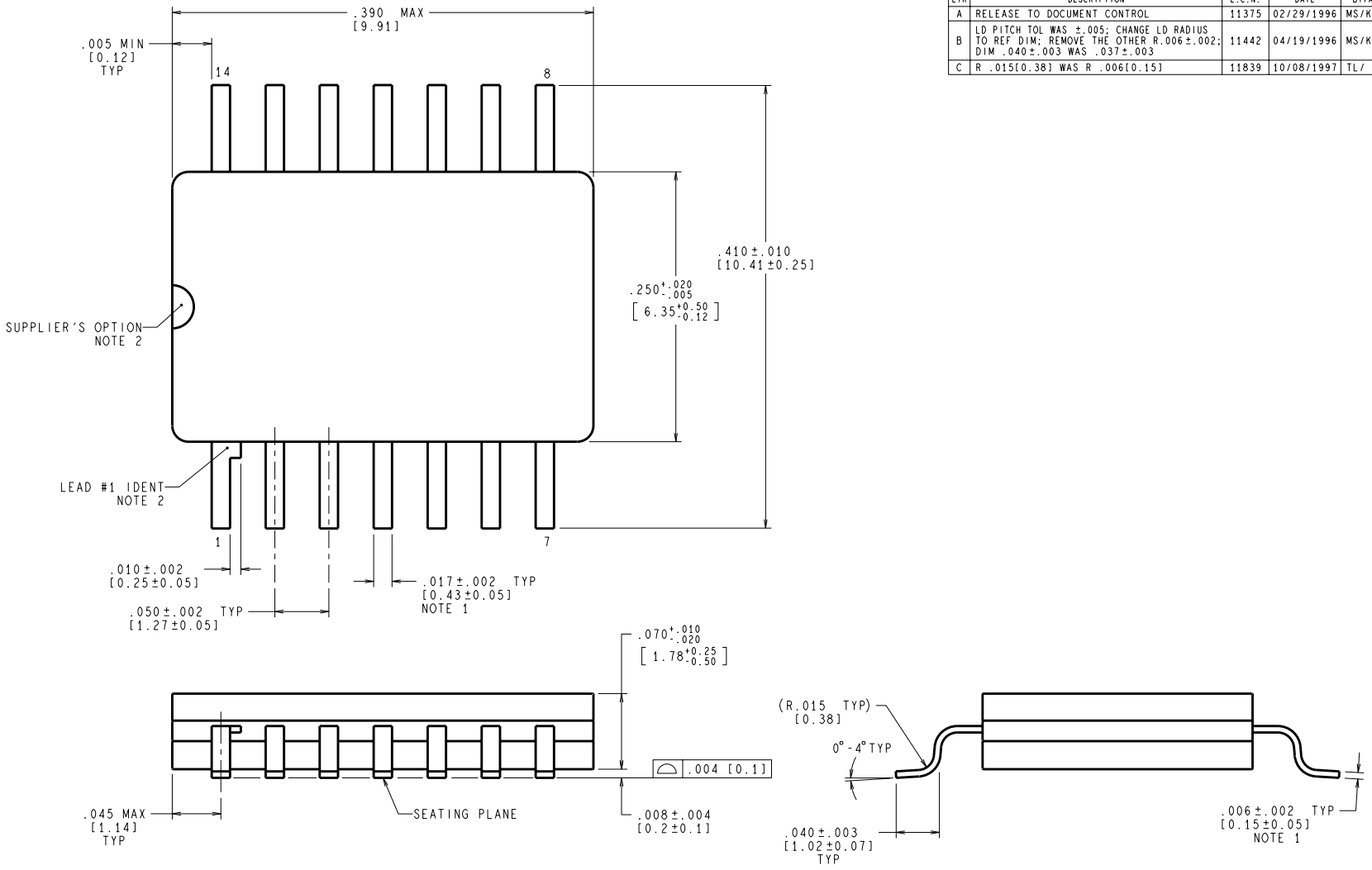
National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 14 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-W14B	N

DO NOT SCALE DRAWING | SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11375	02/29/1996	MS/KH
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002; DIM .040±.003 WAS .037±.003	11442	04/19/1996	MS/KH
C	R .015[0.38] WAS R .006[0.15]	11839	10/08/1997	TL/



NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
2. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
3. NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: MARTA SUCHY	02/29/96
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 14 LEAD, GULL WING

PROJECTION — INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	(SC)MKT-WG14A	C

DO NOT SCALE DRAWING — SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
1A0	M0003654	03/28/02	Rose Malone	Update MDS - MJLM124-X, Rev. 0BL to Fully Released MDS, MJLM124-X, Rev. 1A0. Parameters Delta Vio/Delta T and Delta Iio/Delta T changed from +25 C ≤ TA ≤ +125 C and -55 C ≤ TA ≤ +25 C. Is Now, +25 C ≤ TA ≤ +125 C, +Vcc = 5V, -Vcc = 0V, Vcm = -1.4V and -55 C ≤ TA ≤ +25 C, +Vcc = 5V, -Vcc = 0V, Vcm = -1.4V. To clarify the Tempco test Conditions.
1B1	M0003979	03/28/02	Rose Malone	Update MDS: MJLM124-X, Rev. 1A0 to JMLM124-X, Rev. 1B1. Added WG pkg to Main Table, Absolute Maximum Ratings Section and Graphics Section.