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# HN58S256AI Series

32768-word × 8-bit Electrically Erasable and Programmable  
CMOS ROM

## HITACHI

ADE-203-669A (Z)

Rev. 1.0

May. 20, 1997

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### Description

The Hitachi HN58S256AI is electrically erasable and programmable ROM organized as 32768-word × 8-bit. It has realized high speed, low power consumption and high reliability by employing advanced MNOS memory technology and CMOS process and circuitry technology. It also has a 64-byte page programming function to make the write operations faster.

### Features

- Single 3 V supply: 2.2 to 3.6 V
- Access time: 150 ns/200 ns (max)
- Power dissipation
  - Active: 10 mW/MHz (typ)
  - Standby: 36 μW (max)
- On-chip latches: address, data,  $\overline{CE}$ ,  $\overline{OE}$ ,  $\overline{WE}$
- Automatic byte write: 15 ms (max)
- Automatic page write (64 bytes): 15 ms (max)
- Data polling and Toggle bit
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology
- 10<sup>5</sup> erase/write cycles (in page mode)
- 10 years data retention
- Software data protection
- Wide temperature range: -40 to 85°C

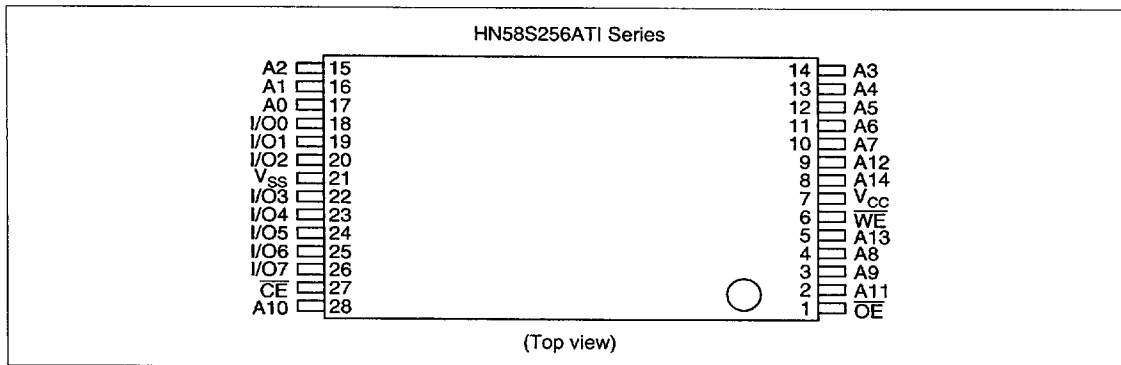
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## HN58S256AI Series

### Ordering Information

Type No.	Access time	Package
HN58S256ATI-15	150 ns	28-pin plastic TSOP (TFP-28DB)
HN58S256ATI-20	200 ns	

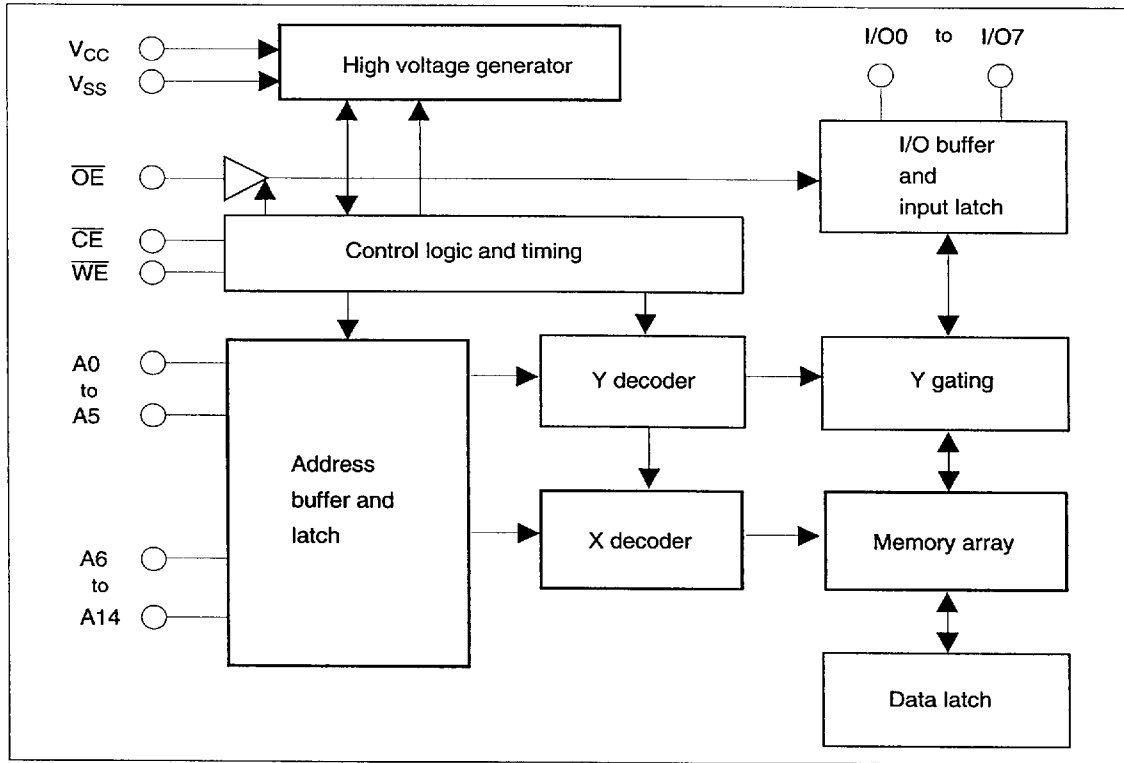
### Pin Arrangement



### Pin Description

Pin name	Function
A0 to A14	Address input
I/O0 to I/O7	Data input/output
$\overline{OE}$	Output enable
CE	Chip enable
WE	Write enable
V <sub>cc</sub>	Power supply
V <sub>ss</sub>	Ground

**Block Diagram**



**Operation Table**

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	$V_{IL}$	$V_{IL}$	$V_{IH}$	Dout
Standby	$V_{IH}$	$\times^{*2}$	$\times$	High-Z
Write	$V_{IL}$	$V_{IH}$	$V_{IL}$	Din
Deselect	$V_{IL}$	$V_{IH}$	$V_{IH}$	High-Z
Write inhibit	$\times$	$\times$	$V_{IH}$	—
	$\times$	$V_{IL}$	$\times$	—
Data polling	$V_{IL}$	$V_{IL}$	$V_{IH}$	Dout (I/O7)

Notes: 1. Refer to the recommended DC operating condition.  
 2.  $\times$ : Don't care

## HN58S256AI Series

### Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to $V_{SS}$	$V_{CC}$	-0.6 to +4.6	V
Input voltage relative to $V_{SS}$	$V_{in}$	-0.5* <sup>1</sup> to +4.6* <sup>3</sup>	V
Operating temperature range* <sup>2</sup>	$T_{opr}$	-40 to +85	°C
Storage temperature range	$T_{stg}$	-55 to +125	°C

- Notes: 1.  $V_{in}$  min = -3.0 V for pulse width  $\leq$  50 ns  
 2. Including electrical characteristics and data retention  
 3. Should not exceed  $V_{CC} + 1.0$  V.

### Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	2.2	3.0	3.6	V
	$V_{SS}$	0	0	0	V
Input voltage	$V_{IL}$	-0.3* <sup>1</sup>	—	0.4	V
	$V_{IH}$	$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$ * <sup>2</sup>	V
Operating temperature	$T_{opr}$	-40	—	85	°C

- Notes: 1.  $V_{IL}$  min: -1.0 V for pulse width  $\leq$  50 ns.  
 2.  $V_{IH}$  max:  $V_{CC} + 1.0$  V for pulse width  $\leq$  50 ns.

### DC Characteristics ( $T_a = -40$ to $+85^\circ\text{C}$ , $V_{CC} = 2.2$ to $3.6$ V)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	$I_{LI}$	—	—	2	$\mu\text{A}$	$V_{CC} = 3.6$ V, $V_{in} = 0$ to $3.6$ V
Output leakage current	$I_{LO}$	—	—	2	$\mu\text{A}$	$V_{CC} = 3.6$ V, $V_{out} = 3.6/0.4$ V, $\overline{CE} = V_{IH}$ , $V_{in} = 0$ to $3.6$ V
Standby $V_{CC}$ current	$I_{CC1}$	—	—	10	$\mu\text{A}$	$\overline{CE} = V_{CC}$
	$I_{CC2}$	—	—	500	$\mu\text{A}$	$\overline{CE} = V_{IH}$
Operating $V_{CC}$ current	$I_{CC3}$	—	—	8	mA	$I_{out} = 0$ mA, Duty = 100%, Cycle = 1 $\mu\text{s}$ at $V_{CC} = 3.6$ V
		—	—	15	mA	$I_{out} = 0$ mA, Duty = 100%, Cycle = 150 ns at $V_{CC} = 3.6$ V
Output low voltage	$V_{OL}$	—	—	0.4	V	$I_{OL} = 1.0$ mA
Output high voltage	$V_{OH}$	$V_{CC} \times 0.8$	—	—	V	$I_{OH} = -100$ $\mu\text{A}$

## HN58S256AI Series

### Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance*1	Cin	—	—	6	pF	Vin = 0 V
Output capacitance*1	Cout	—	—	12	pF	Vout = 0 V

Note: 1. This parameter is periodically sampled and not 100% tested.

### AC Characteristics (Ta = -40 to +85°C, Vcc = 2.2 to 3.6 V)

#### Test Conditions

- Input pulse levels: 0.4 V to 1.9 V (Vcc ≤ 2.7V), 0.4V to 2.4 V (Vcc > 2.7 V)
- Input rise and fall time: ≤ 5 ns
- Input timing reference levels: 0.8, 1.8 V
- Output load: 1TTL Gate +100 pF
- Output reference levels: 1.1 V, 1.1 V (Vcc ≤ 2.7V), 1.5 V, 1.5 V (Vcc > 2.7 V)

#### Read Cycle

Parameter	Symbol	HN58S256AI				Unit	Test conditions
		-15		-20			
		Min	Max	Min	Max		
Address to output delay	t <sub>ACC</sub>	—	150	—	200	ns	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$
$\overline{CE}$ to output delay	t <sub>CE</sub>	—	150	—	200	ns	$\overline{OE} = V_{IL}, \overline{WE} = V_{IH}$
$\overline{OE}$ to output delay	t <sub>OE</sub>	10	80	10	100	ns	$\overline{CE} = V_{IL}, \overline{WE} = V_{IH}$
Address to output hold	t <sub>OH</sub>	0	—	0	—	ns	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$
$\overline{OE}$ ( $\overline{CE}$ ) high to output float*1	t <sub>DF</sub>	0	100	0	100	ns	$\overline{CE} = V_{IL}, \overline{WE} = V_{IH}$

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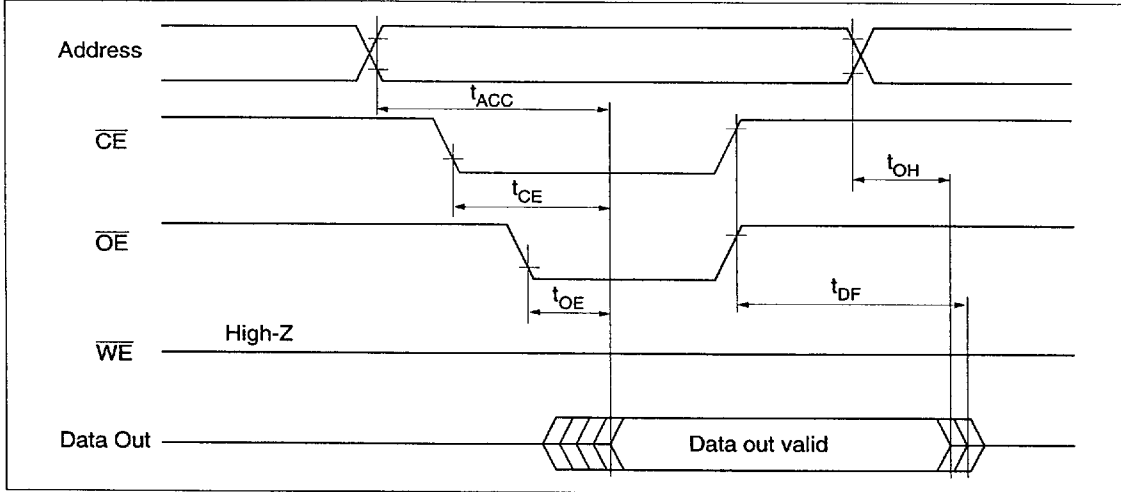
## HN58S256AI Series

### Write Cycle

Parameter	Symbol	Min* <sup>2</sup>	Typ	Max	Unit	Test conditions
Address setup time	$t_{AS}$	0	—	—	ns	
Address hold time	$t_{AH}$	150	—	—	ns	
$\overline{CE}$ to write setup time ( $\overline{WE}$ controlled)	$t_{CS}$	0	—	—	ns	
$\overline{CE}$ hold time ( $\overline{WE}$ controlled)	$t_{CH}$	0	—	—	ns	
$\overline{WE}$ to write setup time ( $\overline{CE}$ controlled)	$t_{WS}$	0	—	—	ns	
$\overline{WE}$ hold time ( $\overline{CE}$ controlled)	$t_{WH}$	0	—	—	ns	
$\overline{OE}$ to write setup time	$t_{OES}$	0	—	—	ns	
$\overline{OE}$ hold time	$t_{OEH}$	0	—	—	ns	
Data setup time	$t_{DS}$	150	—	—	ns	
Data hold time	$t_{DH}$	0	—	—	ns	
$\overline{WE}$ pulse width ( $\overline{WE}$ controlled)	$t_{WP}$	200	—	—	ns	
$\overline{CE}$ pulse width ( $\overline{CE}$ controlled)	$t_{CW}$	200	—	—	ns	
Data latch time	$t_{DL}$	200	—	—	ns	
Byte load cycle	$t_{BLC}$	0.4	—	30	$\mu$ s	
Byte load window	$t_{BL}$	100	—	—	$\mu$ s	
Write cycle time	$t_{WC}$	—	—	15* <sup>3</sup>	ms	
Write start time	$t_{DW}$	0* <sup>4</sup>	—	—	ns	

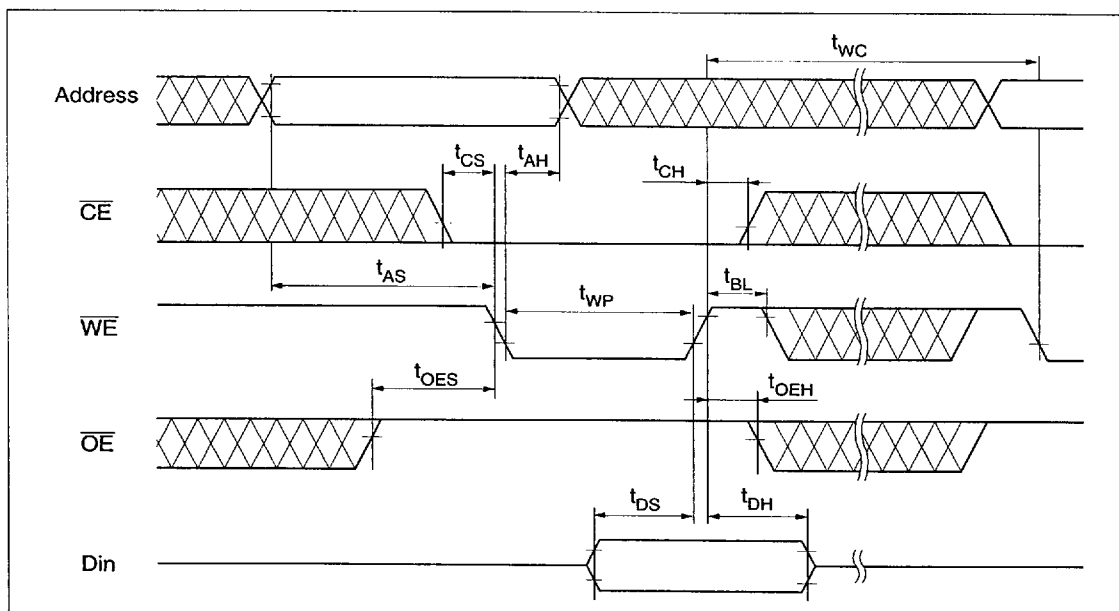
- Notes:
- $t_{DF}$  is defined as the time at which the outputs achieve the open circuit conditions and are no longer driven.
  - Use this device in longer cycle than this value.
  - $t_{WC}$  must be longer than this value unless polling techniques is used. This device automatically completes the internal write operation within this value.
  - Next read or write operation can be initiated after  $t_{DW}$  if polling techniques is used.
  - A16 through A14 are page addresses and these addresses are latched at the first falling edge of  $\overline{WE}$ .
  - A16 through A14 are page addresses and these addresses are latched at the first falling edge of  $\overline{CE}$ .
  - See AC read characteristics.

Read Timing Waveform

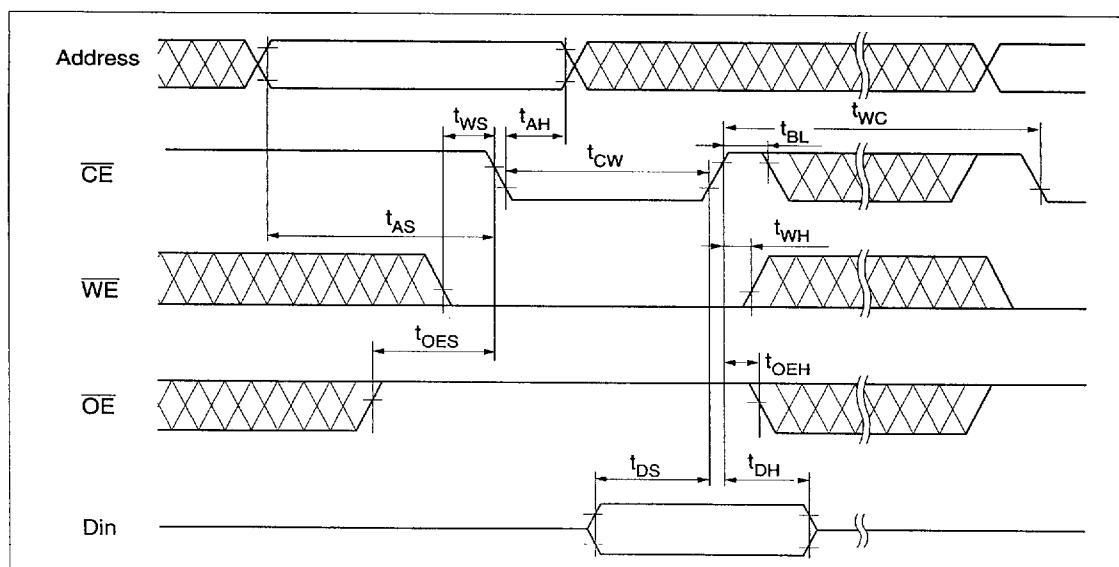


## HN58S256AI Series

Byte Write Timing Waveform (1) ( $\overline{WE}$  Controlled)

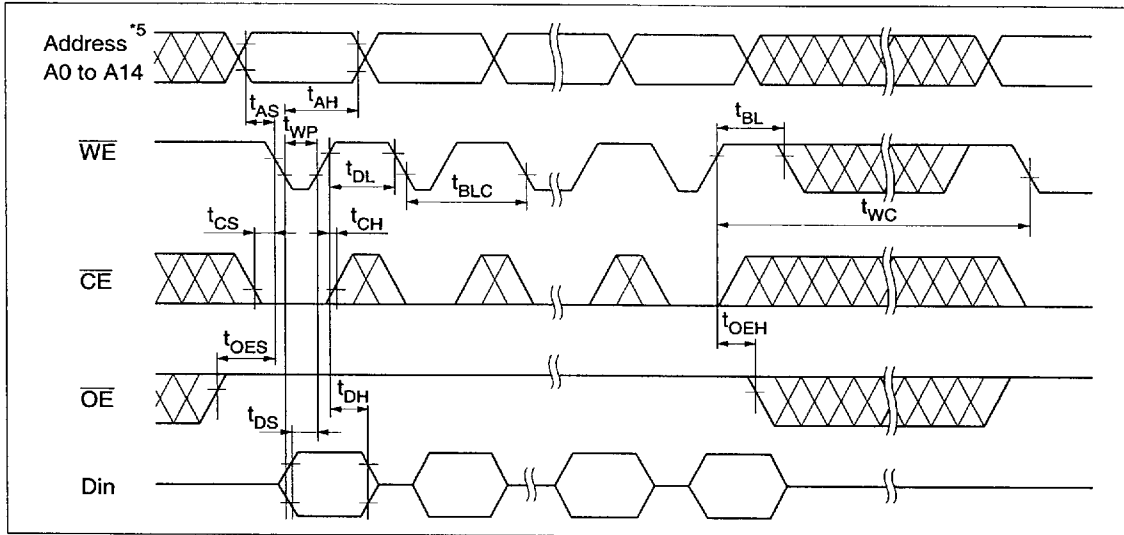


Byte Write Timing Waveform (2) ( $\overline{CE}$  Controlled)

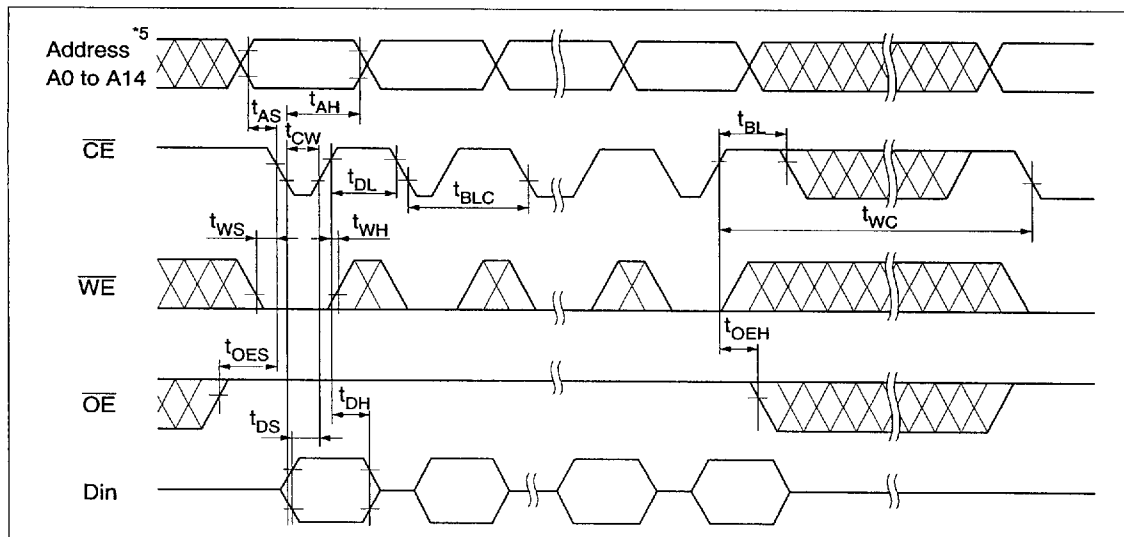




Page Write Timing Waveform (1) ( $\overline{WE}$  Controlled)



Page Write Timing Waveform (2) ( $\overline{CE}$  Controlled)



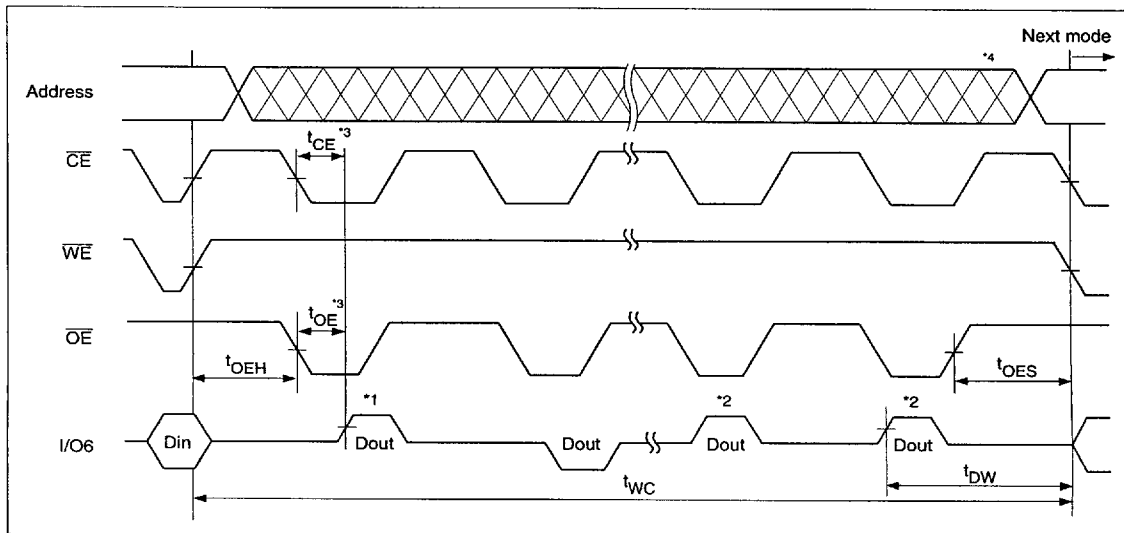


**Toggle bit**

This device provide another function to determine the internal programming cycle. If the EEPROM is set to read mode during the internal programming cycle, I/O6 will charge from "1" to "0" (toggling) for each read. When the internal programming cycle is finished, toggling of I/O6 will stop and the device can be accessible for next read or program.

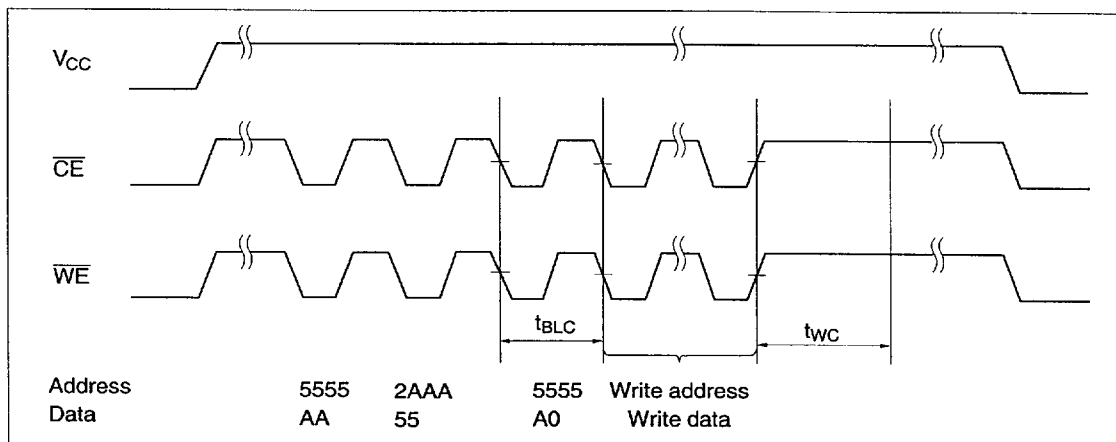
**Toggle bit Waveform**

- Notes: 1. I/O6 beginning state is "1".  
 2. I/O6 ending state will vary.  
 3. See AC read characteristics.  
 4. Any address location can be used, but the address must be fixed.

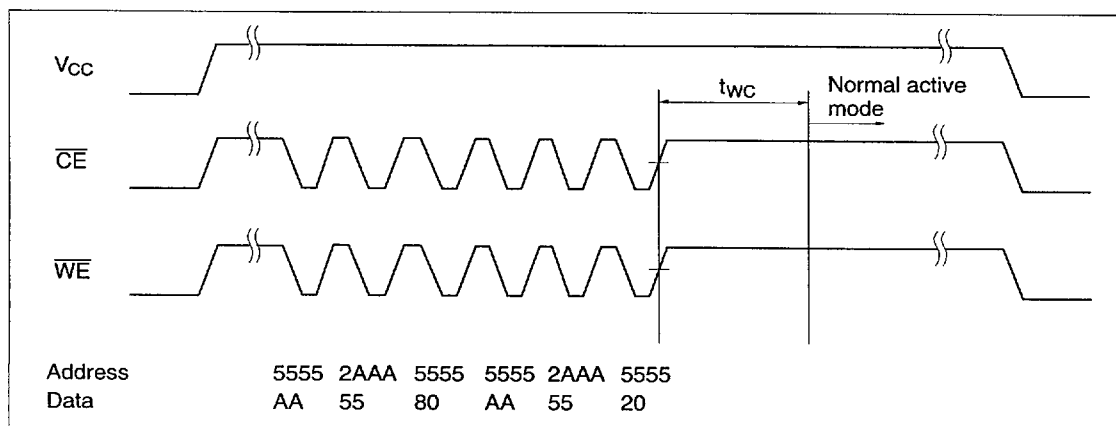


## HN58S256AI Series

Software Data Protection Timing Waveform (1) (in protection mode)



Software Data Protection Timing Waveform (2) (in non-protection mode)



## **Functional Description**

### **Automatic Page Write**

Page-mode write feature allows 1 to 64 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 63 bytes can be written in the same manner. Each additional byte load cycle must be started within 30  $\mu$ s from the preceding falling edge of  $\overline{WE}$  or  $\overline{CE}$ . When  $\overline{CE}$  or  $\overline{WE}$  is high for 100  $\mu$ s after data input, the EEPROM enters write mode automatically and the input data are written into the EEPROM.

### **$\overline{Data}$ Polling**

Data polling indicates the status that the EEPROM is in a write cycle or not. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data outputs from I/O7 to indicate that the EEPROM is performing a write operation.

### **$\overline{WE}$ , $\overline{CE}$ Pin Operation**

During a write cycle, addresses are latched by the falling edge of  $\overline{WE}$  or  $\overline{CE}$ , and data is latched by the rising edge of  $\overline{WE}$  or  $\overline{CE}$ .

### **Write/Erase Endurance and Data Retention Time**

The endurance is  $10^5$  cycles in case of the page programming and  $10^4$  cycles in case of the byte programming (1% cumulative failure rate). The data retention time is more than 10 years when a device is page-programmed less than  $10^4$  cycles.

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## HN58S256AI Series

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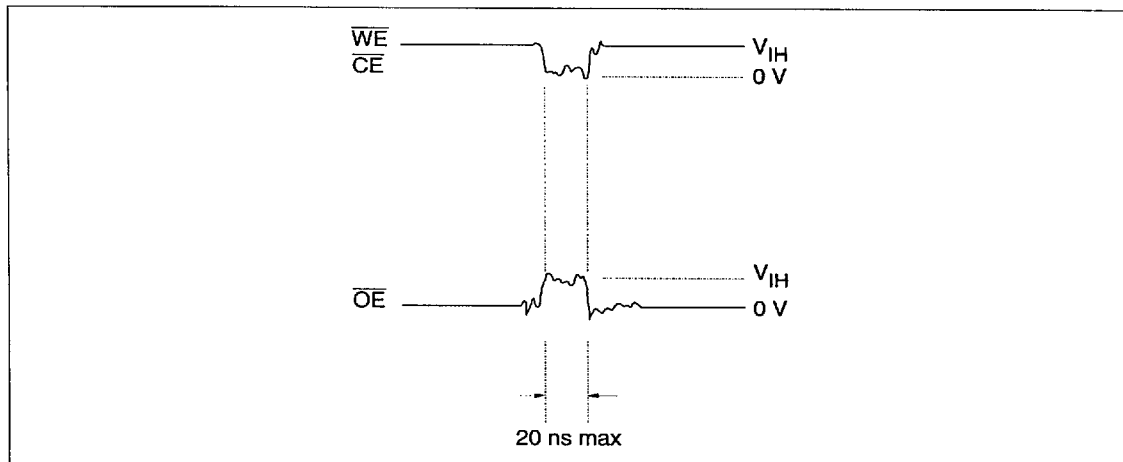
### Data Protection

#### 1. Data Protection against Noise on Control Pins ( $\overline{\text{CE}}$ , $\overline{\text{OE}}$ , $\overline{\text{WE}}$ ) during Operation

During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake.

To prevent this phenomenon, this device has a noise cancellation function that cuts noise if its width is 20 ns or less.

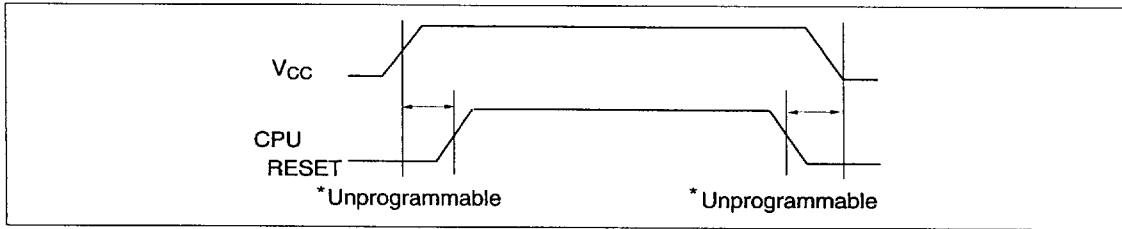
Be careful not to allow noise of a width of more than 20 ns on the control pins.



2. Data Protection at  $V_{CC}$  On/Off

When  $V_{CC}$  is turned on or off, noise on the control pins generated by external circuits (CPU, etc.) may act as a trigger and turn the EEPROM to program mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable state while the CPU is in an unstable state.

Note: The EEPROM should be kept in unprogrammable state during  $V_{CC}$  on/off by using CPU RESET signal.



(1) Protection by  $\overline{CE}$ ,  $\overline{OE}$ ,  $\overline{WE}$

To realize the unprogrammable state, the input level of control pins must be held as shown in the table below.

$\overline{CE}$	$V_{CC}$	x	x
$\overline{OE}$	x	$V_{SS}$	x
$\overline{WE}$	x	x	$V_{CC}$

x: Don't care.

$V_{CC}$ : Pull-up to  $V_{CC}$  level.

$V_{SS}$ : Pull-down to  $V_{SS}$  level.

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### 3. Software data protection

To prevent unintentional programming, this device has the software data protection (SDP) mode. The SDP is enabled by inputting the following 3 bytes code and write data. SDP is not enabled if only the 3 bytes code is input. To program data in the SDP enable mode, 3 bytes code must be input before write data.

Address	Data
5555	AA
↓	↓
2AAA	55
↓	↓
5555	A0
↓	↓
Write address	Write data } Normal data input

The SDP mode is disabled by inputting the following 6 bytes code. Note that, if data is input in the SDP disable cycle, data not be written.

Address	Data
5555	AA
↓	↓
2AAA	55
↓	↓
5555	80
↓	↓
5555	AA
↓	↓
2AAA	55
↓	↓
5555	20

The software data protection is not enabled at the shipment.

Note: There are some differences between Hitachi's and other company's for enable/disable sequence of software data protection. If there are any questions, please contact with Hitachi sales offices.

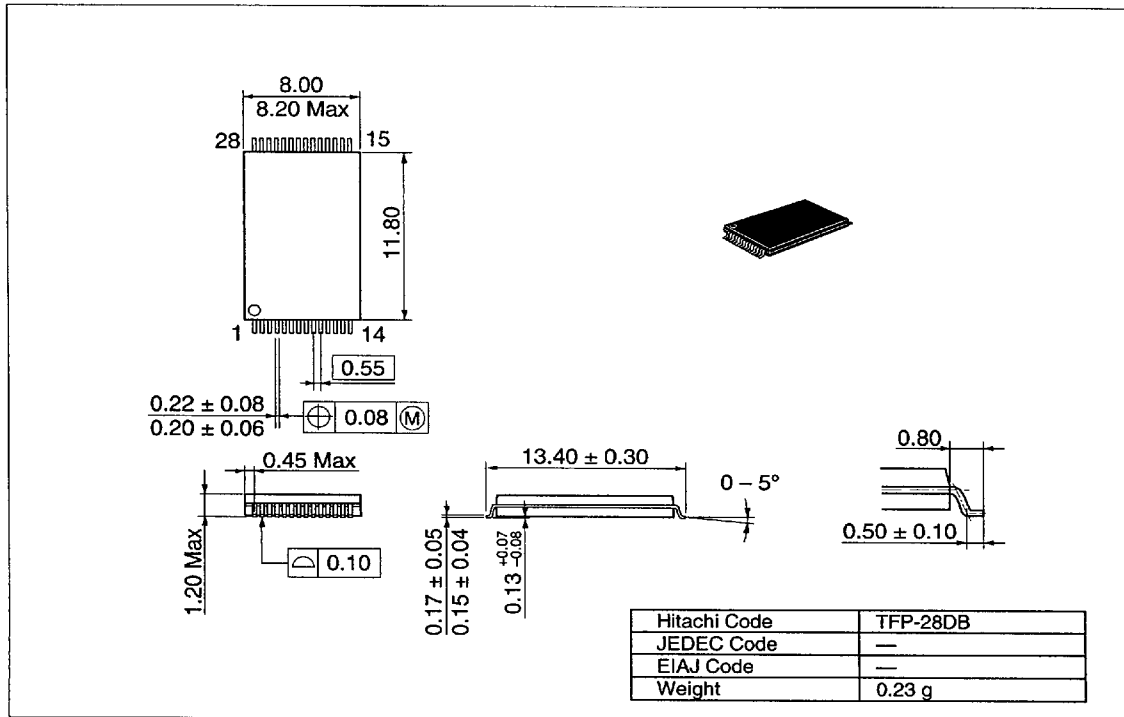


# HN58S256AI Series

## Package Dimensions

HN58S256AI Series (TFP-28DB)

Unit: mm



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