SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

ST75C520 HARDWARE POWER-UP

The ST75C520 is a monochip fax component which includes a DSP (Digital Signal Processor), memory (Program, Coefficients, Ram), CPU interface (Dual Port Ram) and also an AFE (Analog Front End).

In a FAX application we assume that two main states could happend :
- Power OFF state,
- Power ON state.

Power OFF State

In the Power OFF state we assume that all the hardware of the FAX application is turned off and both DV_{DD} and AV_{DD} are equal to 0V and the ST75C520 digital inputs are equal to 0V.

Power ON State

In the Power ON state we assume that all the hardware of the FAX application is turned on and both DV_{DD} and AV_{DD} are equal to +5V. We remenber that it is possible to set the ST75C520 in a sleep mode to reduce the power consumption when the power supply of the FAX equipment is turned on. To do that the CPU will have to send the SLEEP command to the ST75C520.

Take care that in **sleep mode** the ST75C520 stops all the chip, the oscillator (so it means that the CLKOUT signal will not be actived and the EXTAL/EXATL pins will not work).
To awake the ST75C520 the application will have three possibilities :

a) Use the RESET pin :
The ST75C520 starts as at power up and will set IT6 (Interupt 6 in ITSRCR register) when the full initialization will be done (the ST75C520 is ready to accept a command from the CPU).

b) Send a low level on the RING input :
The ST75C520 awakes and starts an initialization and then set IT5 (Interrupt 5 in ITSRCR register) when it is ready to accept a command fro the CPU.

c) Do a dummy write in the Dual Port Ram with the CPU : The ST75C520 will do as for case b).

Special Power DOWN State

It can be interesting to reduce to the minimum the power consumption of the FAX equipment. To do that the DV_{DD} and AV_{DD} will not be provided and all the power supply will be turn off (for the ST75C520 and but also for some other component as the CPU ...). In such a case if the DV_{DD} and AV_{DD} and all the digital inputs of the ST75C520 are equal to 0V we are in the POWER OFF state already described above.

But if the DV_{DD}, AV_{DD} and all the digital inputs are not equal to 0V (for exemple : 0.3V or 0.6V) the ST75C520 Boundary Scan Interface could be disturbed when the FAX equipment will be turn on :
We have to consider that the DSP is used by the FAX application with the CPU interface (Dual Port Ram) but that the DSP CORE can also be used by another way : the Boundary Scan Interface. The purpose of the Boundary Scan Interface function is only to provide a way to access to the DSP core (for DSP software debug) and to do some tests in production. But the Boundary Scan Interface must not be used in the FAX application.

We remenber that the Boundary Scan Signals are (see data sheet page 4/44) :

SCIN	input
SCCLK	input
SCOUT	output
BOS	input
EOS	input
MCO..MC2	input
HALT	input
MCI	output
RDYS	output
EBS	input
CLKOUT	output

All the Boundary Scan Interface are sampled on the rising edge of the SCCLK signal (EBS is not sample and is a static signal).

MC0, MC1, MC2 will select the operating mode of DSP CORE : normal mode, DSP core test...
MC0 = MC1 = MC2 = 0 will select the normal mode.

As in our case the DV_{DD}, AV_{DD} and all the Boundary Scan Interface inputs are not equal to 0V (for exemple 0.3V or 0.6V) a digital noise could appear when the application will turn on the power supply.

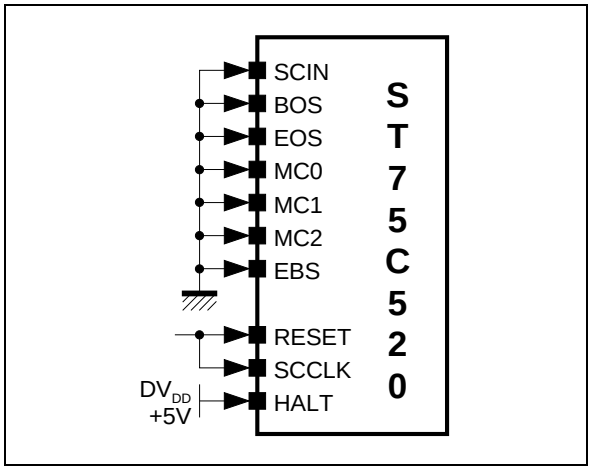
So the Boundary Scan interface could be selected instead of the Dual Port Ram and some special behaviour could be started (as test of the DSP CORE). In such a case the CPU will not have the possibility to use the ST75C520.

To avoid this kind of problem the customer has to connect the Boundary Scan Interface input as indicated :

- SCIN to the GND
- EOS to the GND
- BOS to the GND
- MC0 to the GND
- MC1 to the GND
- MC2 to the GND
- HALT to the DV_{DD} (+5V)
- EBS to the GND
- SCCLK to the RESET pin

The rising edge of the RESET signal will set up the Boundary Scan Interface in the right mode and the DSP will be ready to run its software and to communicate with the CPU using the Dual Port Ram Interface.

Figure 1 : Connection of the Boundary Scan Interface Input in the FAX Application



Here after (see Figure 2) is given a simple block diagram of the chip which shows the main parts of the ST75C520.

Figure 2 : Simple Block Diagram