

RJK6024DPE

600V - 0.4A - MOS FET
High Speed Power Switching

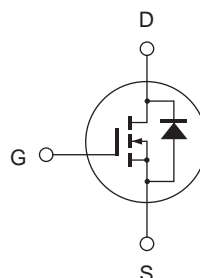
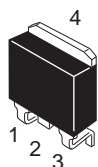
R07DS0424EJ0200
Rev.2.00
Feb 27, 2012

Features

- Low on-resistance
 $R_{DS(on)} = 28 \Omega$ typ. (at $I_D = 0.2 \text{ A}$, $V_{GS} = 10 \text{ V}$, $T_a = 25^\circ\text{C}$)
- Low leakage current
- High speed switching

Outline

RENESAS Package code: PRSS0004AE-B
(Package name: LDKPAK(S)-(1))



1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	600	V
Gate to source voltage	V_{GSS}	± 30	V
Drain current	I_D	0.4	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	0.6	A
Body-drain diode reverse drain current	I_{DR}	0.4	A
Body-drain diode reverse drain peak current	$I_{DR(pulse)}$ ^{Note1}	0.6	A
Channel dissipation	P_{ch} ^{Note2}	20	W
Channel to case thermal impedance	θ_{ch-c}	6.25	$^\circ\text{C}/\text{W}$
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

- Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$
2. Value at $T_c = 25^\circ\text{C}$

Electrical Characteristics

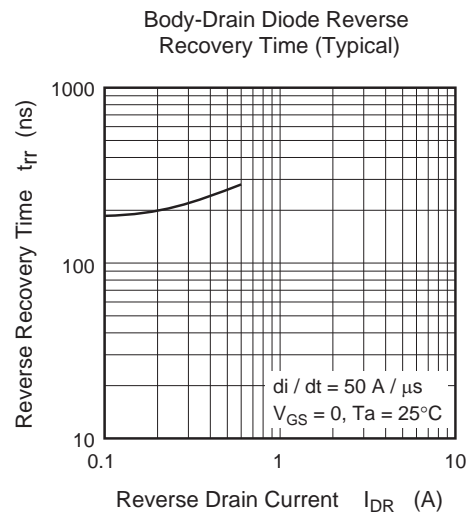
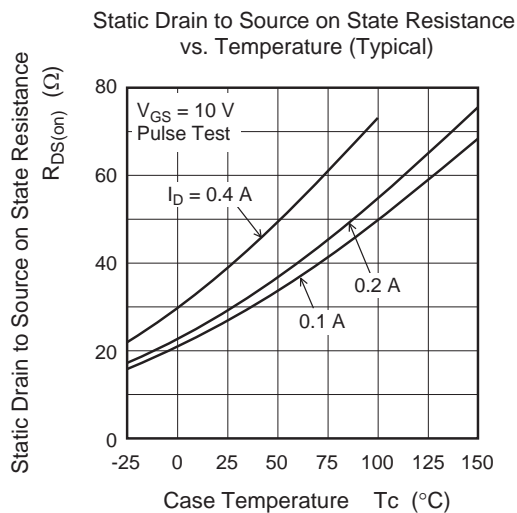
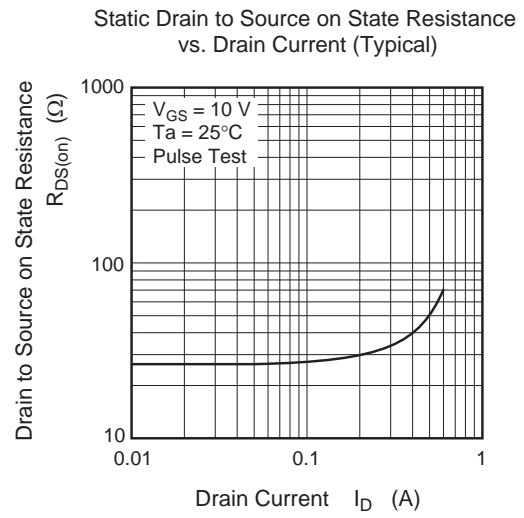
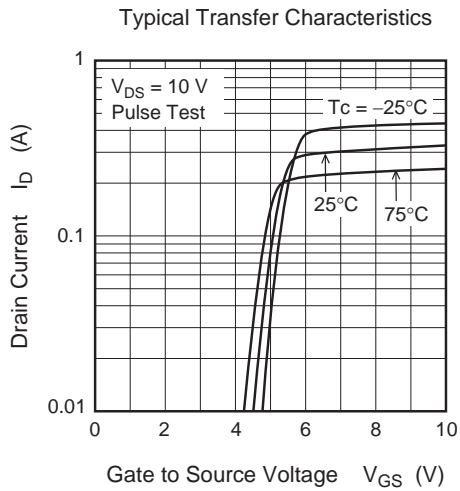
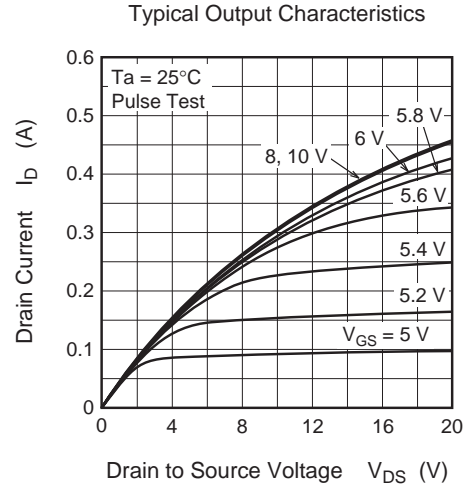
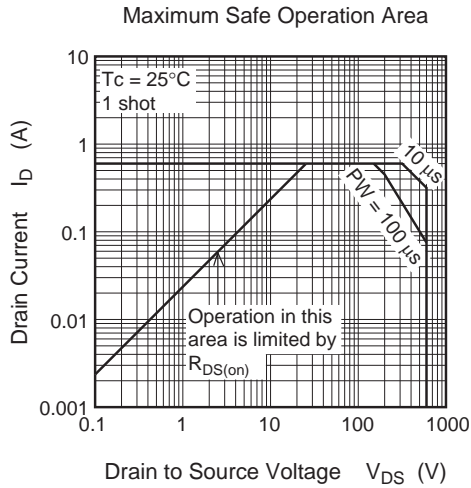
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	600	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 600 \text{ V}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 30 \text{ V}$, $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	3	—	5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	28	42	Ω	$I_D = 0.2 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note3}
Input capacitance	C_{iss}	—	37.5	—	pF	$V_{DS} = 25 \text{ V}$
Output capacitance	C_{oss}	—	7.5	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	0.9	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	30	—	ns	$I_D = 0.2 \text{ A}$
Rise time	t_r	—	14.5	—	ns	$V_{GS} = 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	48	—	ns	$R_L = 1500 \Omega$
Fall time	t_f	—	77	—	ns	$R_g = 10 \Omega$
Total gate charge	Q_g	—	4.3	—	nC	$V_{DD} = 480 \text{ V}$
Gate to source charge	Q_{gs}	—	0.5	—	nC	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Q_{gd}	—	3.2	—	nC	$I_D = 0.4 \text{ A}$
Body-drain diode forward voltage	V_{DF}	—	0.85	1.45	V	$I_F = 0.4 \text{ A}$, $V_{GS} = 0$ ^{Note3}
Body-drain diode reverse recovery time	t_{rr}	—	230	—	ns	$I_F = 0.4 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 50 \text{ A}/\mu\text{s}$

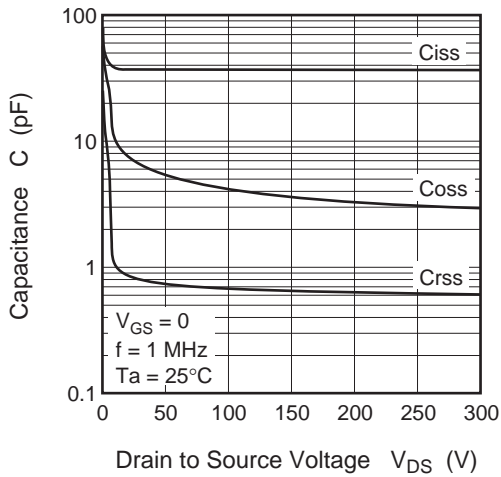
Notes: 3. Pulse test

4. Since this device is equipped with high voltage FET chip ($V_{DSS} \geq 600 \text{ V}$), high voltage may be supplied. Therefore, please be sure to confirm about Electric discharge between Drain terminal and other terminal.
5. This device is sensitive to electrostatic discharge.
It is recommended to adopt appropriate cautions when handling this product.

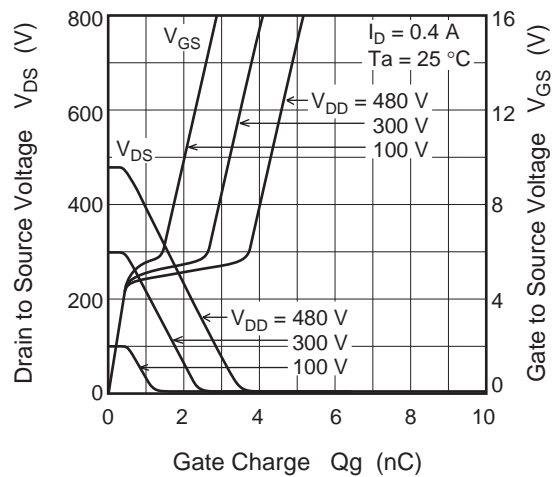
Main Characteristics



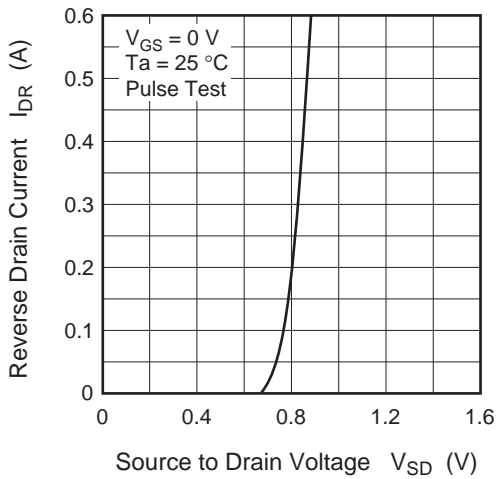
Typical Capacitance vs. Drain to Source Voltage (Typical)



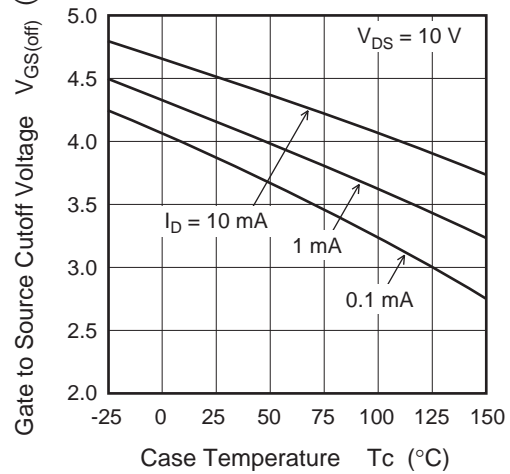
Dynamic Input Characteristics (Typical)



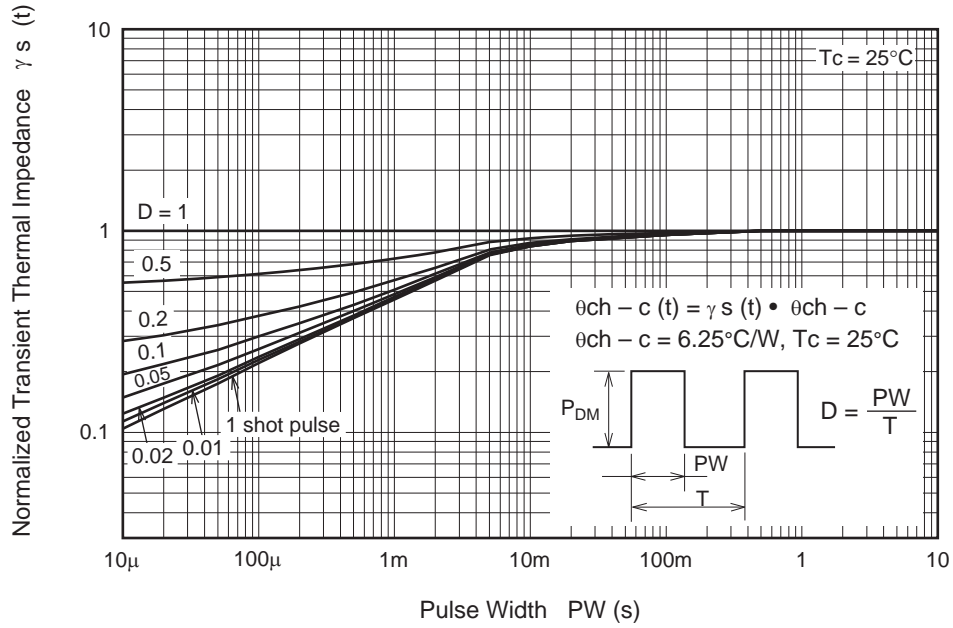
Reverse Drain Current vs. Source to Drain Voltage (Typical)



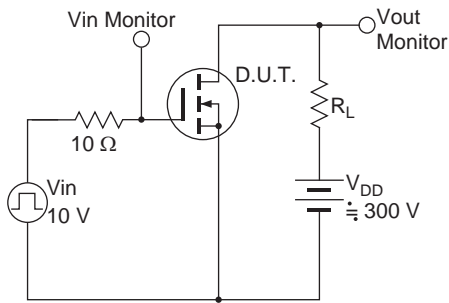
Gate to Source Cutoff Voltage vs. Case Temperature (Typical)



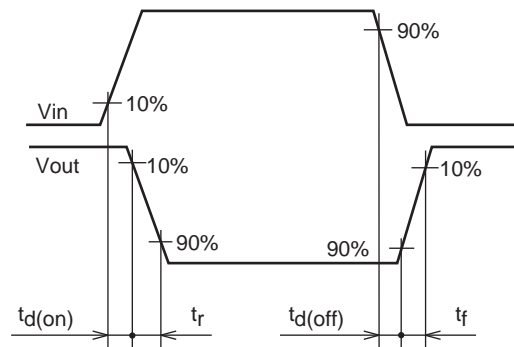
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit



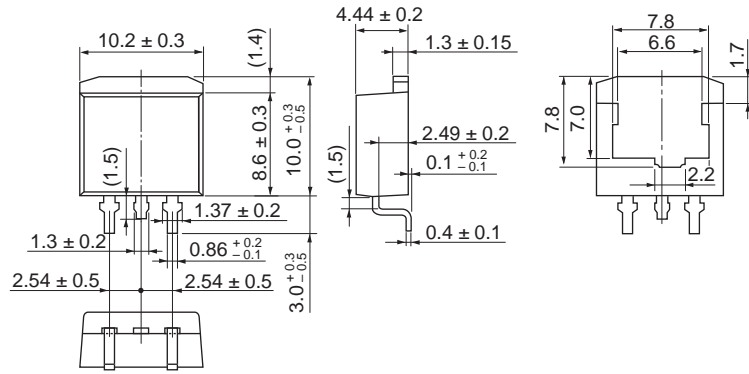
Waveform



Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
LDBPAK(S)-(1)	SC-83	PRSS0004AE-B	LDBPAK(S)-(1) / LDBPAK(S)-(1)V	1.30g

Unit: mm



Ordering Information

Orderable Part Number	Quantity	Shipping Container
RJK6024DPE-00#J3	1000 pcs	Taping

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