PM5355

S/UNI-622 DATASHEET ERRATA

Issue 7: March, 1998

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1. ISSUE 7 ERRATA

This Issue 7 contains errata applied to the PMC-941027 Issue 2 datasheet. The Issue 2 datasheet and Issue 7 errata supersede all prior editions and versions.

A change bar indicates a section that has been revised.

2. TIMING PARAMETER CHANGES

2.1. Minimum Prop Delays for LAIS, LOP, & PRDI page 221

Specification of the minimum propagation delays for LAIS, LOP, and PRDI have been removed.

Receive Alarm Output (Fig. 42)

Symbol	Description	Min	Max	Units
$t_{PGROCLK}$	PICLK High to GROCLK Edge	3	25	ns
t_{POOF}	PICLK High to OOF Valid	3	30	ns
t_{PLOF}	PICLK High to LOF Valid	3	30	ns
t_{PLOS}	PICLK High to LOS Valid	3	30	ns
t_{PLAIS}	PICLK High to LAIS Valid	~~3~~	30	ns
t_{PLRDI}	PICLK High to LRDI Valid	3	30	ns
t_{PLOP}	GROCLK Low to LOP Valid	~~3~~	25	ns
t_{PPAIS}	GROCLK Low to PAIS Valid	3	25	ns
P_{PRDI}	GROCLK Low to PRDI Valid	~~3~~	25	ns
t_{PLCD}	GROCLK Low to LCD Valid	3	25	ns

2.2. TGFC and TCP Parameters page 233

Specification of all parameters for TGFC and TCP are removed.

~~Transmit GFC Access (Fig. 48)~~

Symbol	Description	Min	Max	Units
~~tP_{TCP}~~	~~GTOCLK Low to TCP Valid~~	~~3~~	~~20~~	~~ns~~
~~tS_{TGFC}~~	~~TGFC Set-up time to GTOCLK~~	~~5~~		~~ns~~
~~tH_{TGFC}~~	~~TGFC Hold time to GTOCLK~~	~~1~~		~~ns~~

3. REGISTER CHANGES

3.1. Register 0x2C Page 105

This register is not supported.

~~Register 0x2C: SSTB Expected Clock Synchronization Message~~

~~Bit~~	~~Type~~	~~Function~~	~~Default~~
~~Bit 7~~	~~R/W~~	~~EZ1[7]~~	~~0~~
~~Bit 6~~	~~R/W~~	~~EZ1[6]~~	~~0~~
~~Bit 5~~	~~R/W~~	~~EZ1[5]~~	~~0~~
~~Bit 4~~	~~R/W~~	~~EZ1[4]~~	~~0~~
~~Bit 3~~	~~R/W~~	~~EZ1[3]~~	~~0~~
~~Bit 2~~	~~R/W~~	~~EZ1[2]~~	~~0~~
~~Bit 1~~	~~R/W~~	~~EZ1[1]~~	~~0~~
~~Bit 0~~	~~R/W~~	~~EZ1[0]~~	~~0~~

~~This register contains the expected clock synchronization message byte (Z1) in the receive stream.~~

EZ1[7:0]:

The EZ1[7] - EZ1[0] bits contain the expected clock synchronization message byte (Z1). EZ1[7:0] is compared with the clock synchronization message byte extracted from the receive stream. A clock synchronization message byte mismatch (CSMM) is declared if the accepted clock synchronization message byte differs from the expected clock synchronization message byte. If enabled, an interrupt is asserted upon declaration and removal of CSMM.

4. PIN DESCRIPTION CHANGES

4.1. Pin 74 TFP Page 13

TFP	Input	74	The active high transmit frame pulse (TFP) signal is used to align the SONET/SDH transport frame generated by the S/UNI-622 device to a system reference. TFP should be brought high for a single GTOCLK period every 810 (STS-1), 2430 (STS-3c), 2430 (STS-12c) GTOCLK cycles, or a multiple thereof. TFP ~~may~~ ***must*** be tied low if such synchronization is not required. The offset between a pulse applied to the TFP input and the resultant FPOUT pulse is 18 TCLK periods in STS-1 mode, 26 TCLK periods in STS-3c mode and 81 TCLK periods in STS-12c mode. TFP is sampled on the rising edge of GTOCLK.

4.2. Pin 68 TCP Page 27

~~TCP~~ ***Reserved***	Output	68	~~The transmit cell pulse (TCP) signal is provided to locate the most significant GFC bit (GFC[3]) of a cell's GFC field sourced on input TGFC. TCP pulses high for one GTOCLK period to identify the GTOCLK cycle before the cycle the GFC[3] bit is output on TGFC. TCP is updated on the falling edge of GTOCLK.~~***This pin is reserved.***

4.3. Pin 62 TGFC Page 27

~~TGFC~~ ***Reserved***	Input	62	~~The transmit generic flow control (TGFC) input contains GFC bits that can be inserted into the GFC fields of transmitted cells (including idle/unassigned cells). Insertion is controlled using bits in the TACP Fixed Stuff/GFC register. TGFC is sampled on the rising edge of GTOCLK.~~***This pin is reserved and must be tied to GND for proper operation of the S/UNI-622***

5. CLARIFICATION OF OPERATION

5.1. TCA May De-assert Early

The TCA signal may de-assert incorrectly. To avoid this problem the FIFORST bit in register 0x60 TACP Control/Status should be asserted after power-up or a hardware reset. A transmit FIFORST should be issued each time the TSOC changes boundaries. These boundary changes are identified by the TSOCI bit (bit 6 of the same register).

5.2. Cells Can Be Retransmitted

It has been found that a glitch on TFCLK may cause the S/UNI-622 to transmit previously transmitted cells. If this situation arises it can be cleared with a TXFIFO reset.

5.3. S1 (Z1) Byte Synchronization Message

The current GR-253-CORE (5.4.7.1) requires the byte validation to be done over 8 frames, instead of 5 frames as is done in the S/UNI-622. This, however, is still useful to be included, since it relieves the microprocessor from polling Reg. 0x0E, the Receive S1 (Z1) register every frame to validate the synchronization message.

5.4. RX FIFO Must Not Be Gapped During Last Two Words of a Cell

Do not de-assert RRDENB during the second to last word (or byte) of a cell. It has been found that the removal of RRDENB during the second to last word (or byte) of a cell will result in the loss of the last word (or byte).

5.5 Page 188: Changes to Bit Error Rate Monitor Settings

The recommended register settings for STS-1 mode should be as follows:

BER	Reg. 0x72	Reg. 0x73	Reg. 0x74	Reg. 0x75
10-4	A0	00	4F	00
10-5	B0	04	3E	00
10-6	E0	2E	3E	00

The recommended register settings for STS-3c mode should be as follows:

BER	Reg. 0x72	Reg. 0x73	Reg. 0x74	Reg. 0x75
10-4	34	00	4D	00
10-5	90	01	3E	00
10-6	A0	0F	3E	00
10-7	40	9C	3E	00

The recommended register settings for STS-12c mode should be as follows:

BER	Reg. 0x72	Reg. 0x73	Reg. 0x74	Reg. 0x75
10-4	20	00	CC	00
10-5	64	00	3E	00
10-6	E8	03	3E	00
10-7	10	27	3E	00

5.6 Page 149: STS-3c Application Information for the FIFORST bit.

In STS-3c mode of operation, the FIFORST bit in register 0x60: “TACP Control/Status” initializes the transmit FIFO. For correction operation, a FIFORST should be issues at the end of each initialization cycle (ie. at the end of the reset routine). A transmit FIFORST should also be issued each time TSOC changes boundaries. Boundary changes are identified by TSOCI (bit 6).

The FIFORST should be asserted for a minimum of 3.5us. (one cell period at 155Mbps).

6. CONTACTING PMC-SIERRA

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