National Semiconductor

January 1995

NM27P010 1,048,576-Bit (128k x 8) POP™ Processor Oriented CMOS EPROM

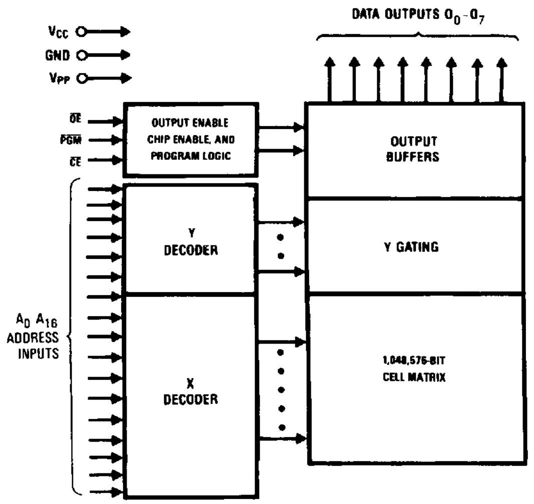
General Description

The NM27P010 is a 1 Mbit POP EPROM configured as 128k x 8. It's designed to simplify microprocessor interfacing while remaining compatible with standard EPROMs. It can reduce both wait states and glue logic when the specification improvements are taken advantage of in the system design. The NM27P010 is implemented in National's advanced CMOS EPROM process to provide excellent reliability and access times as fast as 70 ns. The interface improvements eliminate the need for additional devices to adapt the EPROM to the microprocessor and to eliminate wait states at the termination of the access cycle. Even with these improvements, the NM27P010 remains compatible with industry standard JEDEC pinout EPROMs.

Features

- Fast output turn off to eliminate wait states
- Extended data hold time for microprocessor compatibility
- High performance CMOS
  - 70 ns access time
- JEDEC standard pin configuration
  - 32-pin DIP package
  - 32-pin PLCC package
  - 32-pin TSOP package

Block Diagram



TL/D/12309-1

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POP™ is a trademark of National Semiconductor Corporation

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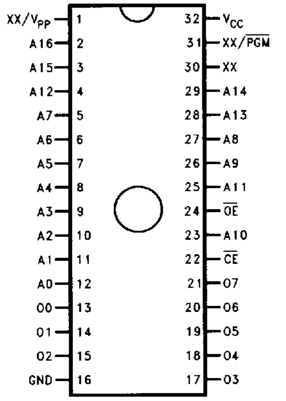
RRD-B20M15/Printed in U S A

Connection Diagrams

27P040	27P020	27P512
XX/V_{PP}	XX/V_{PP}	
A16	A16	
A15	A15	A15
A12	A12	A12
A7	A7	A7
A6	A6	A6
A5	A5	A5
A4	A4	A4
A3	A3	A3
A2	A2	A2
A1	A1	A1
A0	A0	A0
O0	O0	O0
O1	O1	O1
O2	O2	O2
GND	GND	GND

DIP
NM27P010



27P512	27P020	27P040
	V_{CC}	V_{CC}
	A18	A18
V_{CC}	A17	A17
A14	A14	A14
A13	A13	A13
A8	A8	A8
A9	A9	A9
A11	A11	A11
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A10	A10	A10
$\overline{CE}$	$\overline{CE}$	$\overline{CE/PGM}$
O7	O7	O7
O6	O6	O6
O5	O5	O5
O4	O4	O4
O3	O3	O3

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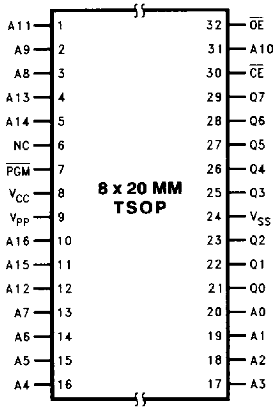
Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the NM27P010 pin

Top View

TSOP Pin Configuration



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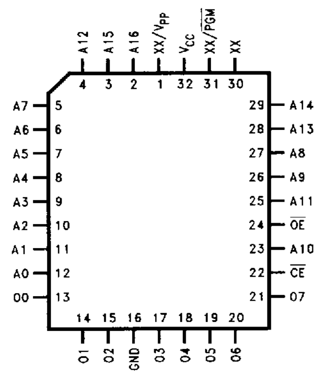
Top View

PLCC Pin Configuration



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Top View

Pin Names

A0–A16	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)

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Connection Diagrams (Continued)

Commercial Temperature Range
(0°C to +70°C) V_{CC} = 5V ±10%

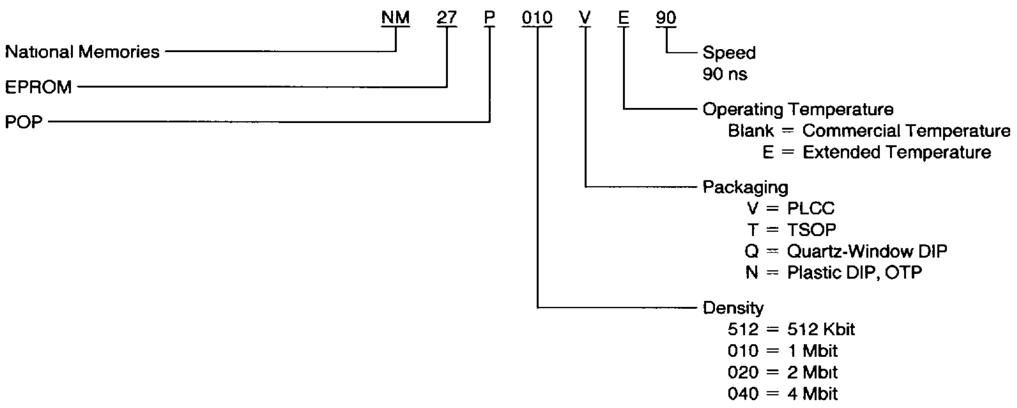
Parameter/Order Number	Access Time (ns)
NM27P010 Q, V, T 70	70
NM27P010 Q, V, T 90	90
NM27P010 Q, V, T 120	120
NM27P010 Q, V, T 150	150
NM27P010 Q, V, T 200	200

Note: All versions are guaranteed to function at slower speeds

Extended Temperature Range
(−40°C to +85°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27P010 QE, VE, TE 90	90
NM27P010 QE, VE, TE 120	120
NM27P010 QE, VE, TE 150	150
NM27P010 QE, VE, TE 200	200

Ordering Information



Absolute Maximum Ratings (Note 5)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +125°C
All Input Voltage except A9 with Respect to Ground	−0.6V to +7V
V_{PP} and A9 with Respect to Ground	−0.6V to +14V
V_{CC} Supply Voltage with Respect to Ground	−0.6V to +7V
All Output Voltages with Respect to Ground	V_{CC} + 10V to GND − 0.6V

Note 5: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device, This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.*

Operating Range

Range	Temperature	V_{CC}	Tolerance
Commercial	0°C to +70°C	+5V	±10%
Industrial	−40°C to +85°C	+5V	±10%

Read Operation

DC Electrical Characteristics Over operating range with $V_{PP} = V_{CC}$

Symbol	Parameter	Conditions		Min	Max	Units
V_{IL}	Input Low Voltage			−0.5	0.8	V
V_{IH}	Input High Level			2	V_{CC} + 1	V
V_{OL1}	Output Low Voltage (TTL)	I_{OL} = 2.1 mA			−0.4	V
V_{OH1}	Output High Voltage (TTL)	I_{OH} = −2.5 mA		2.4		V
V_{OL2}	Output Low Voltage (CMOS)	I_{OL} = 10 mA			0.1	V
V_{OH2}	Output High Voltage (CMOS)	I_{OH} = −10 μA		V_{CC} − 0.1		V
I_{SB}	V_{CC} Standby Current (CMOS) (Note 3)	$\overline{CE}$ = V_{CC} ± 0.3V			100	μA
I_{SB2}	V_{CC} Standby Current	V_{PP} = V_{CC}			1	mA
I_{CC}	V_{CC} Active Current (Note 1)	f = 5 MHz $\overline{CE}$, $\overline{OE}$ = V_{IL} I/O = 0 mA			35	mA
			AC (Note 4)		25	mA
I_{PP}	V_{PP} Supply Current	V_{PP} = V_{CC}			10	μA
V_{PP}	V_{PP} Read Voltage			V_{CC} − 0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or GND		−1	1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND		−10	10	μA

AC Electrical Characteristics Over operating range with $V_{PP} = V_{CC}$

Symbol	Parameter	70		90		120		150		200		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		70		90		120		150		200	ns
t_{CE}	CE to Output Delay		70		90		120		150		200	ns
t_{OE}	OE to Output Delay		35		40		40		50		50	ns
t_{DF}	Output Disable to Output Float (Note 2)		35		35		35		45		55	ns
t_{OH}	Output Hold from Addresses, CE or OE, Whichever Occurred First	7		7		7		7		7		ns

Note 1: The supply current is the sum of I_{CC} and I_{PP} The maximum current value is with outputs O0 to O7 unloaded

Note 2: This parameter is only sampled and is not 100% tested Output Float is defined as the point where data is no longer driven (see Timing Diagram)

Note 3: CMOS inputs. V_{IL} = GND ± 0 3V, V_{IH} = V_{CC} ± 0 3V

Note 4: AC denotes Advance CMOS and I_{CC} of 25 mA

Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	15	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	10	15	pF

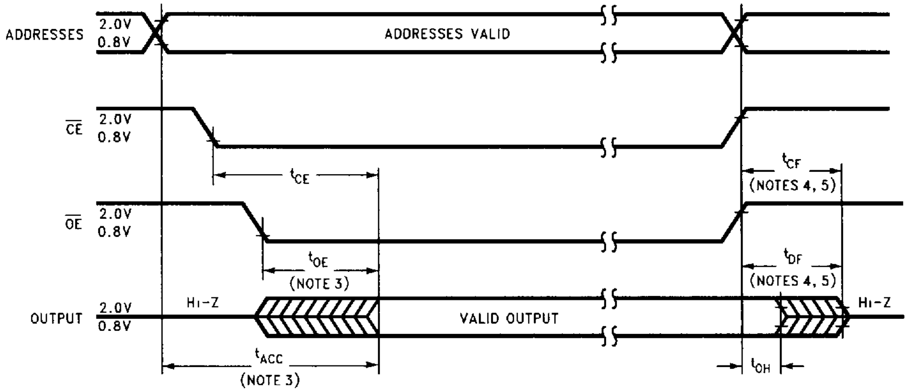
AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V

Timing Measurement Reference Level (Note 10)

Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7 and 9)



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Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Note 2: This parameter is only sampled and is not 100% tested

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}

Note 4: The t_{DF} and t_{CF} compare level is determined as follows High to TRI-STATE®, the measured V_{OH1} (DC) − 0 1V; Low to TRI-STATE, the measured V_{OL1} (DC) + 0.1V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1V to avoid latch-up and device damage

Note 8: 1 TTL Gate: I_{OL} = 1 6 mA, I_{OH} = −400 µA. C_L: 100 pF includes fixture capacitance. C_L: 35 pF for all 70 ns devices

Note 9: V_{PP} may be connected to V_{CC} except during programming

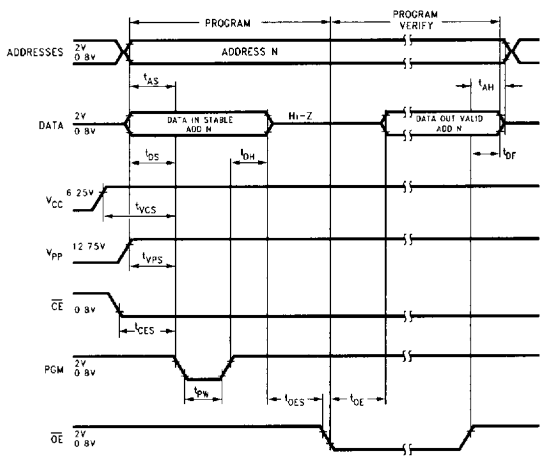
Note 10: Inputs and outputs can undershoot to −2V for 20 ns max

Note 11: Includes fixture capacitance.

DC Electrical Characteristics (Notes 1, 2, 3, 4 and 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			µs
t_{OES}	$\overline{OE}$ Setup Time		1			µs
t_{CES}	$\overline{CE}$ Setup Time	$\overline{OE} = V_{IH}$	1			µs
t_{DS}	Data Setup Time		1			µs
t_{VPS}	V_{PP} Setup Time		1			µs
t_{VCS}	V_{CC} Setup Time		1			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		1			µs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		60	µs
t_{PW}	Program Pulse Width		95	100	105	µs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				30	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage		−0.1	0	0.45	V
V_{IH}	Input High Voltage		2.4	4		V
t_{IN}	Input Timing Reference Voltage		0.8		2	V
t_{OUT}	Output Timing ReferenceVoltage		0.8		2	V

Programming Waveforms (Note 3)



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Note 1: National's standard product warranty applies only to devices programmed to specifications described herein

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification At least a 0 1 µF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device

Note 4: Programming and program verify are tested with the Fast Program Algorithm, at typical power supply voltages and timings

Note 5: During power up the PGM pin must be brought high ($\leq V_{IH}$) whether coincident with or before power is applied to V_{PP}

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 165 mW to 0.55 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the $\overline{OE}$ input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Tying

Because the EPROM is usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, it is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all selected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 µF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each address is programmed with a series of 100 µs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 µs pulse.

The EPROM must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple EPROMs in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled EPROM.

Program Inhibit

Programming multiple EPROMs in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel EPROMs may be common. A TTL low level program pulse applied to an EPROM's $\overline{CE}$ input with V_{PP} at 12.75V will program that EPROM. A TTL high level $\overline{CE}$ input inhibits the other EPROMs from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verity may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC}, except during programming and program verify.

After Programming

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

Manufacturer's Identification Code

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The manufacturer's identification code, shown in Table II, specifically identifies the manufacturer and device type. The code for NM27P010 is "8F86", where "8F" designates that it is made by National Semiconductor, and "86" designates a 1 Mbit (128k x 8) part.

The code is accessed by applying 12V ± 0.5V to address pin A9. Addresses A1–A8, A10–A16, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O0–O7. Proper code access is only guaranteed at 25°C ± 5°C.

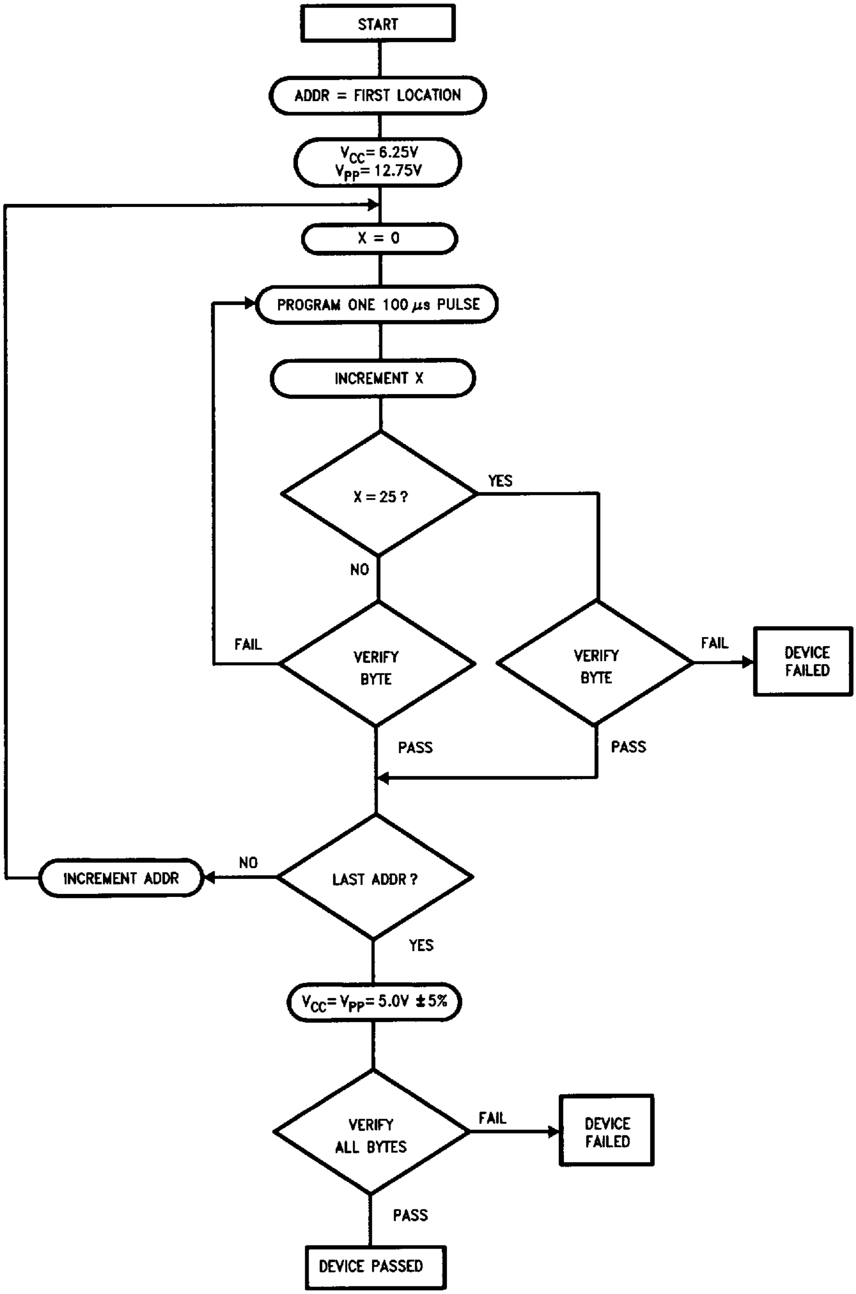

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FIGURE 1. Fast Programming Algorithm Flow Chart

Functional Description (Continued)

Erasure Characteristics

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be minimum of 15W-sec/cm2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increases as the square of the distance from the lamp. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

System Consideration

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

Mode Selection

The modes of operation of the NM27P010 are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 for device signature.

TABLE I. Mode Selection

Mode \ Pins	$\overline{CE}$	$\overline{PGM}$	$\overline{OE}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	X	V_{IL}	X (Note 1)	5V	D_{OUT}
Output Disable	X	X	V_{IH}	X	5V	High Z
Standby	V_{IH}	X	X	X	5V	High Z
Programming	V_{IL}	V_{IL} (Note 2)	V_{IH}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IH}	V_{IL}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	X	X	12.75V	6.25V	High Z

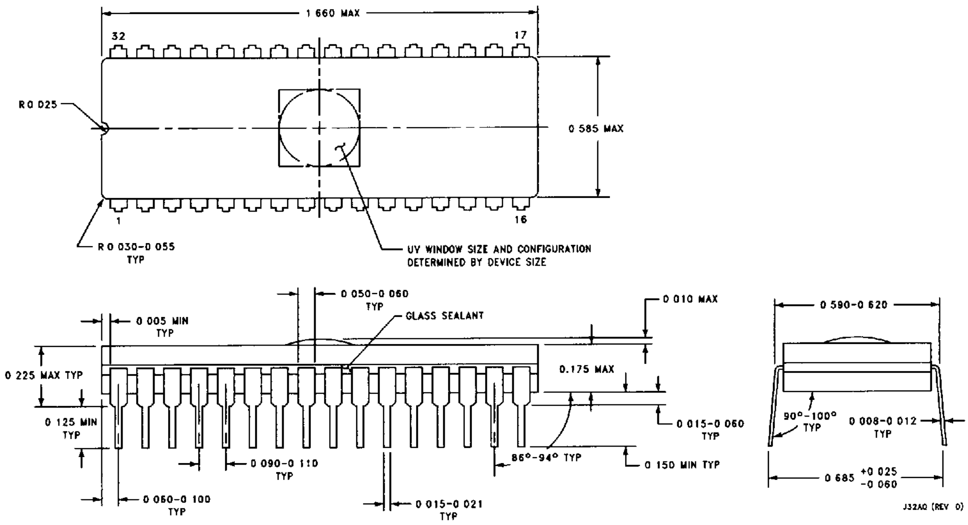
Note 1: X can be V_{IL} or V_{IH}

Note 2: PGM should not be DC value

TABLE II. Manufacturer's Identification Code

Pins	A0 (12)	A9 (26)	O7 (21)	O6 (19)	O5 (18)	O4 (17)	O3 (16)	O2 (15)	O1 (14)	O0 (13)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	1	0	0	0	0	1	1	0	86

Physical Dimensions inches (millimeters)



32-Lead Ceramic Dual-In-Line Package (Q)
Order Number NM27P010QXXX
NS Package Number J32AQ

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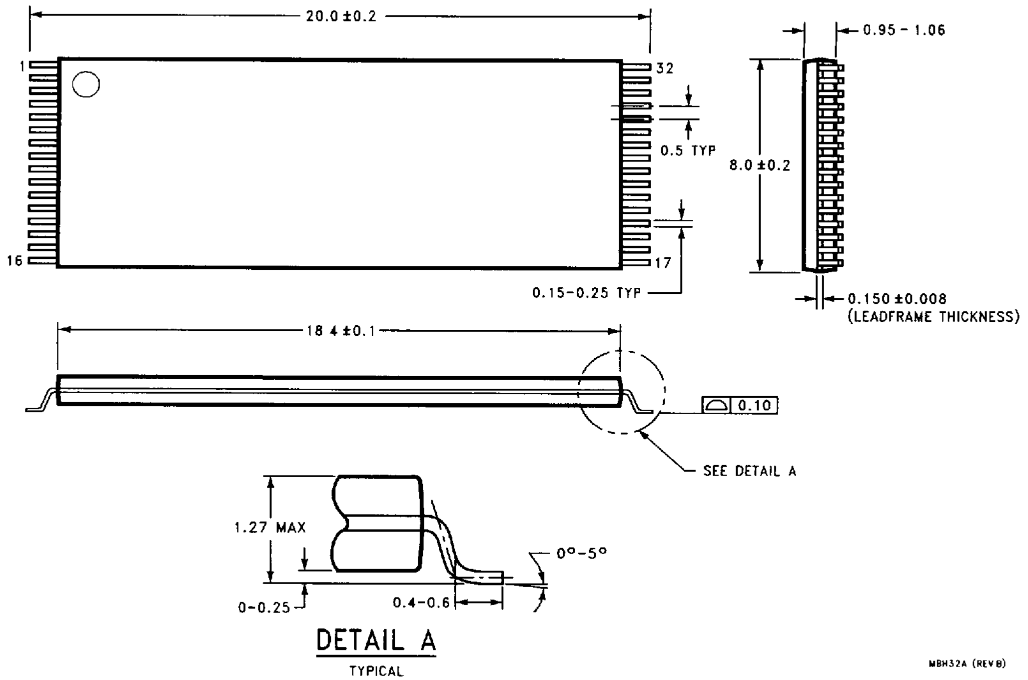
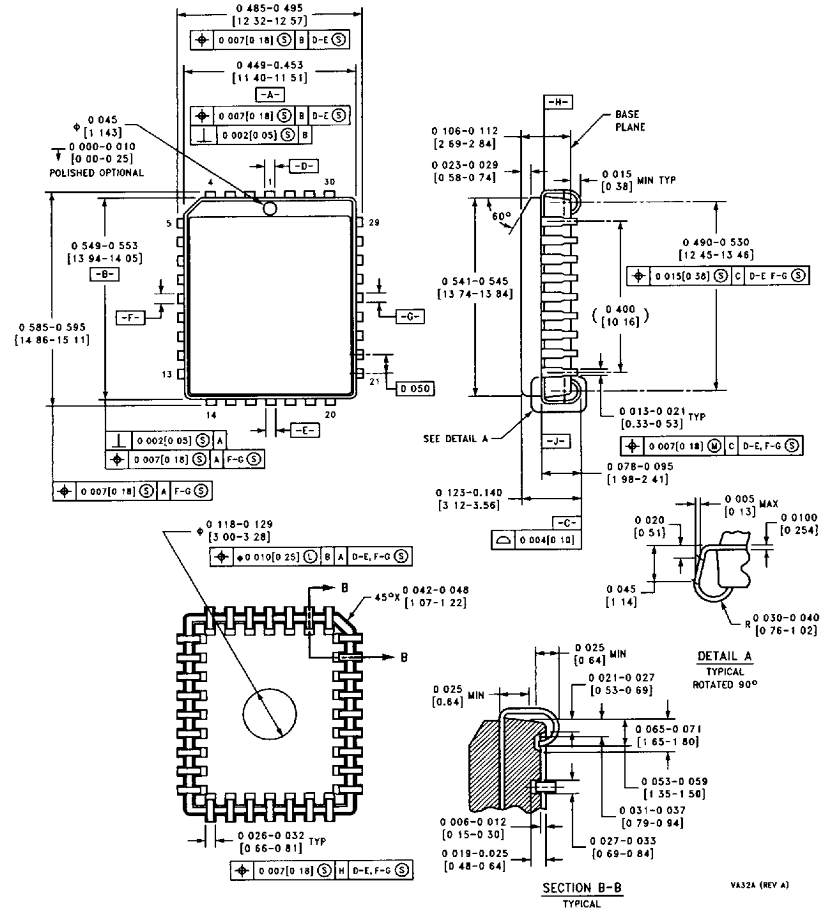
Physical Dimensions inches (millimeters) (Continued)



32-Lead Thin Small Outline Package
Order Number NM27P010TXXX
NS Package Number MBH32A

Lit # 112303-001

Physical Dimensions inches (millimeters) (Continued)



32-Lead PLCC Package
Order Number NM27P010VXXX
NS Package Number VA32A

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