19-3919; Rev 0; 1/06

EVALUATION KIT AVAILABLE

TFT LCD DC-DC Converter with Integrated Charge Pumps

General Description

The MAX8753 quadruple-output DC-DC converter provides the regulated voltages required by active-matrix, thin-film transistor (TFT), liquid-crystal displays (LCDs). It includes a high-power step-up regulator (V_{MAIN}), two low-power charge pumps (V_{POS} and V_{NEG}), and a low-voltage 300mA linear regulator (V_{LOGIC}).

The step-up DC-DC converter is a high-frequency (1MHz) current-mode regulator with a built-in power MOSFET that allows the use of ultra-small inductors and ceramic capacitors. It provides fast transient response to pulsed loads and includes an automatic pulse-skipping mode that increases efficiency over a wide-load current range. The 1.5A current limit allows a +10V output at more than 300mA from a +3.3V input.

The two charge pumps independently regulate one positive and one negative output voltage. The positive charge pump is a voltage tripler that accepts an input voltage up to +13V and delivers a 20mA output up to +28V without external switches or diodes. The negative charge pump inverts an input voltage up to +24V and delivers a 20mA negative output using external diodes.

The logic linear regulator converts the IC's +2.6V-to-+5.5V input to a regulated +2.5V or adjustable output. The MAX8753 is available in a 28-pin thin QFN package with a maximum thickness of 0.8mm for ultra-thin LCD panel design.

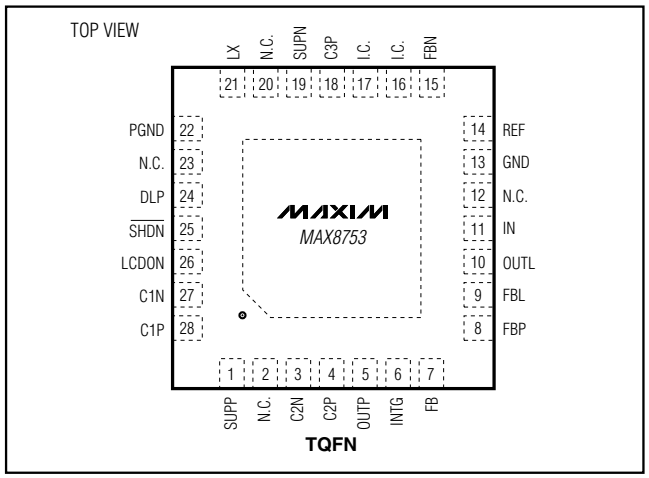
Applications

Notebook Computers, PDAs

Car Navigation Displays

LCD Monitors

Pin Configuration



Features

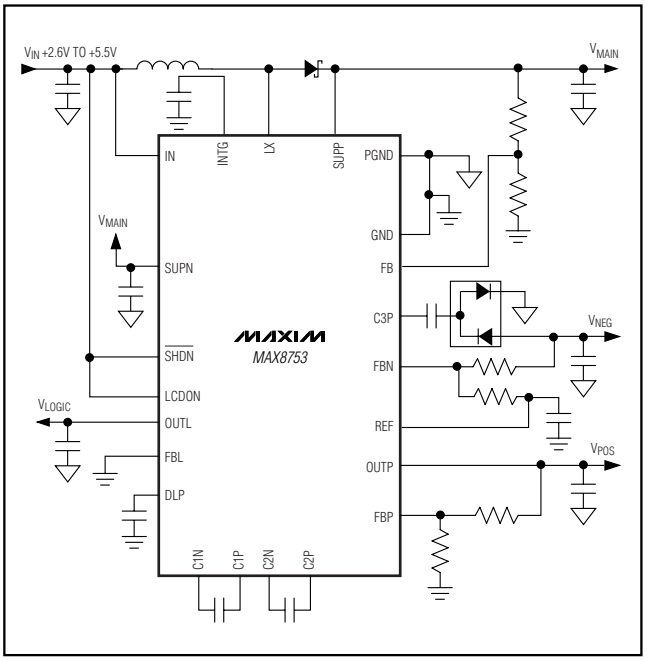
- ♦ **3 Integrated DC-DC Converters, 1 LDO**
- ♦ **1MHz Current-Mode PWM Boost Regulator**
  - **Up to +13V Main High-Power Output**
  - **±1% Accuracy**
  - **High Efficiency (90%)**
- ♦ **Dual Charge-Pump Outputs**
  - **No External Diodes for Positive Charge Pump**
  - **Up to +28V Positive Charge-Pump Output**
  - **Negative Charge-Pump Output**
- ♦ **300mA Logic Linear Regulator**
- ♦ **+2.6V to +5.5V Input Operating Range**
- ♦ **0.8mA Quiescent Current**
- ♦ **Internal Supply Sequencing and Soft-Start**
- ♦ **Thermal Protection**
- ♦ **Ultra-Thin, 28-Pin TQFN Package (0.8mm max)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8753ETI+	-40°C to 85°C	28 Thin QFN (5mm x 5mm)

+Denotes lead-free package.

Minimal Operating Circuit



TFT LCD DC-DC Converter with Integrated Charge Pumps

ABSOLUTE MAXIMUM RATINGS

IN, $\overline{SHDN}$, LCDON to GND .....-0.3V to +6V
DLP, OUTL, FBL, FBP, FBN, INTG, FB, REF to GND .....-0.3V to (V_{IN} + 0.3V)
PGND to GND .....-0.3V to +0.3V
LX to PGND .....-0.3V to +14V
SUPP to PGND .....-0.3V to +14V
C1N, C2N to PGND .....-0.3V to (V_{SUPP} + 0.3V)
OUTP to PGND .....(V_{SUPP} - 0.3V) to +30V
C1P to C1N, C2P to C2N, OUTP to C2P .....-0.3V to +14V
SUPN to PGND.....-0.3V to +30V
C3P to PGND.....-0.3V to (V_{SUPN} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
28-Pin 5mm x 5mm TQFN (derated 21.3mW/°C above +70°C).....1702mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{IN} = 3.0V, $\overline{SHDN}$ = LCDON = IN, V_{SUPP} = V_{SUPN} = 10V, PGND = GND, C_{REF} = 0.22µF, C_{INTG} = 470pF, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLIES						
Input Supply Range	V_{IN}		2.6		5.5	V
Input Undervoltage Threshold	V_{UVLO}	V_{IN} rising, 100mV hysteresis (typ)	2.1	2.3	2.5	V
IN Quiescent Supply Current	I_{IN}	V_{FB} = V_{FBP} = 1.5V, V_{FBN} = -0.2V		0.8	1.5	mA
IN Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{IN} = 5V		0.1	10	µA
SUPP Supply Range	V_{SUPP}		7		13	V
SUPP Quiescent Current	I_{SUPP}	V_{FBP} = 1.5V		0.4	0.8	mA
SUPP Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{SUPP} = 14V, OUTP floating		0.1	10	µA
SUPN Supply Range	V_{SUPN}		7		24	V
SUPN Quiescent Current	I_{SUPN}	V_{FBN} = -0.2V		0.4	0.8	mA
SUPN Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{SUPN} = 24V		0.1	10	µA
MAIN BOOST CONVERTER						
Output Voltage Range	V_{MAIN}		V_{IN}		13	V
FB Regulation Voltage	V_{FB}		1.232	1.245	1.258	V
FB Input Bias Current	I_{FB}	V_{FB} = 1.25V, INTG = GND		125	275	nA
FB Undervoltage Shutdown Threshold		FB falling	75	125	200	mV
Operating Frequency	f_{OSC}		0.85	1.00	1.15	MHz
Oscillator Maximum Duty Cycle			78	85	90	%
Load Regulation		I_{MAIN} = 0 to 100mA, V_{MAIN} = 10V		0.2		%
Line Regulation				0.1		%/V
INTG Transconductance				320		µS
LX Switch On-Resistance	$R_{LX(ON)}$	I_{LX} = 100mA		0.35	0.7	Ω
LX Leakage Current	I_{LX}	V_{LX} = 13V, $V_{\overline{SHDN}}$ = 0		0.01	20	µA

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 3.0V, $\overline{SHDN}$ = LCDON = IN, V_{SUPP} = V_{SUPN} = 10V, PGND = GND, C_{REF} = 0.22µF, C_{INTG} = 470pF, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LX Current Limit	$I_{LX(MAX)}$	Phase I = soft-start (1.0ms)		0.38		A
		Phase II = soft-start (1.0ms)		0.75		
		Phase III = soft-start (1.0ms)		1.13		
		Phase IV = fully on (> 3.0ms)	1.08	1.45	1.80	
Soft-Start Period	t_{SS}	Power-up to the end of phase III		3072 / f_{OSC}		s
POSITIVE CHARGE PUMP						
V_{SUPP} Input Supply Range	V_{SUPP}		7		13	V
V_{SUPP} Overvoltage Threshold		V_{SUPP} = rising, hysteresis (typ) = 200mV	13.2	13.6	14.0	V
OUTP Operating Range			V_{SUPP}		28	V
Operating Frequency				0.25 x f_{OSC}		Hz
FBP Regulation Voltage	V_{FBP}		1.213	1.250	1.287	V
FBP Line Regulation		V_{SUPP} = 8V to 12V, V_{OUTP} = 20V, I_{OUTP} = 5mA		10		mV
FBP Input Bias Current	I_{FBP}	V_{FBP} = 1.5V	-50		+50	nA
Soft-Start Period	V_{SSP}			1024 / f_{OSC}		s
C1N, C2N High-Side On-Resistance		I_{SOURCE} = 50mA			15	Ω
C1N, C2N Low-Side On-Resistance		I_{SINK} = 50mA			5	Ω
C1P Switch On-Resistance		I_{SOURCE} = 50mA			8	Ω
C2P Switch On-Resistance		I_{SOURCE} = 50mA			8	Ω
OUTP Switch On-Resistance		I_{SOURCE} = 50mA			8	Ω
NEGATIVE CHARGE PUMP						
V_{SUPN} Input Supply Range	V_{SUPN}		7		24	V
Operating Frequency				0.25 x f_{OSC}		Hz
FBN Regulation Voltage	V_{FBN}		213	250	287	mV
FBN Line Regulation		V_{SUPN} = 8V to 24V, V_{OUTN} = -10V, I_{OUTN} = 5mA		10		mV
FBN Input Bias Current	I_{FBN}	V_{FBN} = -0.05V	-50		+50	nA
Soft-Start Period	V_{SSN}			1024 / fosc		s
C3P High-Side On-Resistance		I_{SINK} = 50mA			15	Ω
C3P Low-Side On-Resistance		I_{SINK} = 50mA			10	Ω

TFT LCD DC-DC Converter with Integrated Charge Pumps

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 3.0V, $\overline{SHDN}$ = LCDON = IN, V_{SUPP} = V_{SUPN} = 10V, PGND = GND, C_{REF} = 0.22µF, C_{INTG} = 470pF, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{LOGIC} REGULATOR						
FBL Regulation Voltage	V_{FBL}	I_{OUTL} = 0 to 300mA	1.225	1.250	1.275	V
FBL Input Bias Current	I_{FBL}	V_{FBL} = 1.3V	-50		+50	nA
FBL Undervoltage Lockout	V_{FBL_UV}	V_{FBL} rising, hysteresis (typ) = 125mV	1.100	1.125	1.150	V
FBL Dual-Mode™ Threshold		V_{FBL} = rising	220	250	280	mV
OUTL Voltage Accuracy (Preset Mode)		V_{FBL} = GND, I_{OUTL} = 0 to 300mA	2.425	2.500	2.575	V
OUTL Load Regulation		I_{OUTL} = 0 to 300mA			-2	%
OUTL Line Regulation		V_{IN} = 2.6V to 5.5V		0.1		%
OUTL On-Resistance		V_{IN} = 3.3V, I_{OUTL} = 100mA		0.7	1.5	Ω
OUTL Short-Circuit Current		V_{OUTL} = GND, V_{FBL} = 1V		500		mA
REFERENCE						
Reference Voltage	V_{REF}	-2µA < I_{REF} < +50µA	1.231	1.250	1.269	V
Reference Undervoltage Threshold		V_{REF} rising	0.9	1.05	1.2	V
LOGIC SIGNALS						
LCDON, $\overline{SHDN}$ Input Low Voltage		Hysteresis = 0.15 x V_{IN} (typ)			0.9	V
LCDON, $\overline{SHDN}$ Input High Voltage			2.1			V
$\overline{SHDN}$ Input Current	$I_{\overline{SHDN}}$	$V_{\overline{SHDN}}$ = 0 to IN		0.01	1	µA
LCDON Input Current	I_{LCDON}	V_{LCDON} = 0 to IN		0.01	1	µA
SEQUENCING						
DLP Capacitor Charge Current		V_{DLP} = 0.5V	4	5	6	µA
DLP Turn-On Threshold		V_{DLP} = rising	1.20	1.25	1.30	V
DLP Discharge Switch On-Resistance		$V_{\overline{SHDN}}$ = 0		40		Ω
FAULT PROTECTION						
Duration to Trigger Fault	t_{FAULT}			50		ms
FBL Fault-Trip Level		Falling edge	0.95	1.01	1.08	V
FB, FBP Fault-Trip Level		Falling edge	1.07	1.10	1.14	V
FBN Fault-Trip Level		Rising edge	450	500	550	mV
Thermal-Shutdown Threshold		Typical hysteresis = 15°C		+160		°C

Dual-Mode is a trademark of Maxim Integrated Products, Inc.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{IN} = 3.0V, $\overline{SHDN}$ = LCDON = IN, V_{SUPP} = V_{SUPN} = 10V, PGND = GND, C_{REF} = 0.22µF, C_{INTG} = 470pF, **T_A = -40°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLIES						
Input Supply Range	V_{IN}		2.6		5.5	V
Input Undervoltage Threshold	V_{UVLO}	V_{IN} rising, 100mV hysteresis (typ)	2.1		2.5	V
IN Quiescent Supply Current	I_{IN}	V_{FB} = V_{FBP} = 1.5V, V_{FBN} = -0.2V			1.5	mA
SUPP Supply Range	V_{SUPP}		7		13	V
SUPP Quiescent Current	I_{SUPP}	V_{FBP} = 1.5V			0.8	mA
SUPN Supply Range	V_{SUPN}		7		24	V
SUPN Quiescent Current	I_{SUPN}	V_{FBN} = -0.2V			0.8	mA
MAIN BOOST CONVERTER						
Output Voltage Range	V_{MAIN}		V_{IN}		13	V
FB Regulation Voltage	V_{FB}		1.225		1.258	V
FB Undervoltage Shutdown Threshold		FB falling	75		200	mV
Operating Frequency	f_{OSC}		0.75		1.25	MHz
LX Switch On-Resistance	$R_{LX(ON)}$	I_{LX} = 100mA			0.7	Ω
LX Current Limit	$I_{LX(MAX)}$	Phase IV = fully on (> 3.0ms)	1.08		1.8	A
POSITIVE CHARGE PUMP						
V_{SUPP} Input Supply Range	V_{SUPP}		7		13	V
V_{SUPP} Overvoltage Threshold		V_{SUPP} = rising, hysteresis (typ) = 200mV	13.2		14.0	V
FBP Regulation Voltage	V_{FBP}		1.213		1.287	V
NEGATIVE CHARGE PUMP						
V_{SUPN} Input Supply Range	V_{SUPN}		7		24	V
FBN Regulation Voltage	V_{FBN}		213		287	mV
V_{LOGIC} REGULATOR						
FBL Regulation Voltage	V_{FBL}	I_{OUTL} = 0 to 300mA	1.220		1.275	V
OUTL On-Resistance		V_{IN} = 3.3V, I_{OUTL} = 100mA			1.5	Ω
REFERENCE						
Reference Voltage	V_{REF}	-2µA < I_{REF} < +50µA	1.225		1.269	V
Reference Undervoltage Threshold		V_{REF} rising	0.9		1.2	V
LOGIC SIGNALS						
LCDON, $\overline{SHDN}$ Input Low Voltage		Hysteresis = 0.15 x V_{IN} (typ)			0.9	V
LCDON, $\overline{SHDN}$ Input High Voltage			2.1			V

TFT LCD DC-DC Converter with Integrated Charge Pumps

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 3.0V, $\overline{SHDN}$ = LCDON = IN, V_{SUPP} = V_{SUPN} = 10V, PGND = GND, C_{REF} = 0.22µF, C_{INTG} = 470pF, **T_A = -40°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

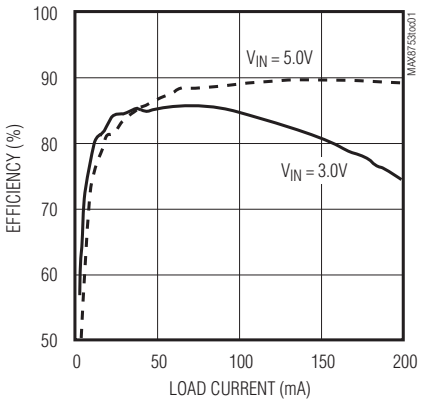
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SEQUENCING						
DLP Turn-On Threshold		V_{DLP} = rising	1.2		1.3	V
FBL Fault-Trip Level		Falling edge	0.95		1.08	V
FB, FBL, FBP Fault-Trip Level		Falling edge	1.07		1.14	V

Note 1: Specifications to -40°C are guaranteed by design, not production tested.

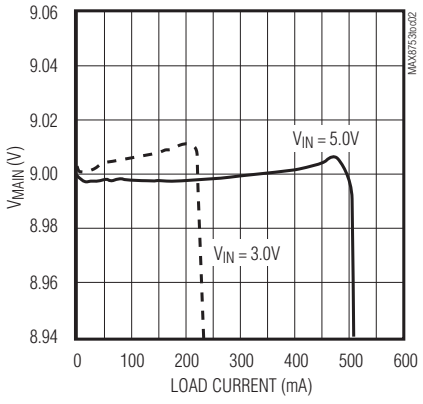
Typical Operating Characteristics

(Circuit of Figure 1, V_{IN} = 3V, V_{MAIN} = 9V, T_A = +25°C, unless otherwise noted.)

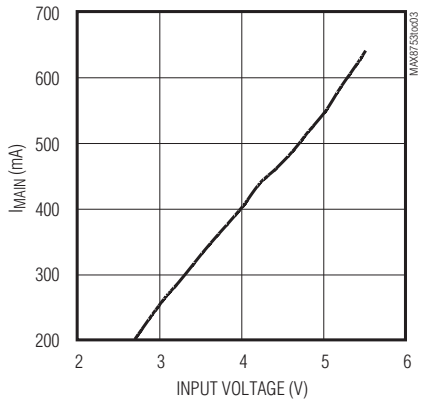
STEP-UP EFFICIENCY vs. LOAD CURRENT



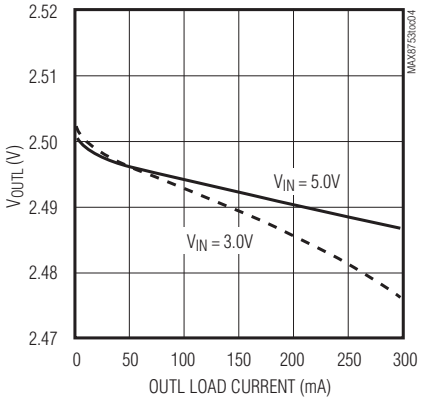
NORMALIZED V_{MAIN} vs. LOAD CURRENT



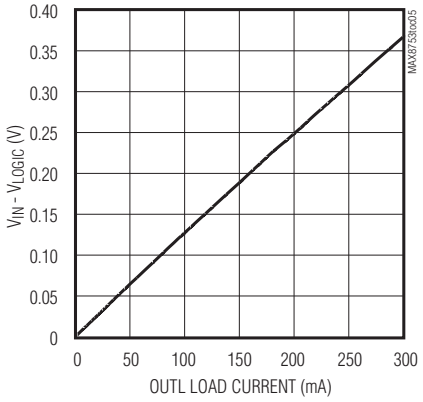
STEP-UP MAXIMUM OUTPUT CURRENT vs. INPUT VOLTAGE



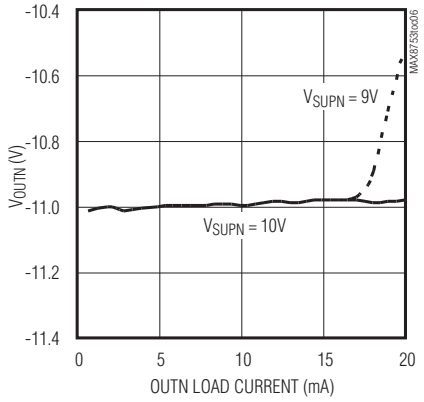
NORMALIZED OUTL VOLTAGE vs. OUTL LOAD CURRENT



OUTL DROPOUT VOLTAGE vs. OUTL LOAD CURRENT



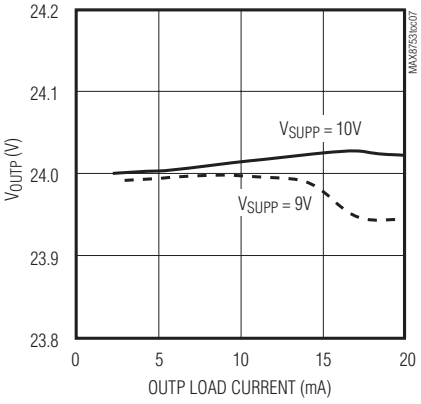
OUTN VOLTAGE vs. OUTN LOAD CURRENT



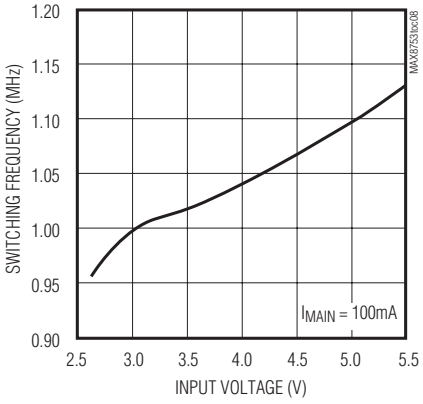
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 3V, V_{MAIN} = 9V, T_A = +25°C, unless otherwise noted.)

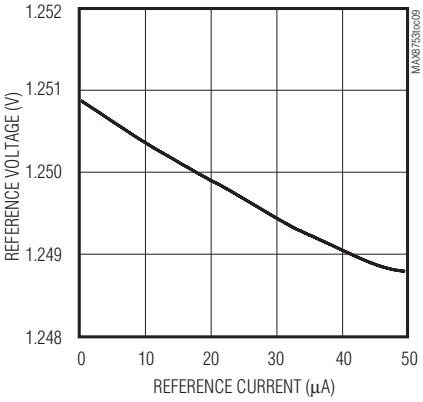
OUTP VOLTAGE vs. OUTP LOAD CURRENT



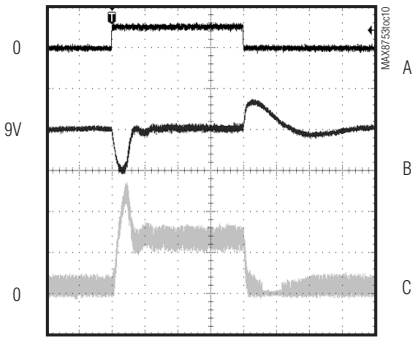
SWITCHING FREQUENCY vs. INPUT VOLTAGE



REFERENCE VOLTAGE vs. REFERENCE CURRENT

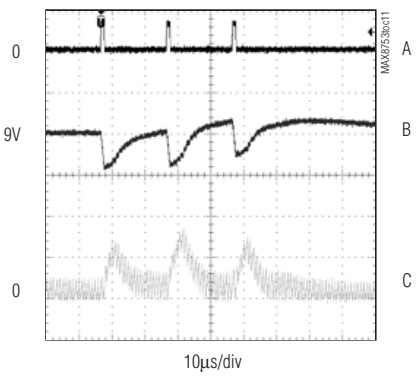


VMAIN TRANSIENT RESPONSE



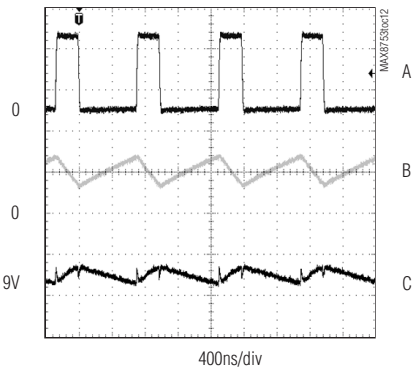
A. LOAD FET GATE, 5V/div
B. V_{MAIN}, 200mV/div
C. I_{LX}, 500mA/div
I_{MAIN} = 20mA TO 160mA

VMAIN 3-PULSE TRANSIENT RESPONSE



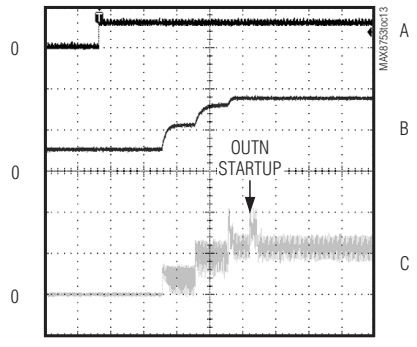
A. LOAD FET GATE, 5V/div
B. V_{MAIN}, 200mV/div
C. I_{LX}, 500mA/div
I_{MAIN} = 20mA TO 1A, 2µs PULSE

VMAIN SWITCHING WAVEFORMS



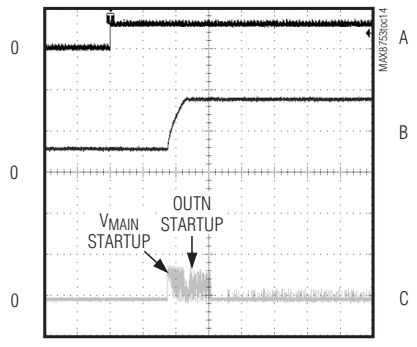
A. V_{LX}, 5V/div
B. I_{LX}, 500mA/div
C. V_{MAIN}, 50mV/div
I_{MAIN} = 160mA

VMAIN SOFT-START



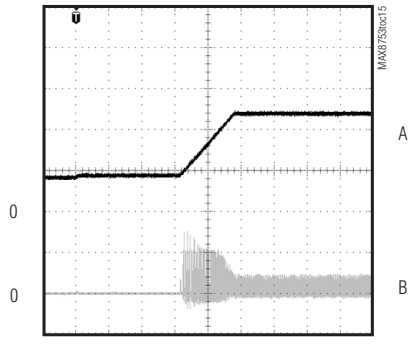
A. $\overline{SHDN}$, 5V/div
B. V_{MAIN}, 5V/div
C. I_{LX}, 500mA/div
I_{MAIN} = 160mA

VMAIN SOFT-START (NO LOAD)



A. $\overline{SHDN}$, 5V/div
B. V_{MAIN}, 5V/div
C. I_{LX}, 500mA/div

OUTP SOFT-START



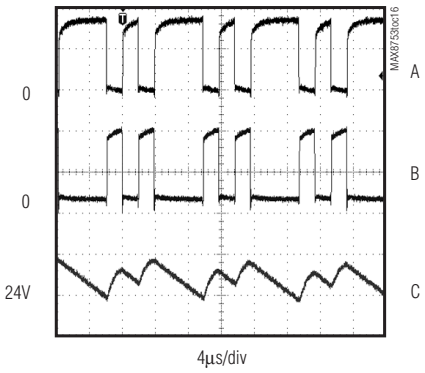
A. OUTP, 10V/div
B. I_{SUPP}, 500mA/div
I_{OUTP} = 20mA

TFT LCD DC-DC Converter with Integrated Charge Pumps

Typical Operating Characteristics (continued)

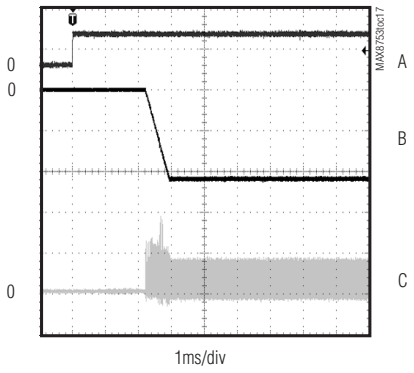
(Circuit of Figure 1, V_{IN} = 3V, V_{MAIN} = 9V, T_A = +25°C, unless otherwise noted.)

OUTP SWITCHING WAVEFORMS



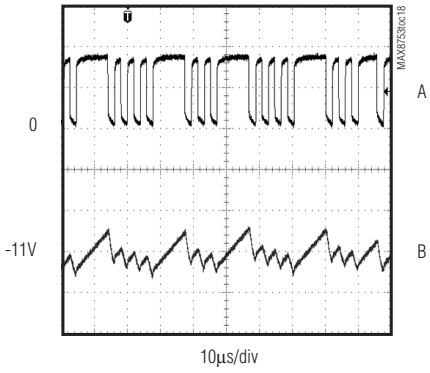
A. V_{CIN}, 5V/div
B. V_{C2N}, 5V/div
C. V_{OUTP}, 200mV/div
I_{OUTP} = 20mA

OUTN SOFT-START



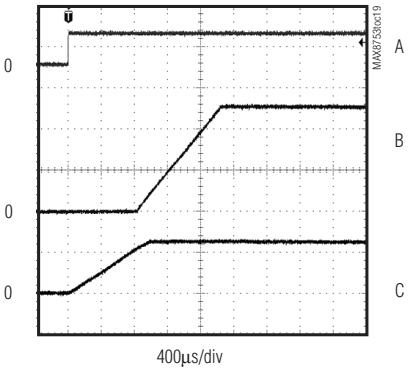
A. $\overline{SHDN}$, 5V/div
B. OUTN, 5V/div
C. I_{SUPN}, 200mA/div
I_{OUTN} = 20mA

OUTN SWITCHING WAVEFORMS



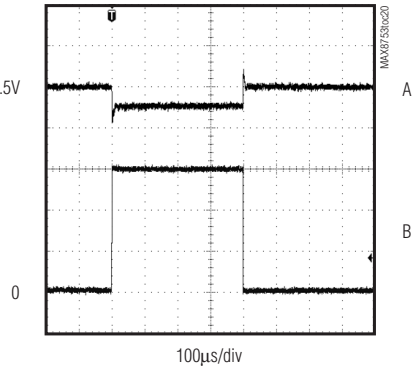
A. V_{C3P}, 5V/div
B. V_{OUTN}, 100mV/div
I_{OUTN} = 10mA

OUTL SOFT-START



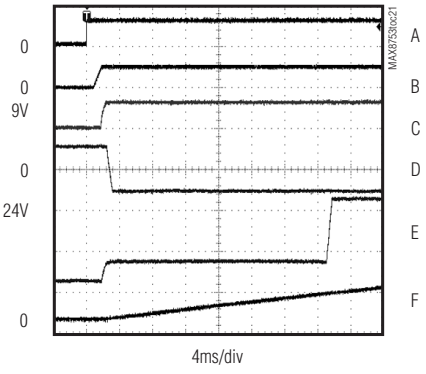
A. $\overline{SHDN}$, 5V/div
B. OUTL, 1V/div
C. V_{REF}, 1V/div
R_{OUTL} = 10Ω

OUTL TRANSIENT RESPONSE



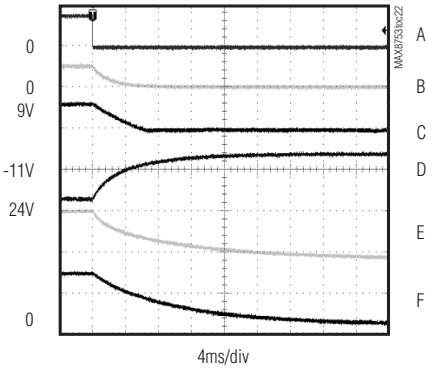
A. V_{OUTL}, 50V/div
B. I_{OUTL}, 100mA/div
I_{OUTL} = 10mA TO 300mA

POWER-UP SEQUENCING



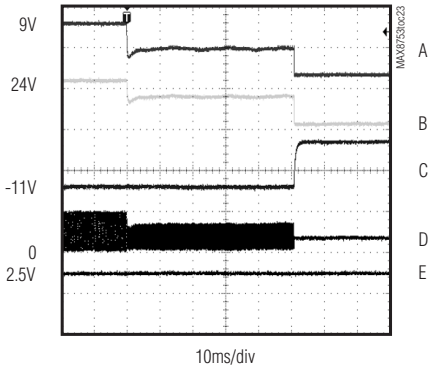
A. $\overline{SHDN}$, 5V/div
B. V_{OUTL}, 5V/div
C. V_{MAIN}, 10V/div
D. V_{OUTN}, 10V/div
E. V_{OUTP}, 10V/div
F. V_{DLP}, 2V/div

POWER-DOWN SEQUENCING



A. $\overline{SHDN}$, 5V/div
B. V_{OUTL}, 5V/div
C. V_{MAIN}, 10V/div
D. V_{OUTN}, 10V/div
E. V_{OUTP}, 10V/div
F. V_{REF}, 1V/div

FAULT TIMER



A. V_{MAIN}, 5V/div
B. V_{OUTP}, 20V/div
C. V_{OUTN}, 10V/div
D. V_{LX}, 10V/div
E. V_{OUTL}, 2V/div
R_{MAIN} = OPEN TO 18Ω

Pin Description

PIN	NAME	FUNCTION
1	SUPP	Positive Charge-Pump Supply Voltage. Bypass to PGND with a 0.1µF capacitor.
2, 12, 20, 23	N.C.	No connection. Not internally connected.
3	C2N	Negative Terminal of Flying Capacitor C2
4	C2P	Positive Terminal of Flying Capacitor C2
5	OUTP	Positive Charge-Pump Output
6	INTG	Step-Up Regulator Integrator Output. Connect a 470pF capacitor from INTG to GND.
7	FB	Step-Up Converter Feedback Input. Regulates to 1.245V (nominal). Connect a resistor-divider from the output (V_{MAIN}) to FB to analog ground (GND). Place the resistor-divider within 5mm of FB.
8	FBP	Positive Charge-Pump Feedback Input. Regulates to 1.25V (nominal). Connect a resistor-divider from the output (OUTP) to FBP to analog ground (GND). Place the resistor-divider within 5mm of FBP.
9	FBL	Logic Linear Regulator Dual-Mode Feedback Input. Connect FBL to GND to select the 2.5V preset linear regulator output voltage (OUTL). Connect FBL to the center tap of a resistive voltage-divider between OUTL and GND to set an adjustable output voltage. In adjustable mode, FBL is regulated at 1.25V nominal. Place the resistive divider within 5mm of FBL.
10	OUTL	Logic Linear Regulator Output. Output of the 2.5V or adjustable linear regulator. Bypass to GND with a 10µF (min) capacitor.
11	IN	Supply Input. +2.6V to +5.5V input range. Supply input for the IC and input for the internal logic linear regulator. Bypass to GND with a 0.1µF capacitor within 5mm of the IC pins.
13	GND	Analog Ground. Connect to power ground (PGND) underneath the IC.
14	REF	Internal Reference Output. Bypass REF to GND with a 0.22µF (min) capacitor. REF can supply up to 50µA to an external load.
15	FBN	Negative Charge-Pump Feedback Input. Connect a resistor-divider from the output (OUTN) to FBN to the reference output (REF). Place the resistor-divider within 5mm of FBN.
16, 17	I.C.	Internally Connected. Make no connection to this pin.
18	C3P	Positive Terminal of Flying Capacitor C3
19	SUPN	Negative Charge-Pump Supply Voltage. Bypass to PGND with a 0.1µF capacitor.
21	LX	Power MOSFET n-Channel Drain and Switching Node. Connect the inductor and catch diode to LX and minimize the trace area for lowest EMI.
22	PGND	Power Ground. PGND is the source of the main boost/n-channel power MOSFET. Connect PGND to the output capacitor ground terminals through a short, wide PC board trace.
24	DLP	Positive Charge-Pump Startup Delay Input. Connect a capacitor from DLP to GND to set the delay time. A 5µA current source charges C_{DLP}. DLP is pulled to GND by a 20Ω switch when shut down.
25	$\overline{SHDN}$	Active-Low Shutdown Control Input. All outputs are disabled when $\overline{SHDN}$ is low. When $\overline{SHDN}$ is high, REF and OUTL are enabled and the LCD supplies can be enabled if LCDON is high.
26	LCDON	LCD Supply Enable Input. All LCD supply outputs (MAIN, OUTN, and OUTP) are disabled when LCDON is low. REF and OUTL are unaffected by LCDON.
27	C1N	Negative Terminal of Flying Capacitor C1
28	C1P	Positive Terminal of Flying Capacitor C1

TFT LCD DC-DC Converter with Integrated Charge Pumps

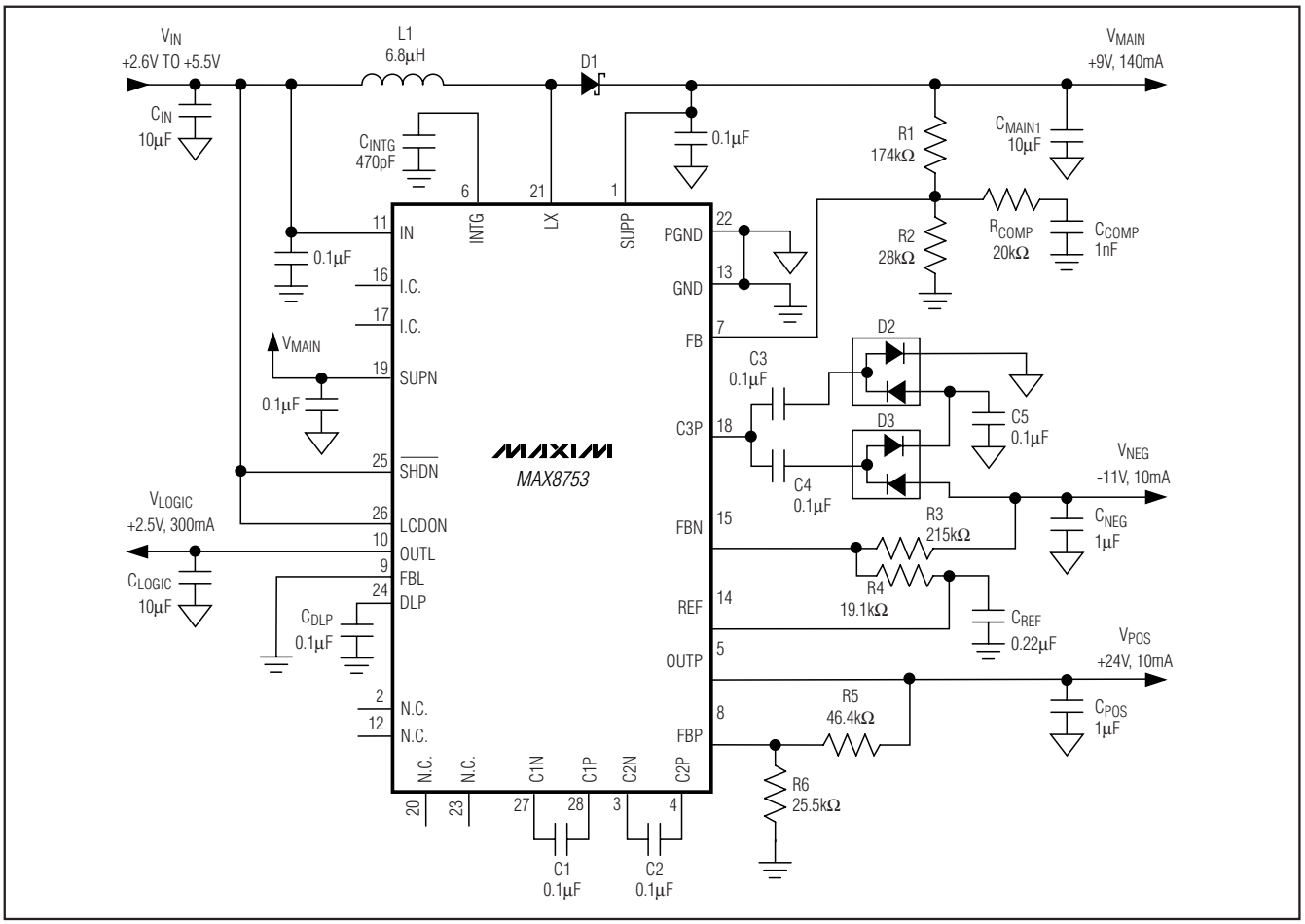


Figure 1. Typical Operating Circuit

Typical Operating Circuit

The MAX8753 typical application circuit (Figure 1) generates a +2.5V logic supply, a +9V source driver supply, and +24V and -11V gate-driver supplies for TFT displays. The input voltage range for the IC is from +2.6V to +5.5V.

Table 1 lists the recommended components and Table 2 lists the contact information for component suppliers.

Table 1. Critical Component List

DESIGNATION	DESCRIPTION
C_{IN}, C_{LOGIC}	10µF, 6.3V X5R ceramic capacitors (0603) TDK C1608X5R0J106M
C_{MAIN}	10µF ±20%, 16V X5R ceramic capacitor (1210) Taiyo Yuden EMK325 BJ106KD
D1	3A, 30V Schottky diode (M-flat) Toshiba CMS02
D2, D3	200mA, 100V, dual ultra-fast diodes (SOT23) Fairchild MMBD4148SE
L1	6.8µH, 1.0A inductor Sumida CDH38D09HP

Table 2. Component Suppliers

SUPPLIER	PHONE	FAX	WEBSITE
Fairchild	408-822-2000	408-822-2102	www.fairchildsemi.com
Sumida	847-545-6700	847-545-6720	www.sumida.com
Taiyo Yuden	408-573-4150	408-573-4159	www.t-yuden.com
TDK	847-803-6100	847-390-4405	www.component.tdk.com
Toshiba	949-455-2000	949-859-3963	www.toshiba.com/taec

Detailed Description

The MAX8753 quadruple-output DC-DC converter provides the regulated voltages required by active-matrix, TFT LCDs. Figure 1 shows the typical operating circuit. It includes a high-power step-up regulator (V_{MAIN}), two low-power charge pumps (V_{POS} and V_{NEG}), and a low-voltage, 300mA linear regulator (V_{LOGIC}). The primary boost converter uses an internal n-channel MOSFET to provide maximum efficiency and to minimize the number of external components. The output voltage of the main boost converter (V_{MAIN}) can be set from V_{IN} to 13V with external resistors. The positive charge pump regulates a positive output (V_{POS}) without external switches or diodes. The negative charge pump regulates a negative output (V_{NEG}) with external diodes. A proprietary regulation algorithm minimizes output ripple, as well as capacitor sizes for both charge pumps. Also included in the MAX8753 is a precision 1.25V reference that sources up to 50µA, logic shutdown, soft-start, power-up sequencing, and fault detection. Figure 2 is the MAX8753 functional diagram.

Main Step-Up Regulator

The main step-up regulator employs a current-mode, fixed-frequency PWM architecture to maximize loop bandwidth and provide fast transient response to pulsed loads and TFT LCD panel source driver applications. The high switching frequency (1MHz) allows the use of low-profile inductors and ceramic capacitors to minimize the thickness of LCD panel designs. The integrated high-efficiency MOSFET and the IC's built-in, digital, soft-start function reduces the number of external components required while controlling inrush current. The output voltage can be set from V_{IN} to 13V with an external resistive voltage-divider.

The regulator controls the output voltage and the power delivered to the output by modulating the duty cycle (D) of the internal power MOSFET in each switching cycle. The duty cycle of the MOSFET is approximated by:

$$D \approx \frac{V_{MAIN} - V_{IN}}{V_{MAIN}}$$

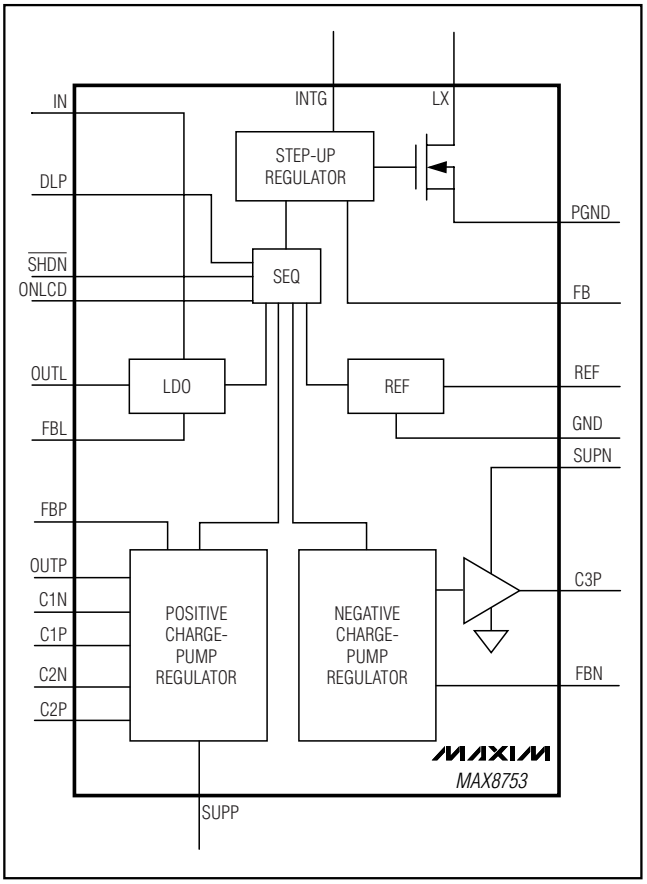


Figure 2. Functional Diagram

Figure 3 shows the block diagram of the step-up regulator. A transconductance error amplifier compares the signal at FB to 1.24V and changes the COMP output. The voltage at COMP determines the current trip point each time the internal MOSFET turns on. As the load varies, the transconductance error amplifier sources or sinks current to the COMP output accordingly to produce the inductor peak current necessary to service the load. To maintain stability at high duty cycles, a

TFT LCD DC-DC Converter with Integrated Charge Pumps

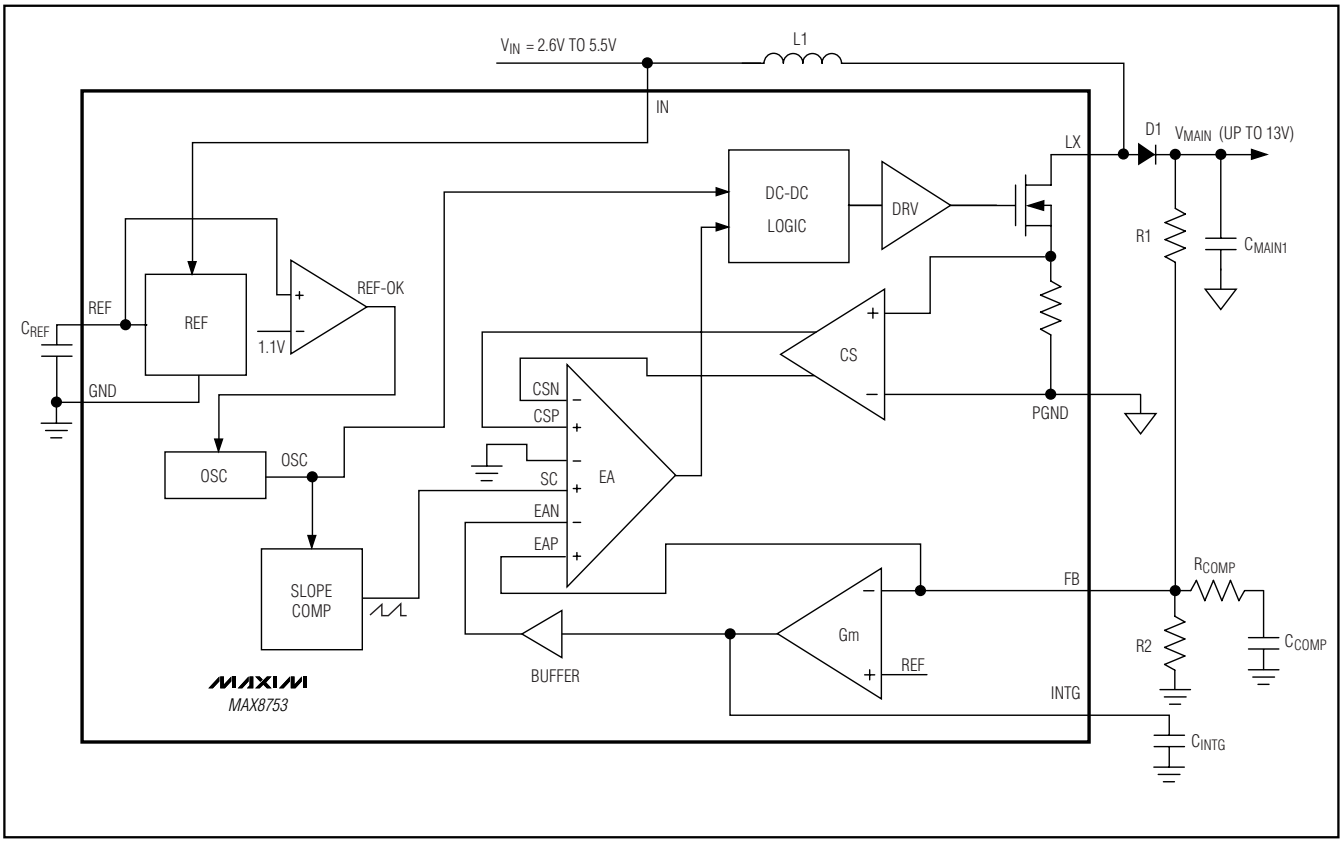


Figure 3. Step-Up Regulator Block Diagram

slope compensation signal is summed with the current-sense and feedback signals.

On the rising edge of the internal clock, the controller sets a flip-flop, turning on the n-channel MOSFET and applying the input voltage across the inductor. The current through the inductor ramps up linearly, storing energy in its magnetic field. Once the sum of the current-feedback signal and the slope compensation exceed the COMP voltage, the controller resets the flip-flop, and turns off the MOSFET. Since the inductor current is continuous, a transverse potential develops across the inductor (L1) that turns on the diode (D1). The voltage across the inductor then becomes the difference between the output voltage and the input voltage. This discharge condition forces the current through the inductor to ramp back down, transferring the energy stored in the magnetic field to the output capacitor and the load. The MOSFET remains off for the rest of the clock cycle.

Positive Charge-Pump Regulator

The positive charge-pump regulator is typically used to generate the positive supply rail for the TFT LCD gate-driver ICs (Figure 4). The output voltage is set with an external resistive voltage-divider from its output to GND with the midpoint connected to FBP. The positive charge pump is a voltage tripler that accepts an input voltage up to +13V and delivers a 20mA output up to +28V without external switches or diodes.

During the first half-cycle (CLK is low), C1N pin is connected to the ground, which allows V_{SUPP} to charge up the first flying capacitor C1 through diode D1. The amount of charge transferred from V_{SUPP} to C1 is determined by the on-resistance of N1, which varies according to the output of the feedback error amplifier. During the second half-cycle (CLK is high), C1N is connected to V_{SUPP} through P1, level shifting C1 by V_{SUPP} volts. The on-resistance of P1 is also controlled by the output of the feedback error amplifier. Meanwhile, CLKB becomes low, pulling C2N to the ground. This connects C1 in parallel with the second flying capacitor

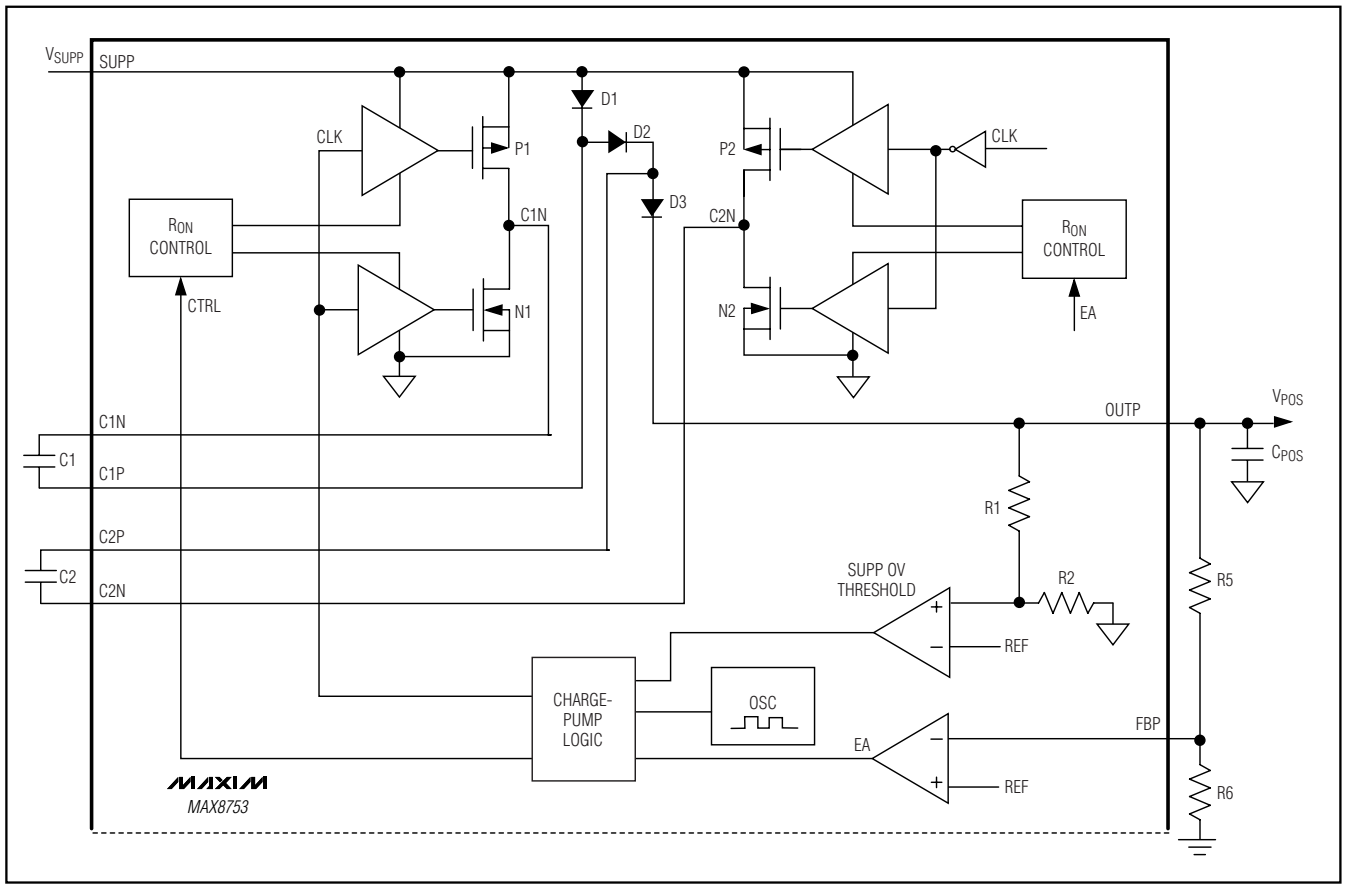


Figure 4. Positive Charge-Pump Regulator Block Diagram

C2. If the voltage across C2 plus a diode drop (V_{C2} + V_{DIODE}) is smaller than the first level-shifted flying capacitor voltage (V_{C1} + V_{SUPP}), charge flows from C1 to C2 until diode D2 turns off. Similarly, when CLKB becomes high, C2 is also level shifted by V_{SUPP} volts. This connects C2 in parallel with the reservoir capacitor C_{POS}. If the voltage across C_{POS} plus a diode drop (V_{POS} + V_{DIODE}) is smaller than the second level-shifted flying capacitor voltage (V_{C2} + V_{SUPP}), charge flows from C2 to C_{POS} until diode D3 turns off.

Negative Charge-Pump Regulator

The negative charge-pump regulator is typically used to generate the negative supply rail for the TFT LCD gate-driver ICs. The output voltage is set with an external resistive voltage-divider from its output to REF with the midpoint connected to FBN. The number of charge-pump stages and the setting of the feedback divider determine the output of the negative charge-pump regulator. The charge-pump controller includes a high-side p-channel MOSFET (P3) and a low-side n-channel MOSFET (N3) to control the power transfer as shown in Figure 5. The negative charge pump can also be configured as a multiple-stage charge pump. The required number of stages (n_{neg}) is determined by V_{SUPN} and the desired negative output voltage. Figure 1 gives an example with a two-stage negative charge pump.

In Figure 5, during the first half-cycle, the p-channel MOSFET turns on and flying capacitor C3 charges to V_{SUPN} minus a diode drop. During the second half-cycle, the p-channel MOSFET turns off, and the n-channel MOSFET turns on, level shifting C3. This connects C3 in parallel with the reservoir capacitor C_{NEG}. If the voltage across C3 minus a diode drop is lower than the voltage across C_{NEG}, charge flows from C3 to C_{NEG} until the diode turns off. The amount of charge transferred to the output is controlled by the variable n-channel on-resistance.

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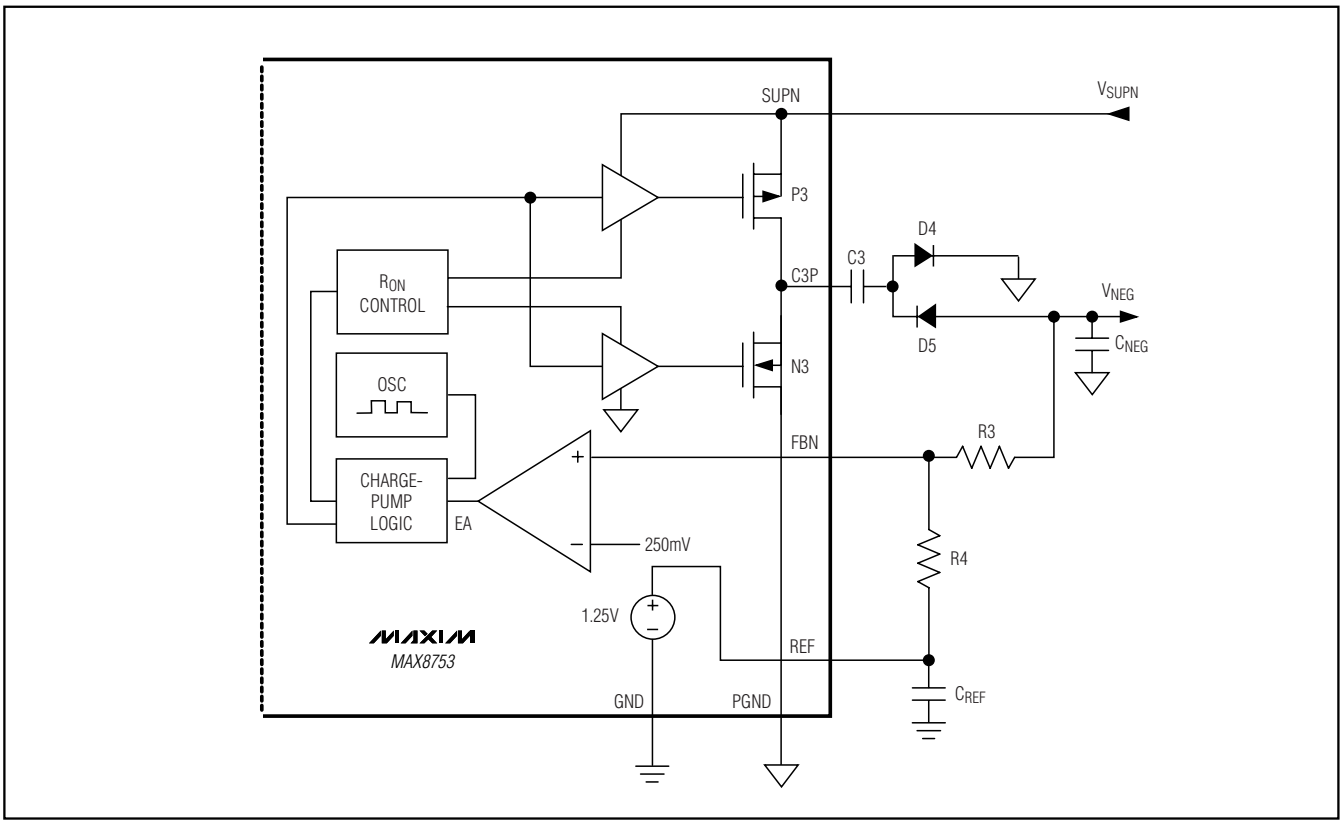

Figure 5. Negative Charge-Pump Regulator Block Diagram

Linear Regulator

The MAX8753 contains a linear regulator that uses an internal pMOS transistor to supply load currents up to 300mA. Connect FBL to GND to set the linear regulator output to 2.5V. Connect an external resistive voltage-divider between the regulator output and GND with the midpoint connected to FBL to adjust the linear-regulator output. An error amplifier compares the FBL voltage with the 1.25V internal reference voltage and amplifies the difference. If the feedback voltage is higher than the reference voltage, the controller lowers the gate voltage of the pMOS transistor, which reduces the amount of current delivered to the output. If the feedback voltage is too low, the device increases the pMOS transistor's gate voltage, which allows more current to pass to the output and raises the output voltage. The linear regulator also includes an output current limit that protects the internal pass transistor against short circuits.

The linear regulator is enabled whenever REF is in regulation and $\overline{SHDN}$ is logic-high.

The linear regulator current-limit circuitry monitors the current flowing through the internal pass transistor. The internal current limit is approximately 500mA. The linear regulator output declines when it is not able to supply the load current. If the FBL voltage drops below 0.75V, the current limit folds back to approximately 100mA.

Reference Voltage (REF)

The reference output is nominally 1.25V and can source up to 50µA. Bypass REF with a 0.22µF ceramic capacitor connected between REF and GND. The reference remains disabled in shutdown.

Power-Up Sequence and Shutdown Control

When the MAX8753 is powered up, all outputs are disabled as long as $\overline{SHDN}$ is low. After $\overline{SHDN}$ is logic-high, the reference and the linear regulator power up first. The main DC-DC step-up converter, the negative

charge pump, and the positive charge pump remain disabled until LCDON is high. When LCDON is logic-high, the main DC-DC step-up converter powers up with soft-start enabled. Once the main step-up converter reaches regulation, the negative charge pump turns on.

When the main step-up converter reaches regulation, the positive charge-pump regulator delay block is enabled. An internal current source starts charging the DLP capacitor. The voltage on DLP linearly rises because of the constant-charging current. When V_{DLP} goes above V_{REF}, the switch control block is enabled, and the positive charge-pump regulator begins its soft-start. After the positive charge-pump regulator's soft-start is completed, the fault protection of the positive charge-pump regulator is also enabled.

A logic-low level on LCDON disables the main BOOST converter, the negative charge pump, and the positive charge pump. The output capacitance and load current determine the rate at which each output voltage decays. The linear regulator and the reference remain enabled unless $\overline{SHDN}$ drops below its logic-low threshold. When shut down, the reference turns off and the IC supply current drops to 0.1µA to maximize battery life in portable applications. Do not leave $\overline{SHDN}$ floating. If unused, connect $\overline{SHDN}$ to IN.

Output Fault Protection

During steady-state operation if the output of the linear regulator, the step-up regulator, or either of the charge-pump regulator outputs, does not exceed its respective fault-detection threshold, the MAX8753 activates an internal fault timer. If any condition or combination of conditions indicates a continuous fault for the fault timer duration (50ms typ), the MAX8753 sets the fault latch, shutting down all the outputs except the reference. Once the fault condition is removed, cycle the input voltage or toggle $\overline{SHDN}$ to clear the fault latch and reactivate the device. Each regulator's fault-detection circuit is disabled during the regulator's soft-start time.

Thermal-Overload Protection

The thermal-overload protection prevents excessive power dissipation from overheating the IC. If the junction temperature exceeds +160°C, a thermal sensor immediately activates the thermal fault protection, which shuts down all the outputs, allowing the device to cool down. Once the device cools down, cycle the input voltage to clear the thermal fault latch and reactivate the device.

Design Procedure

Main Step-Up Regulator

Inductor Selection

The minimum inductance value, peak current rating, and series resistance are factors to consider when selecting the inductor. These factors influence the converter's efficiency, maximum output load capability, transient response time, and output voltage ripple. Physical size and cost are also important factors to be considered.

The maximum output current, input voltage, output voltage, and switching frequency determine the inductor value. Very high inductance values minimize the current ripple and therefore reduce the peak current, which decreases core losses in the inductor and I^2R losses in the entire power path. However, large inductor values also require more energy storage and more turns of wire, which increase physical size and can increase I^2R losses in the inductor. Low inductance values decrease the physical size but increase the current ripple and peak current. Finding the best inductor involves choosing the best compromise between circuit efficiency, inductor size, and cost.

The equations used here include a constant LIR, which is the ratio of the inductor peak-to-peak ripple current to the average DC inductor current at the full-load current. The best trade-off between inductor size and circuit efficiency for step-up regulators generally has an LIR between 0.3 and 0.5. However, depending on the AC characteristics of the inductor core material and ratio of inductor resistance to other power-path resistances, the best LIR can shift up or down. If the inductor resistance is relatively high, more ripple can be accepted to reduce the number of turns required and increase the wire diameter. If the inductor resistance is relatively low, increasing inductance to lower the peak current can decrease losses throughout the power path. If extremely thin high-resistance inductors are used, as is common for LCD panel applications, the best LIR can increase to between 0.5 and 1.0.

Once a physical inductor is chosen, higher and lower values of the inductor should be evaluated for efficiency improvements in typical operating regions.

In Figure 1's typical operating circuit, the LCD's gate-on and gate-off voltages are generated from two charge pumps powered by the step-up regulator. The additional load on V_{MAIN} must therefore be considered in the inductance calculation. The effective maximum output current $I_{MAIN(EFF)}$ becomes the sum of the maximum load current on the step-up regulator's output

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plus the contributions from the positive and negative charge pumps:

$$I_{MAIN(EFF)} = I_{MAIN(MAX)} + n_{NEG} \times I_{NEG} + 3 \times I_{POS}$$

where $I_{MAIN(MAX)}$ is the maximum output current, n_{NEG} is the number of negative charge-pump stages, I_{NEG} is the negative charge-pump output current, and I_{POS} is the positive charge-pump output current.

Calculate the approximate inductor value using the typical input voltage (V_{IN}), the maximum output current ($I_{MAIN(MAX)}$), the expected efficiency (η_{TYP}) taken from an appropriate curve in the *Typical Operating Characteristics*, and an estimate of LIR based on the above discussion:

$$L = \left(\frac{V_{IN}}{V_{MAIN}}\right)^2 \left(\frac{V_{MAIN} - V_{IN}}{I_{MAIN(EFF)} \times f_{OSC}}\right)\left(\frac{\eta_{TYP}}{LIR}\right)$$

Choose an available inductor value from an appropriate inductor family. Calculate the maximum DC input current at the minimum input voltage $V_{IN(MIN)}$ using conservation of energy and the expected efficiency at that operating point (η_{MIN}) taken from an appropriate curve in the *Typical Operating Characteristics*:

$$I_{IN(DC,MAX)} = \frac{I_{MAIN(EFF)} \times V_{MAIN}}{V_{IN(MIN)} \times \eta_{MIN}}$$

Calculate the ripple current at that operating point and the peak current required for the inductor:

$$I_{RIPPLE} = \frac{V_{IN(MIN)} \times \left(V_{MAIN} - V_{IN(MIN)}\right)}{L \times V_{MAIN} \times f_{OSC}}$$

$$I_{PEAK} = I_{IN(DC,MAX)} + \frac{I_{RIPPLE}}{2}$$

The inductor's saturation current rating and the MAX8753's LX current limit ($I_{LX(MAX)}$) should exceed I_{PEAK} and the inductor's DC current rating should exceed $I_{IN(DC,MAX)}$. For good efficiency, choose an inductor with less than 0.1Ω series resistance.

Considering the typical operating circuit, the maximum load current ($I_{MAIN(MAX)}$) is 140mA with a 9V output and a typical input voltage of 3.3V:

$$I_{MAIN(EFF)} = 140mA + 2 \times 10mA + 3 \times 10mA = 190mA$$

Choosing an LIR of 0.45 and estimating efficiency of 80% at this operating point:

$$L = \left(\frac{3.3V}{9V}\right)^2 \left(\frac{9V - 3.3V}{0.19A \times 1MHz}\right)\left(\frac{0.80}{0.45}\right) \approx 6.8\mu H$$

Using the circuit's minimum input voltage (2.6V) and estimating efficiency of 70% at that operating point:

$$I_{IN(DC,MAX)} = \frac{0.19A \times 9V}{2.6V \times 0.7} \approx 0.94A$$

The ripple current and the peak current are:

$$I_{RIPPLE} = \frac{2.6V \times (9V - 2.6V)}{6.8\mu H \times 9V \times 1MHz} = 0.27A$$

$$I_{PEAK} = 0.94A + \frac{0.27A}{2} = 1.08A$$

Output Capacitor Selection

The total output-voltage ripple has two components: the capacitive ripple caused by the charging and discharging of the output capacitance, and the ohmic ripple due to the capacitor's equivalent series resistance (ESR):

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)}$$

$$V_{RIPPLE(C)} \approx \frac{I_{MAIN}}{C_{OUT}}\left(\frac{V_{MAIN} - V_{IN}}{V_{MAIN} f_{OSC}}\right) \text{and}$$

$$V_{RIPPLE(ESR)} \approx I_{PEAK} R_{ESR(COUT)}$$

where I_{PEAK} is the peak inductor current (see the *Inductor Selection* section). For ceramic capacitors, the output voltage ripple is typically dominated by $V_{RIPPLE(C)}$. The voltage rating and temperature characteristics of the output capacitor must also be considered.

Input Capacitor Selection

The input capacitor (C_{IN}) (see Figure 1) reduces the current peaks drawn from the input supply and reduces noise injection into the IC. A 10µF ceramic capacitor is used in the typical operating circuit (Figure 1) because of the high source impedance seen in typical lab setups. Actual applications usually have much lower source impedance since the step-up regulator often runs directly from the output of another regulated supply. Typically, C_{IN} can be reduced below the values used in the typical operating circuit. Ensure a low noise supply at IN by using adequate C_{IN}.

Rectifier Diode

The MAX8753's high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. In general, a 2A Schottky diode complements the internal MOSFET well.

Output-Voltage Selection

The output voltage of the main step-up regulator can be adjusted by connecting a resistive voltage-divider from the output (V_{MAIN}) to GND with the center tap connected to FB (see Figure 1). Select R2 in the 10kΩ to 50kΩ range. Calculate R1 with the following equation:

$$R1 = R2 \times \left(\frac{V_{MAIN}}{V_{FB}} - 1 \right)$$

where V_{FB}, the step-up regulator's feedback set point, is 1.245V. Place R1 and R2 close to the IC.

Loop Compensation

For stability, add a pole-zero pair from FB to GND in the form of a series resistor (R_{COMP}) and capacitor (C_{COMP}). R_{COMP} should be approximately half the value of the R2 feedback resistor. To further optimize transient response, vary R_{COMP} in 20% steps and C_{COMP} in 50% steps while observing transient response waveforms.

Charge-Pump Regulators

Output Voltage Selection

Adjust the positive charge-pump regulator output voltage by connecting a resistive voltage-divider from the regulator output V_{POS} to GND with the center tap connected to FBP (Figure 1). Select the lower resistor of the divider R6 in the 10kΩ to 50kΩ range. Calculate upper resistor R5 with the following equation:

$$R5 = R6 \times \left(\frac{V_{POS}}{V_{FBP}} - 1 \right)$$

where V_{FBP} = 1.25V (typ) is the regulation point of the positive charge-pump regulator.

Adjust the negative charge-pump regulator output voltage by connecting a resistive voltage-divider from the negative charge-pump output V_{NEG} to REF with the center tap connected to FBN (Figure 1). Select R4 in the 20kΩ to 100kΩ range. Calculate R3 with the following equation:

$$R3 = R4 \times \frac{V_{FBN} - V_{NEG}}{V_{REF} - V_{FBN}}$$

where V_{REF} = 1.25V, and V_{FBN} = 250mV is the regulation point of the negative charge-pump regulator.

Flying Capacitor

Increasing the flying capacitor (C_X) value lowers the effective source impedance and increases the output-current capability of the charge pump. Increasing the capacitance indefinitely has a negligible effect on output-current capability because the internal switch resistance and the diode impedance place a lower limit on the source impedance. A 0.1µF ceramic capacitor works well in most low-current applications. The flying capacitor's voltage rating must exceed the following:

$$V_{C1} > V_{SUPP}$$
$$V_{C2} > 2V_{SUPP}$$
$$V_{C3} > V_{SUPN}$$
$$V_{C4} > 2V_{SUPN}, \text{ if used}$$

Charge-Pump Input Capacitor

Use an input capacitor on SUPP and SUPN with a value equal to or greater than the flying capacitors on that charge pump. Place the capacitors as close to SUPP and SUPN as possible. Connect the capacitors directly to PGND.

Charge-Pump Output Capacitor

Increasing the output capacitance or decreasing the ESR reduces the output ripple voltage and the peak-to-peak transient voltage. With ceramic capacitors, the output-voltage ripple is dominated by the capacitance value. Use the following equation to approximate the required capacitor value:

$$C_{OUT\_CP} \geq \frac{I_{LOAD\_CP}}{2f_{OSC}V_{RIPPLE\_CP}}$$

where C_{OUT_CP} is the output capacitor of the charge pump, I_{LOAD_CP} is the load current of the charge pump, and V_{RIPPLE_CP} is the desired peak-to-peak value of the output ripple.

Charge-Pump Rectifier Diode

Use low-cost silicon switching diodes for D2 and D3 with a current rating equal to or greater than two times the average charge-pump input current. If it helps avoid an extra stage, some or all of the diodes can be replaced with Schottky diodes with an equivalent current rating.

TFT LCD DC-DC Converter with Integrated Charge Pumps

Applications Information

Power Dissipation

An IC's maximum power dissipation depends on the thermal resistance from the die to the ambient environment and the ambient temperature. The thermal resistance depends on the IC package, PC board copper area, other thermal mass, and airflow.

The MAX8753, with its exposed backside paddle soldered to 1in^2 of PC board copper, can dissipate about 1.7W into +70°C still air. More PC board copper, cooler ambient air, and more airflow increase the possible dissipation while less copper or warmer air decreases the IC's dissipation capability. The major components of power dissipation are the power dissipated in the step-up regulator, the linear regulator, and the charge pumps.

Step-Up Regulator

The largest portions of power dissipation in the step-up regulator are the internal MOSFET, inductor, and the output diode. If the step-up regulator has 90% efficiency, approximately 3% to 5% of the power is lost in the internal MOSFET, approximately 3% to 4% in the inductor, and approximately 1% in the output diode. The remaining 1% to 3% is distributed among the input and output capacitors and the PC board traces. If the input power is approximately 5W, the power lost in the internal MOSFET is approximately 150mW to 250mW.

Linear Regulator

The power dissipation in the linear regulator is:

$$P_{D(LOGIC)} = (V_{IN} - V_{LOGIC}) \times I_{LOGIC}$$

Positive Charge-Pump Regulator

The power dissipation in the positive charge-pump regulator is:

$$P_{D(POS)} = (3 \times V_{MAIN} - V_{POS}) \times I_{POS}$$

Negative Charge-Pump Regulator

The power dissipation in the negative charge-pump regulator is:

$$P_{D(NEG)} = (n_{NEG} \times V_{SUPN} + V_{NEG}) \times I_{NEG}$$

PC Board Layout and Grounding

Careful PC board layout is important for proper operation. Use the following guidelines for good PC board layout:

1) Minimize the area of the step-up regulator's high-current loops by placing the inductor (L1), output diode (D1), and output capacitor (C_{MAIN}) near the input capacitor (C_{IN}) and near the LX and PGND pins. The high-current input loop goes from the positive terminal of C_{IN} to L_1, to the IC's LX pin, out of PGND, and to C_{IN}'s negative terminal. The high-current output loop is from the positive terminal of C_{IN} to L1, to the output diode (D1), to the positive terminal of C_{MAIN}, reconnecting between the output capacitor and input capacitor ground terminals. Connect these loop components with short, wide connections. Avoid using vias in the high-current paths. If vias are unavoidable, use many vias in parallel to reduce resistance and inductance.
2) Create a power-ground island (PGND) consisting of the input and output capacitor grounds, PGND pin, the charge-pump input capacitors, output capacitors, and diodes. Connect these together with short, wide traces or a small ground plane. Maximizing the width of the power-ground traces improves efficiency and reduces output-voltage ripple and noise spikes. Create an analog-ground plane (AGND) consisting of the GND pin, all the feedback-divider ground connections, the INTG and DEL capacitor ground connections, and the device's exposed backside pad. Connect the AGND and PGND islands by connecting the PGND pin directly to the exposed backside pad. Make no other connections between these separate ground planes.
3) Place the feedback voltage-divider resistors as close to the feedback pin as possible. The divider's center trace should be kept short. Placing the resistors far away causes the FB traces to become antennas that can pick up switching noise. Care should be taken to avoid running any feedback trace near LX or the switching nodes in the charge pumps.
4) Place the IN and OUTL bypass capacitors as close to the device as possible. The ground connections of the IN and OUTL bypass capacitors should be connected directly to the PGND plane near the PGND pin with a wide trace.

5) Minimize the length and maximize the width of the traces between the output capacitors and the load for best transient response.
6) Minimize the size of the LX node while keeping it wide and short. Keep the LX node away from the feedback node and analog ground. Use DC traces as shield if necessary.

Refer to the MAX8753 evaluation kit for an example of proper board layout.

Chip Information

TRANSISTOR COUNT: 6922

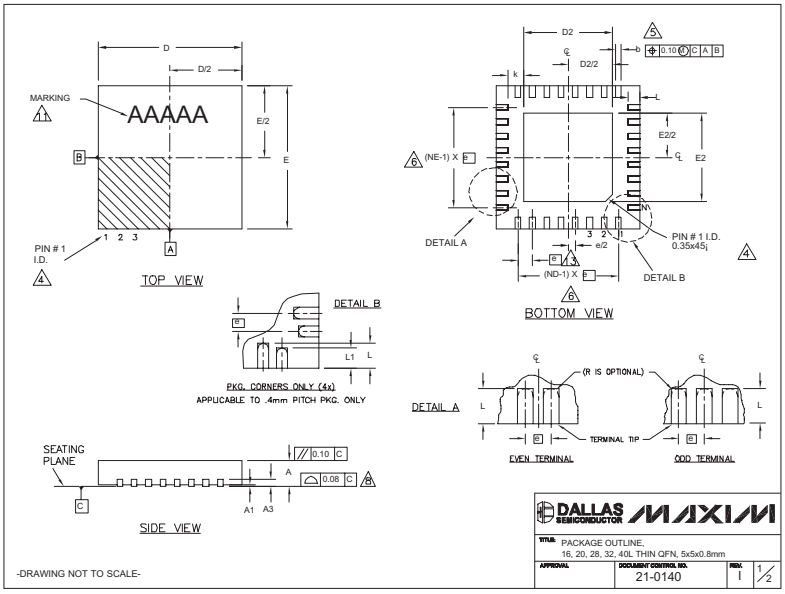
PROCESS: BiCMOS

TFT LCD DC-DC Converter with Integrated Charge Pumps

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QFN THIN.EPS



-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	I	1/2

COMMON DIMENSIONS

PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	0.35	0.45
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.40	0.50	0.60
L1	-	-	-	-	-	-	-	-	-	-	-	-	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			L	DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	-0.15	
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35	0.40	YES
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35	**	YES
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80	**	NO
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35	0.40	YES
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T4055-1	3.20	3.30	3.40	3.20	3.30	3.40	**	YES

**SEE COMMON DIMENSIONS TABLE

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3 AND T2855-6.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", –0.05.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm

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