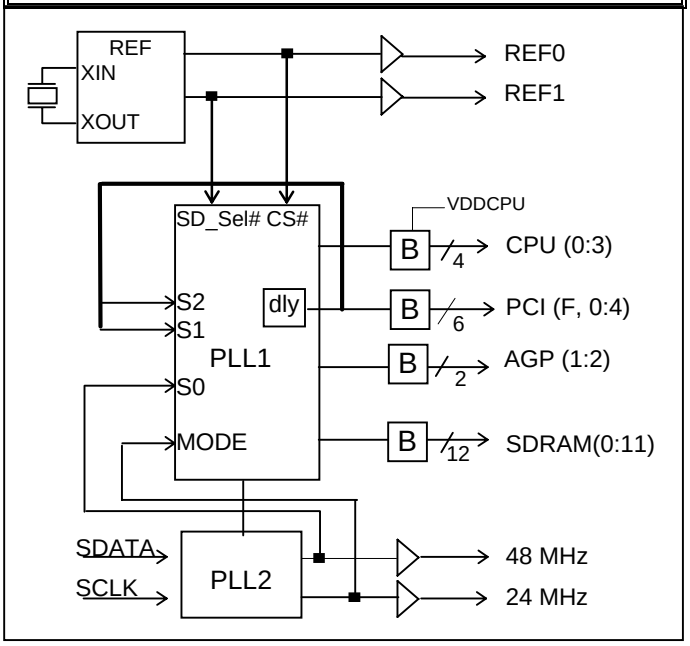
I²C Clock Generator for SiS5591/2, or VIA MVP3, 3 DIMM, Socket 7 Designs with AGP Support.

Approved Product

PRODUCT FEATURES

- Supports Pentium®, Pentium®II, M2,& K6 CPUs.
- Designed to support SiS5591/2 and MVP3 logic.
- 4 CPU & 2 (Sync./ Async.) AGP clocks
- Up to 12 SDRAM clocks for 3 DIMMs.
- 6 (Sync./ Async.) PCI clocks.
- Optional common or mixed supply mode:
  (VDD = VDDPCI = VDDCPU = 3.3V) or
  (VDD = VDDPCI = 3.3V, VDDCPU = 2.5V)
- < 250ps skew among CPU or SDRAM clocks.
- < 250ps skew among PCI clocks.
- I²C 2-Wire serial interface
- Programmable registers featuring:
  - Jumperless frequency selection
  - enable/disable each output pin
  - mode as tri-state, test, or normal
- Power Management Capability.
- 48 MHz for USB support
- Internal Crystal Load Capacitors.
- 48-pin SSOP package
- **Spread Spectrum Technology for EMI reduction**

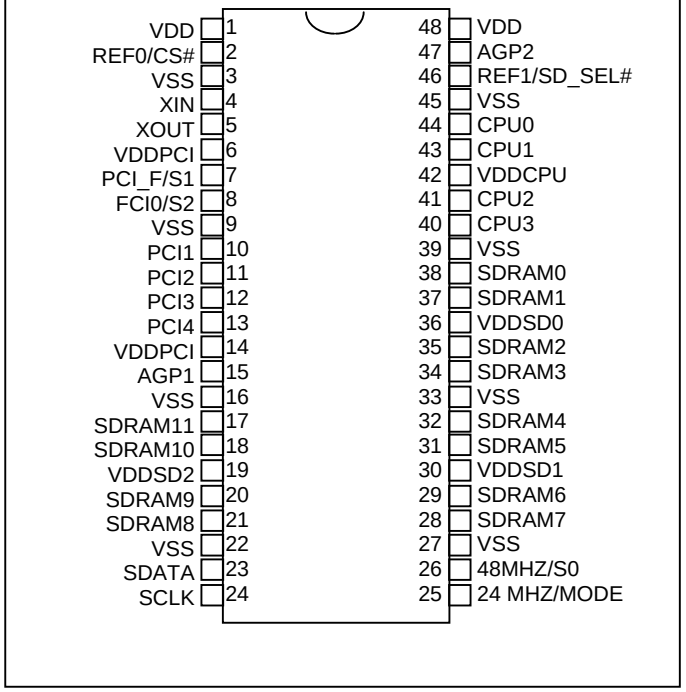
BLOCK DIAGRAM



FREQUENCY TABLE (MHz)

SD	S2	S1	S0	CPU	PCI	AGP	SDRAM
0	0	0	0	60	30	60	60
0	0	0	1	66.8	33.4	66.8	66.8
0	0	1	0	50	25	50	50
0	0	1	1	75	37.5	64	64
0	1	0	0	75	32	64	64
0	1	0	1	83.3	32	64	64
0	1	1	0	90	30	60	60
0	1	1	1	100	33.3	66.6	66.6
1	0	0	0	60	30	60	60
1	0	0	1	66.8	33.4	66.8	66.8
1	0	1	0	50	25	50	50
1	0	1	1	75	37.5	64	75
1	1	0	0	75	32	64	75
1	1	0	1	83.3	32	64	83.3
1	1	1	0	90	30	60	90
1	1	1	1	100	33.3	66.6	100

CONNECTION DIAGRAM



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PIN DESCRIPTION

Pin Number	Pin Name	PWR	I/O	TYPE	Description
4	**Xin**	VDD	I		These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal (Typ. 14.318 MHz). Xin may also serve as input for an externally generated reference signal. in which case Pin 5 is left unconnected
5	**Xout**	VDD	O		
7	**PCI_F**	VDDPCI	O		This is a bidirectional pin. During power up, this pin is an input for frequency selection S1 control bit (see page1, and app note on page 12) and sets the bit to its initial state. When the power reaches the rail (see fig.1, page 3), this pin becomes a low skew PCI clock output.
	S1	VDD	I		
8	**PCI0**	VDDPCI	O		This is a bidirectional pin. During power up, this pin is an input for frequency selection S2 control bit (see page1, and app note on page 12) and sets the bit to its initial state. When the power reaches the rail(see fig.1, page 3), this pin becomes a low skew PCI clock output.
	S2	VDD	I		
10, 11, 12, 13	**PCI (1:4)**	VDDPCI	O		Low skew PCI output clocks. Powered by VDDPCI
15, 47	**AGP(1:2)**	VDD	O		Accelerated Graphics Port output clocks. See frequency table page1.
44, 43, 41, 40	**CPU(0:3)**	VDDCPU	O		Low skew (<250 pS) clock outputs for host frequencies such as CPU, AGP, Chipset, Cache. Powered by VDDCPU.
38, 37, 35,34, 32, 31, 29, 28, 21, 20, 18, 17	**SDRAM(0:11)**	VDDSD(0:2)	O		Synchronous DRAM DIM clocks. They are powered by VDDSD0 thru VDDSD2. See VDDSD power pin description.
2	**REF0**	VDD	O		IF MODE=1 this pin becomes a buffered reference of the crystal.
	CS#	VDD	I		If MODE=0 then this pin controls CPU clock outputs by enabling (set to a logic 1) or disabling (set to a logic 0).
46	**SD_Sel#**	VDD	I		This is a bidirectional pin. During power up, this pin is an input "SD_Sel" for selecting the SDRAM frequency (see page1, and app note on page 12). If SD_Sel# is high (default), the SDRAM frequency is same as CPU. If it is low, the SDRAM frequency is same as AGP. When the power reaches the rail, (see fig.1, page 3), This pin becomes a 14.318 MHz reference clock output.
	REF1	VDD	O		
26	**48 MHz**	VDDSD1	I/O		This is a bidirectional pin. During power up, this pin is an input for frequency selection S0 control bit (see page1, and app note on page 12) and sets the bit to its initial state. After a fixed period of time (see fig.1, page 3), this pin becomes a 48 MHz frequency clock.
	S0		I*		
25	**24 MHz**	VDDSD1	O		This is a bidirectional pin. During power up, this pin is an input that enables (0) or disables (1) the power management shared pin (2, (see app note on page 12) and sets the bit to its initial state). After a fixed period of time (see fig.1, page 3), this pin becomes a 24 MHz frequency clock.
	MODE	VDD	I		
23	**SDATA**	VDD	I		Serial Data for I²C 2-wire control interface. Has internal pull-up.
24	**SCLK**	VDD	I		Serial Clock of I²C 2-wire control interface. Has internal pull-up.
3, 9, 16, 22, 27, 33, 39, 45	**VSS**	-	P		Ground pins.
1,48	**VDD**	-	P		Power supply pins for analog circuit, core logic and reference clock buffers, and AGP clocks.
6, 14	**VDDPCI**	-	P		3.3 volt power for PCI clocks.
36, 30, 19	**VDDSD0,1,2**	-	P		3.3 volt power for SDRAM clocks.
42	**VDDCPU**	-	P		3.3 or 2.5 volt power for CPU clocks.

***NOTE:** Require external 10K ohm pull-up resistors or 10K ohm pull down resistors for programming.*

A bypass capacitor (0.1µF) should be placed as close as possible to each power (Vdd) pin. If these bypass capacitors are not close to the pins their high frequency filtering characteristic will be canceled by the lead inductances of the traces.

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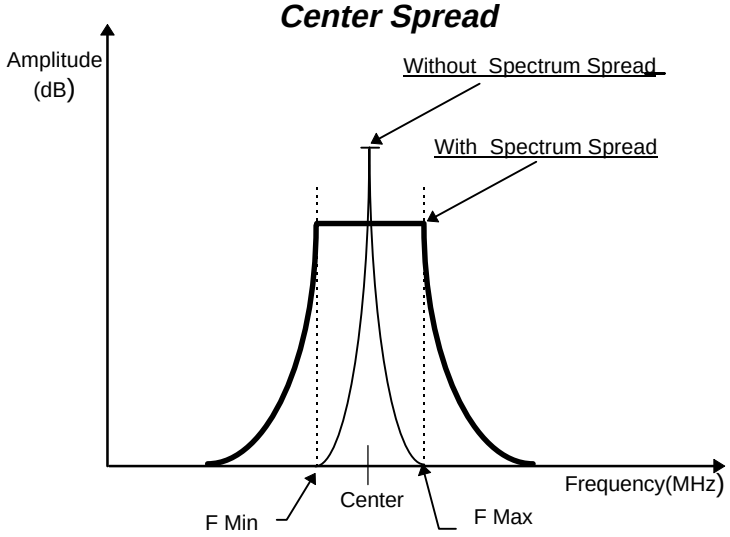
SPECTRUM SPREAD CLOCKING

Center Spread



Spectrum Analysis

SPECTRUM SPREADING SELECTION TABLE

Rested Frequency in MHz desired (actual)	Center Spreading							
	SSW=1				SSW=0			
	F Min	F Center	F Max	Spread	F Min	F Center	F Max	Spread
50 (50.11)	49.62	49.97	50.32	+/- 0.70%	49.28	49.97	50.66	+/- 1.38%
60 (60.00)	59.75	60.10	60.45	+/- 0.58%	59.41	60.10	60.79	+/- 1.15%
66.6 (66.82)	66.39	66.74	67.09	+/- 0.52%	66.05	66.74	67.43	+/- 1.04%
75 (75.00)	74.78	75.13	75.48	+/- 0.47%	74.43	75.13	75.83	+/- 0.93%
83.3 (83.52)	83.16	83.51	83.86	+/- 0.42%	82.82	83.51	84.20	+/- 0.83%
100 (100.23)	99.59	99.94	100.29	+/- 0.35%	99.24	99.94	100.64	+/- 0.70%

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POWER UP BIDIRECTIONAL PIN TIMING

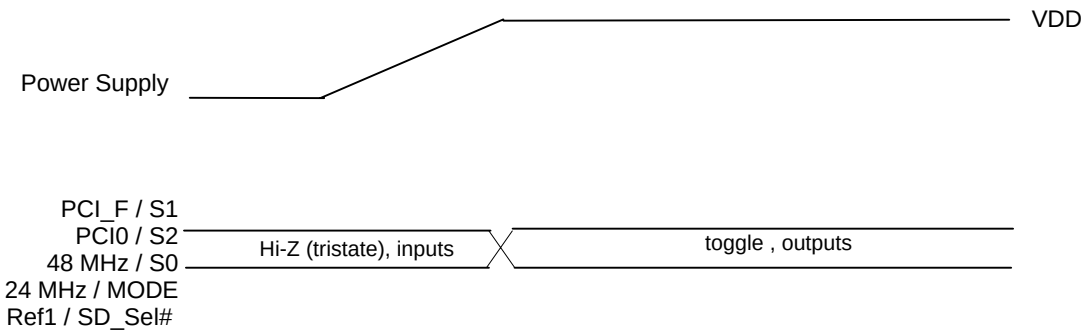

Fig.1

POWER MANAGEMENT FUNCTIONS

When MODE=0, pin 2 is an input CS# (CPU_STOP#), (when MODE=1, this functions are not available). A particular output is enabled only when both the serial interface and these pins indicate that it should be enabled. The IMISG745 CPU(0:3) clocks may be disabled according to the following table in order to reduce power consumption. All clocks are stopped in the low state. All clocks maintain a valid high period on transitions from running to stopped. The CPU clocks transition between running and stopped by waiting for one positive edge on PCICLK_F followed by a negative edge on the clock of interest, after which high levels of the output are either enabled or disabled.

CPU_STOP#	CPU	OTHER CLKs	XTAL & VCOs
0	LOW	RUNNING	RUNNING
1	RUNNING	RUNNING	RUNNING

Please note that all clocks can be asynchronously enabled or stopped via the 2-wire I²C control interface. In this case all clocks are stopped in the low state.

I²C Clock Generator for SiS5591/2, or VIA MVP3, 3 DIMM, Socket 7 Designs with AGP Support.
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2-WIRE I²C CONTROL INTERFACE

The 2-wire control interface implements a write only slave interface. The IMISG745 cannot be read back. Sub-addressing is not supported, thus all preceding bytes must be sent in order to change one of the control bytes. The 2-wire control interface allows each clock output to be individually enabled or disabled.

During normal data transfer, the SDATA signal only changes when the SCLK signal is low, and is stable when SCLK is high. There are two exceptions to this. A high to low transition on SDATA while SCLK is high is used to indicate the start of a data transfer cycle. A low to high transition on SDATA while SCLK is high indicates the end of a data transfer cycle. Data is always sent as complete 8-bit bytes, after which an acknowledge is generated. The first byte of a transfer cycle is a 7-bit address with a Read/Write bit as the LSB. Data is transferred MSB first.

The IMISG745 will respond to writes to 10 bytes (max) of data to address **D2** by generating the acknowledge (low) signal on the SDATA wire following reception of each byte. The IMISG745 will not respond to any other control interface conditions. Previously set control registers are retained.

SERIAL CONTROL REGISTERS

NOTE: The Pin# column lists the affected pin number where applicable. The @Pup column gives the state at true power up. Bytes are set to the values shown only on true power up, and not when the PWR_DWN# pin is activated.

Following the acknowledge of the Address Byte (D2), two additional bytes must be sent:
1) "**Command Code** " byte, and
2) "**Byte Count**" byte.
Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledged.

After the Command Code and the Count bytes have been acknowledged, the below described sequence (Byte 0, Byte 1, Byte 2, ...) will be valid and acknowledged.

Byte 0: Frequency, Function Select Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	*	SSW bit. Selects Spread Spectrum width. 0 = Wide; 1 = Narrow. See table on page 3
6	1	*	S2 (for frequency table selection by software via I2C)
5	1	*	S1 (for frequency table selection by software via I2C)
4	1	*	S0 (for frequency table selection by software via I2C)
3	0	*	enables freq. Selection by hardware (set to 0) or software I²C (set to 1)
2	1	*	Reserved
1 0	0 0		Bit 1 Bit 0 1 1 Tri-State 1 0 Normal (with Spread Spectrum On) mode 0 1 Test Mode 0 0 Normal (No Spread Spectrum) mode

I²C Clock Generator for SiS5591/2, or VIA MVP3, 3 DIMM, Socket 7 Designs with AGP Support.
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SERIAL CONTROL REGISTERS (Cont.)

Function Table

Function Description	Outputs				
	CPU	PCI	SDRAM	Ref	AGP
Tri-State	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Normal	see table	see table	CPU	14.318	14.318

Notes:
1. Tclk is a test clock over driven on the Xin input during test mode.

Byte 1: CPU, SIO, USB Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	26	48 MHz enable/Stopped
6	1	25	24 MHz enable/Stopped
5	1	-	0 = Reserved for IMI TEST. 1 = normal operation.
4	x	-	Reserved
3	1	40	CPUCLK3 enable/Stopped
2	1	41	CPUCLK2 enable/Stopped
1	1	43	CPUCLK1 enable/Stopped
0	1	44	CPUCLK0 enable/Stopped

Byte 2: PCI Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	1	7	PCI_F enable/Stopped
5	1	15	AGP1 enable/Stopped
4	1	13	PCI4 enable/Stopped
3	1	12	PCI3 enable/Stopped
2	1	11	PCI2 enable/Stopped
1	1	10	PCI1 enable/Stopped
0	1	8	PCI0 enable/Stopped

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SERIAL CONTROL REGISTERS (Cont.)

Byte 3: SDRAM Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	28,29,31,32	SDRAM(4:7) enable/Stopped
6	1	-	Reserved
5	1	-	Reserved
4	1	-	Reserved
3	1	34,35,37,38	SDRAM(0:3) enable/Stopped
2	1	-	Reserved
1	1	-	Reserved
0	1	-	Reserved

Byte 4: Additional SDRAM Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	x	-	Reserved
5	x	-	Reserved
4	x	-	Reserved
3	1	17,18,20,21	SDRAM(8:11) enable/Stopped
2	1	-	Reserved
1	1	-	Reserved
0	1	-	Reserved

Byte 5: Peripheral Control (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	x	-	Reserved
5	x	-	Reserved
4	1	47	AGP2 enable/Stopped
3	x	-	Reserved
2	x	-	Reserved
1	x	46	REF1 / SD_Sel# enable/Stopped
0	1	2	REF0 / CS# enable/Stopped

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MAXIMUM RATINGS

Voltage Relative to VSS:	-0.3V
Voltage Relative to VDD:	0.3V
Storage Temperature:	-65ºC to + 150ºC
Ambient Temperature:	0ºC to +70ºC
Maximum Power Supply:	7V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Type	Max	Units	Conditions
Input Low Voltage	VIL	-	-	0.8	Vdc	-
Input High Voltage	VIH	2.0	-	-	Vdc	-
Input Low Current	IIL			-66	µA	
Input High Current	IIH			5	µA	
Tri-State leakage Current	Ioz	-	-	10	µA	
Dynamic Supply Current	Idd	-	-	116	mA	CPU = 66.6 MHz, PCI = 33.3 MHz
Static Supply Current	Isdd	-	-	200	µA	-
Short Circuit Current	ISC	25	-	-	mA	1 output at a time - 30 seconds
VDD = VDDSD* = VDDPCI =3.3V ±5%, VDDCPU = 2.5 ± 5%, TA = 0ºC to +70ºC						

SWITCHING CHARACTERISTICS

Characteristic	Symbol	Min	Type	Max	Units	Conditions
Output Duty Cycle	-	45	50	55	%	Measured at 1.5V
CPU/SDRAM to PCI Offset	tOFF	1	-	4	ns	15 pf Load Measured at 1.5V
Skew (CPU-CPU), (CPU-AGP)*), (PCI-PCI), (SDRAM-SDRAM)	tSKEW1	-	-	250	ps	15 pf Load Measured at 1.5V
Skew (CPU-SDRAM)	tSKEW2	-	-	500	ps	15 pf Load Measured at 1.5V
ΔPeriod Adjacent Cycles	ΔP	-	-	±250	ps	-
Jitter Spectrum 20 dB Bandwidth from Center	BW_J			500	KHz	
VDD = VDDSD* = VDDPCI =3.3V ±5%, VDDCPU = 2.5 ± 5%, TA = 0ºC to +70ºC						

Note 1: Ring Back must not enter this range.
* In synchronous mode only.

TB4_V BUFFER CHARACTERISTICS FOR CPU (0:3)						
Characteristic	**Symbol**	**Min**	**Type**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	13	-	20	mA	Vout = VDD - .5V
Pull-Up Current Max	IOH_{max}	22	-	37	mA	Vout = 1.25V
Pull-Down Current Min	IOL_{min}	18	-	23	mA	Vout = 0.4V
Pull-Down Current Max	IOL_{max}	50	-	61	mA	Vout = 1.5V
Rise/Fall Time Min Between 0.4 V and 2.0 V	TRF_{min}	0.4	-	-	nS	10 pF Load
Rise/Fall Time Max Between 0.4 V and 2.0 V	TRF_{max}	-	-	2.0	nS	20 pF Load
VDD = VDDSD* = VDDPCI =3.3V ±5%, VDDCPU = 2.5 ± 5%, TA = 0ºC to +70ºC						

TB4 BUFFER CHARACTERISTICS FOR PCICLK(0:4,F), SDRAM(0:11), and REF0						
Characteristic	**Symbol**	**Min**	**Type**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	18	-	23	mA	Vout = VDD - .5V
Pull-Up Current Max	IOH_{max}	44	-	64	mA	Vout = 1.5V
Pull-Down Current Min	IOL_{min}	18	-	25	mA	Vout = 0.4V
Pull-Down Current Max	IOL_{max}	50	-	70	mA	Vout = 1.5V
Rise/Fall Time Min Between 0.4 V and 2.4 V	TRF_{min}	0.5	-	-	nS	15 pF Load
Rise/Fall Time Max Between 0.4 V and 2.4 V	TRF_{max}	-	-	2.0	nS	30 pF Load
VDD = VDDSD* = VDDPCI =3.3V ±5%, VDDCPU = 2.5 ± 5%, TA = 0ºC to +70ºC						

TB5 BUFFER CHARACTERISTICS FOR 24M, 48M and REF1						
Characteristic	**Symbol**	**Min**	**Type**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	13	-	17	mA	Vout = VDD - .5V
Pull-Up Current Max	IOH_{max}	30	-	40	mA	Vout = 1.5V
Pull-Down Current Min	IOL_{min}	13	-	19	mA	Vout = 0.4V
Pull-Down Current Max	IOL_{max}	32	-	44	mA	Vout = 1.5V
Rise/Fall Time Max Between 0.4 V and 2.4 V	TRF	-	-	2.0	nS	20 pF Load
VDD = VDDSD* = VDDPCI =3.3V ±5%, VDDCPU = 2.5 ± 5%, TA = 0ºC to +70ºC						

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CRYSTAL AND REFERENCE OSCILLATOR PARAMETERS						
Characteristic	**Symbol**	**Min**	**Type**	**Max**	**Units**	**Conditions**
Frequency	F_o	12.00	14.31818	16.00	MHz	
Tolerance	TC	-	-	+/-100	PPM	Calibration note 1
	TS	-	-	+/- 100	PPM	Stability (Ta -10 to +60C) note 1
	TA	-	-	5	PPM	Aging (first year @ 25C) note 1
Mode	OM	-	-	-		Parallel Resonant
Pin Capacitance	CP		36		pF	Capacitance of XIN and Xout pins to ground (each)
DC Bias Voltage	V_{BIAS}	0.3Vdd	Vdd/2	0.7Vdd	V	
Startup time	Ts	-	-	30	µS	
Load Capacitance	CL	-	20	-	pF	the crystals rated load. note 1
Effective Series resistance (ESR)	R1	-	-	40	Ohms	
Power Dissipation	DL	-	-	0.10	mW	note 1
Shunt Capacitance	CO	-	--	8	pF	crystals internal package capacitance (total)

For maximum accuracy, the total circuit loading capacitance should be equal to CL. This loading capacitance is the effective capacitance across the crystal pins and includes the device pin capacitance (CP) in parallel with any circuit traces, the clock generator and any onboard discrete load capacitors.
Budgeting Calculations
Typical trace capacitance, (< half inch) is 4 pF, Load to the crystal is therefore = 2.0 pF
Clock generator internal pin capacitance of 36 pF, Load to the crystal is therefore = 18.0 pF
the total parasitic capacitance would therefore be = 20.0 pF.

Note 1: It is recommended but not mandatory that a crystal meets these specifications.

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APPLICATION NOTE FOR SELECTION ON BIDIRECTIONAL PINS

Pins 7, 8, 25, 26 and 46 are Power up bidirectional pins and are used for selecting different functions in this device (see Pin description, Page 2). During power-up of the device, these pins are in input mode (see Fig1, page4), therefore, they are considered input select pins internal to the IC, these pins have a large value pull-up each (250KΩ), therefore, a selection "1" is the default. If the system uses a slow power supply (over 5ms settling time), then it is recommended to use an external Pullup (Rup) in order to insure a high selection. In this case, the designer may choose one of two configurations, see FIG.3A and Fig. 3B.

Fig. 3A represents an additional pull up resistor 50KΩ connected from the pin to the power line, which allows a faster pull to a high level.
If a selection "0" is desired, then a jumper is placed on JP1 to a 5KΩ resistor as implemented as shown in Fig. 3A. Please note the selection resistors (Rup, and Rdn) are placed before the Damping resistor (Rd) close to the pin.

Fig. 3B represents a single resistor 10KΩ connected to a 3 way jumper, JP2. When a "1" selection is desired, a jumper is placed between leads1 and 3. When a "0" selection is desired, a jumper is placed between leads 1 and 2.

If the system power supply is fast (less than 5ms settling time), then FIG3A only applies and Pull up Rup resistor is not necessary.

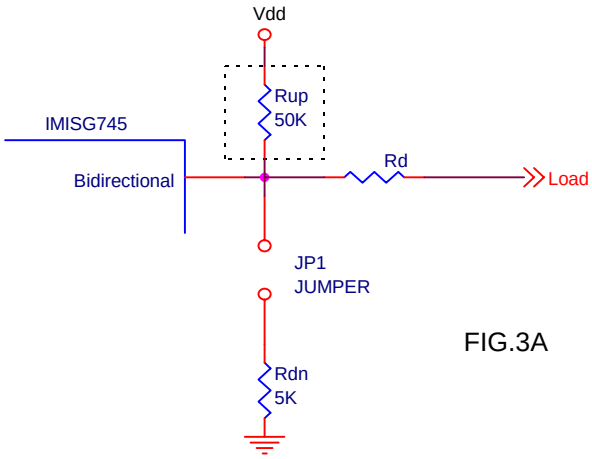

FIG.3A

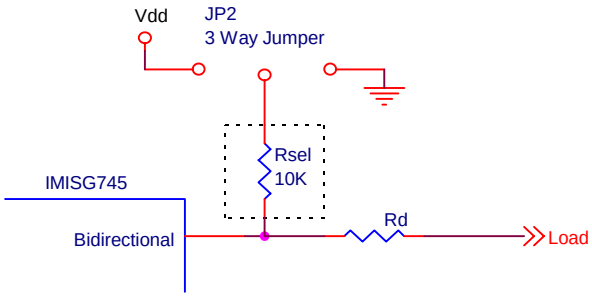

FIG.3B

I²C Clock Generator for SiS5591/2, or VIA MVP3, 3 DIMM, Socket 7 Designs with AGP Support.
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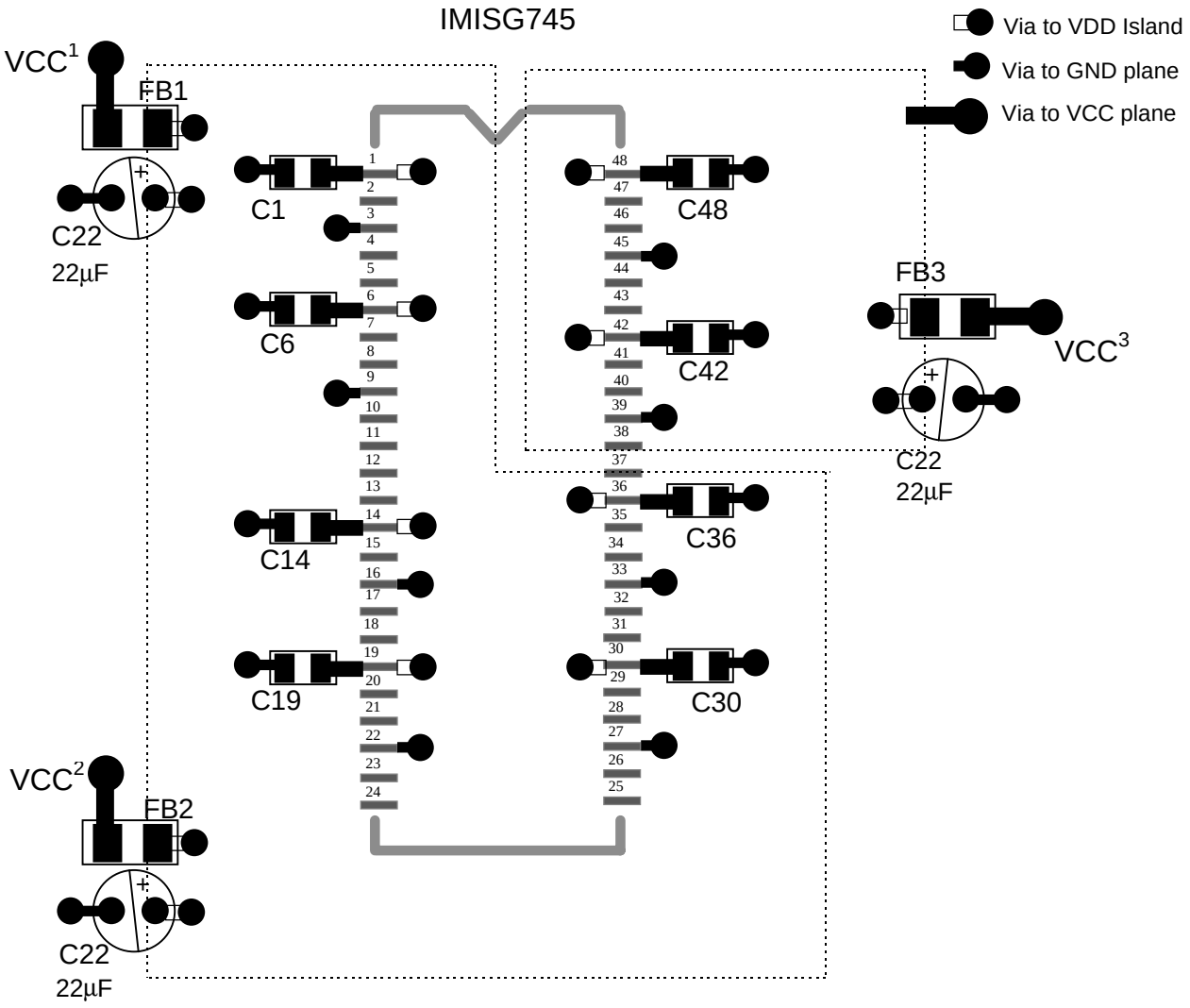
PCB LAYOUT SUGGESTION



This is only a layout recommendation for best performance and lower EMI. The designer may choose a different approach but C1, C6, C14, C19, C30, C36, C42, and C48 (all are 0.1µf) should always be used and placed as close as possible to their VDD pins.

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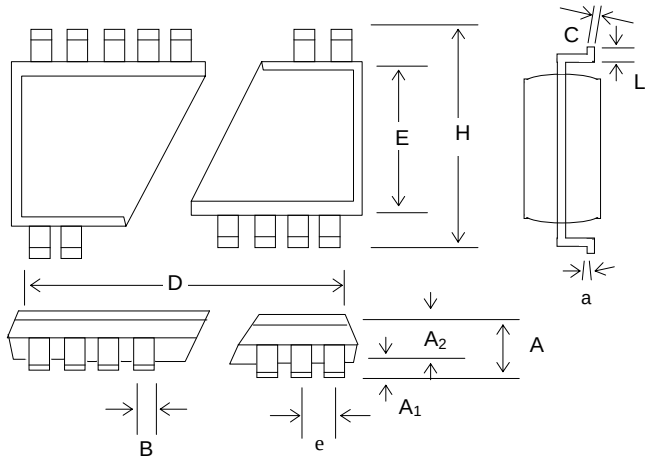
PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.095	0.102	0.110	2.41	2.59	2.79
A_1	0.008	0.012	0.016	0.20	0.31	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.0135	0.203	0.254	0.343
c	0.005	.008	0.010	0.127	0.20	0.254
D	0.620	0.625	0.637	15.75	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.0256 BSC			0.640 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.024	0.030	0.040	0.61	0.76	1.02
a	0º	4º	8º	0º	4º	8º

ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMISG745BYB	48 PIN SSOP	Commercial, 0ºC to +70ºC

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
SG745BYB
Date Code, Lot #

IMISG745BYB

Flow
B = Commercial, 0ºC to + 70ºC

Package
Y = SSOP

Revision

IMI Device Number