

**165-Bump BGA**  
**Commercial Temp**  
**Industrial Temp**

## 18Mb Burst of 2 SigmaQuad SRAM

**200 MHz–100 MHz**  
**2.5 V V<sub>DD</sub>**  
**1.8 V or 1.5 V I/O**

### Features

- Simultaneous Read and Write SigmaQuad™ Interface
- JEDEC-standard pinout and package
- Dual DoubleData Rate interface
- Byte Write controls sampled at data-in time
- Burst of 2 Read and Write
- 2.5 V +100/–100 mV core power supply
- 1.5 V or 1.8 V HSTL Interface
- Pipelined read operation
- Fully coherent read and write pipelines
- ZQ mode pin for programmable output drive strength
- IEEE 1149.1 JTAG-compliant Boundary Scan
- 165-bump, 13 mm x 15 mm, 1 mm bump pitch BGA package
- Pin-compatible with future 36Mb, 72Mb, and 144Mb devices
- RoHS-compliant 165-bump BGA package available

### SigmaRAM™ Family Overview

GS8180QV18 are built in compliance with the SigmaQuad SRAM pinout standard for Separate I/O synchronous SRAMs. They are 18,874,368-bit (18Mb) SRAMs. These are the first in a family of wide, very low voltage HSTL I/O SRAMs designed to operate at the speeds needed to implement economical high performance networking systems.

SigmaQuad SRAMs are offered in a number of configurations. Some emulate and enhance other synchronous separate I/O SRAMs. A higher performance SDR (Single Data Rate) Burst of 2 version is also offered. The logical differences between the protocols employed by these RAMs hinge mainly on

various combinations of address bursting, output data registering, and write cueing. Along with the Common I/O family of SigmaRAMs, the SigmaQuad family of SRAMs allows a user to implement the interface protocol best suited to the task at hand.

### Clocking and Addressing Schemes

A Burst of 2 SigmaQuad SRAM is a synchronous device. It employs two input register clock inputs, K and  $\bar{K}$ . K and  $\bar{K}$  are independent single-ended clock inputs, not differential inputs to a single differential clock input buffer. The device also allows the user to manipulate the output register clock inputs quasi independently with the C and  $\bar{C}$  clock inputs. C and  $\bar{C}$  are also independent single-ended clock inputs, not differential inputs. If the C clocks are tied high, the K clocks are routed internally to fire the output registers instead.

Because Separate I/O Burst of 2 RAMs always transfer data in two packets, A0 is internally set to 0 for the first read or write transfer, and automatically incremented by 1 for the next transfer. Because the LSB is tied off internally, the address field of a Burst of 2 RAM is always one address pin less than the advertised index depth (e.g., the 1M x 18 has a 512K addressable index).

### Parameter Synopsis\*

	<b>-200</b>	<b>-167</b>	<b>-133</b>	<b>-100</b>
t <sub>KHKH</sub>	5.0 ns	6.0 ns	7.5 ns	10.0 ns
t <sub>KHQV</sub>	2.3 ns	2.5 ns	3.0 ns	3.0 ns

## 1M x 18 SigmaQuad SRAM—Top View (Package D)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	MCL/SA (144Mb)	NC/SA (36Mb)	$\overline{W}$	$\overline{BW1}$	$\overline{K}$	NC	$\overline{R}$	SA	MCL/SA (72Mb)	NC
B	NC	Q9	D9	SA	NC	K	$\overline{BW0}$	SA	NC	NC	Q8
C	NC	NC	D10	V <sub>SS</sub>	SA	SA	SA	V <sub>SS</sub>	NC	Q7	D8
D	NC	D11	Q10	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	NC	NC	D7
E	NC	NC	Q11	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	D6	Q6
F	NC	Q12	D12	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	NC	Q5
G	NC	D13	Q13	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	NC	D5
H	NC	V <sub>REF</sub>	V <sub>DDQ</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	V <sub>DDQ</sub>	V <sub>REF</sub>	ZQ
J	NC	NC	D14	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	Q4	D4
K	NC	NC	Q14	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	D3	Q3
L	NC	Q15	D15	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	NC	Q2
M	NC	NC	D16	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	NC	Q1	D2
N	NC	D17	Q16	V <sub>SS</sub>	SA	SA	SA	V <sub>SS</sub>	NC	NC	D1
P	NC	NC	Q17	SA	SA	C	SA	SA	NC	D0	Q0
R	TDO	TCK	SA	SA	SA	$\overline{C}$	SA	SA	SA	TMS	TDI

 11 x 15 Bump BGA—13 x 15 mm<sup>2</sup> Body—1 mm Bump Pitch

**Notes:**

- Expansion addresses: A3 for 36Mb, A10 for 72Mb, A2 for 144Mb
- BW0 controls writes to D0:D8. BW1 controls writes to D9:D17.
- MCL = Must Connect Low
- It is recommended that H1 be tied low for compatibility with future devices.

## 512K x 36 SigmaQuad SRAM—Top View (Package D)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	MCL/SA (288Mb)	NC/SA (72Mb)	$\overline{W}$	$\overline{BW2}$	$\overline{K}$	$\overline{BW1}$	$\overline{R}$	NC/SA (36Mb)	MCL/SA (144Mb)	NC
B	Q27	Q18	D18	SA	$\overline{BW3}$	K	$\overline{BW0}$	SA	D17	Q17	Q8
C	D27	Q28	D19	V <sub>SS</sub>	SA	SA	SA	V <sub>SS</sub>	D16	Q7	D8
D	D28	D20	Q19	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	Q16	D15	D7
E	Q29	D29	Q20	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	Q15	D6	Q6
F	Q30	Q21	D21	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	D14	Q14	Q5
G	D30	D22	Q22	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	Q13	D13	D5
H	NC	V <sub>REF</sub>	V <sub>DDQ</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	V <sub>DDQ</sub>	V <sub>REF</sub>	ZQ
J	D31	Q31	D23	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	D12	Q4	D4
K	Q32	D32	Q23	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	Q12	D3	Q3
L	Q33	Q24	D24	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	D11	Q11	Q2
M	D33	Q34	D25	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	D10	Q1	D2
N	D34	D26	Q25	V <sub>SS</sub>	SA	SA	SA	V <sub>SS</sub>	Q10	D9	D1
P	Q35	D35	Q26	SA	SA	C	SA	SA	Q9	D0	Q0
R	TDO	TCK	SA	SA	SA	$\overline{C}$	SA	SA	SA	TMS	TDI

 11 x 15 Bump BGA—13 x 15 mm<sup>2</sup> Body—1 mm Bump Pitch

**Notes:**

- Expansion addresses: A9 for 36Mb, A3 for 72Mb, A10 for 144Mb, A2 for 288Mb
- $\overline{BW0}$  controls writes to D0:D8.  $\overline{BW1}$  controls writes to D9:D17.
- $\overline{BW2}$  controls writes to D18:D26.  $\overline{BW3}$  controls writes to D27:D35.
- MCL = Must Connect Low
- It is recommended that H1 be tied low for compatibility with future devices.

**Pin Description Table**

Symbol	Description	Type	Comments
SA	Synchronous Address Inputs	Input	—
NC	No Connect	—	—
$\bar{R}$	Synchronous Read	Input	Active Low
$\bar{W}$	Synchronous Write	Input	Active Low
$\overline{BW0-BW1}$	Synchronous Byte Writes	Input	Active Low
$\overline{BW2-BW3}$	Synchronous Byte Writes	Input	Active Low (x36 only)
K	Input Clock	Input	Active High
$\bar{K}$	Input Clock	Input	Active Low
C	Output Clock	Input	Active High
$\bar{C}$	Output Clock	Input	Active Low
TMS	Test Mode Select	Input	—
TDI	Test Data Input	Input	—
TCK	Test Clock Input	Input	—
TDO	Test Data Output	Output	—
V <sub>REF</sub>	HSTL Input Reference Voltage	Input	—
ZQ	Output Impedance Matching Input	Input	—
MCL	Must Connect Low	—	—
D0–D17	Synchronous Data Inputs	Input	
D18–D35	Synchronous Data Inputs	Input	
Q0–Q17	Synchronous Data Outputs	Output	
Q18–Q35	Synchronous Data Outputs	Output	
V <sub>DD</sub>	Power Supply	Supply	2.5 V Nominal
V <sub>DDQ</sub>	Isolated Output Buffer Supply	Supply	1.8 or 1.5 V Nominal
V <sub>SS</sub>	Power Supply: Ground	Supply	—

**Note:**

NC = Not Connected to die or any other pin

**Background**

Separate I/O SRAMs, from a system architecture point of view, are attractive in applications where alternating reads and writes are needed. Therefore, the SigmaQuad SRAM interface and truth table are optimized for alternating reads and writes. Separate I/O SRAMs are unpopular in applications where multiple reads or multiple writes are needed because burst read or write transfers from Separate I/O SRAMs can cut the RAM's bandwidth in half.

A SigmaQuad SRAM can begin an alternating sequence of reads and writes with either a read or a write. In order for any separate I/O SRAM that shares a common address between its two ports to keep both ports running all the time, the RAM must implement some sort of burst transfer protocol. The burst must be at least long enough to cover the time the opposite port is receiving

instructions on what to do next. The rate at which a RAM can accept a new random address is the most fundamental performance metric for the RAM. Each of the three SigmaQuad SRAMs support similar address rates because random address rate is determined by the internal performance of the RAM and they are all based on the same internal circuits. Differences between the truth tables of the different SigmaQuad SRAMs, or any other Separate I/O SRAMs, follow from differences in how the RAM's interface is contrived to interact with the rest of the system. Each mode of operation has its own advantages and disadvantages. The user should consider the nature of the work to be done by the RAM to evaluate which version is best suited to the application at hand.

### Alternating Read-Write Operations

SigmaQuad SRAMs follow a few simple rules of operation.

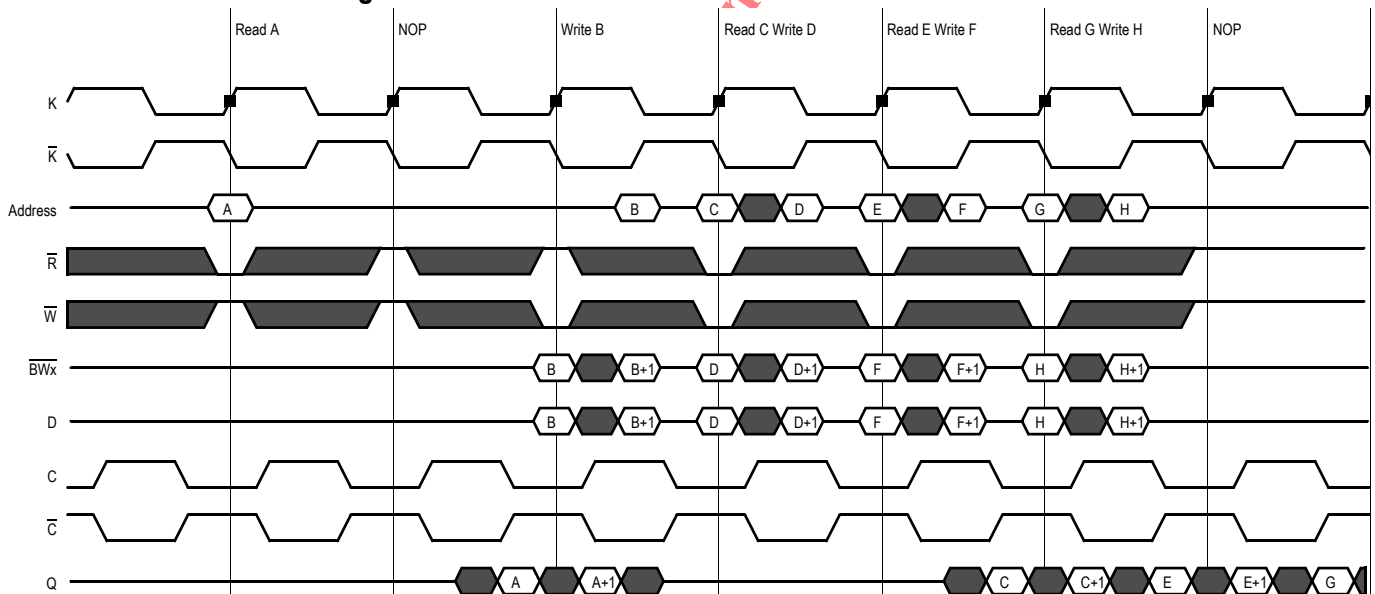
- Read or Write commands issued on one port are never allowed to interrupt an operation in progress on the other port.
- Read or Write data transfers in progress may not be interrupted and re-started.
- $\bar{R}$  and  $\bar{W}$  high always deselected the RAM.
- All address, data, and control inputs are sampled on clock edges.

In order to enforce these rules, each RAM combines present state information with command inputs. See the Truth Table for details.

### Burst of 2 SigmaQuad SRAM DDR Read

The read port samples the status of the Address Input and  $\bar{R}$  pins at each rising edge of K. A low on the Read Enable-bar pin,  $\bar{R}$ , begins a read cycle. Data can be clocked out one cycle later and again one half cycle after that. A high on the Read Enable-bar pin,  $\bar{R}$ , begins a read port deselect cycle.

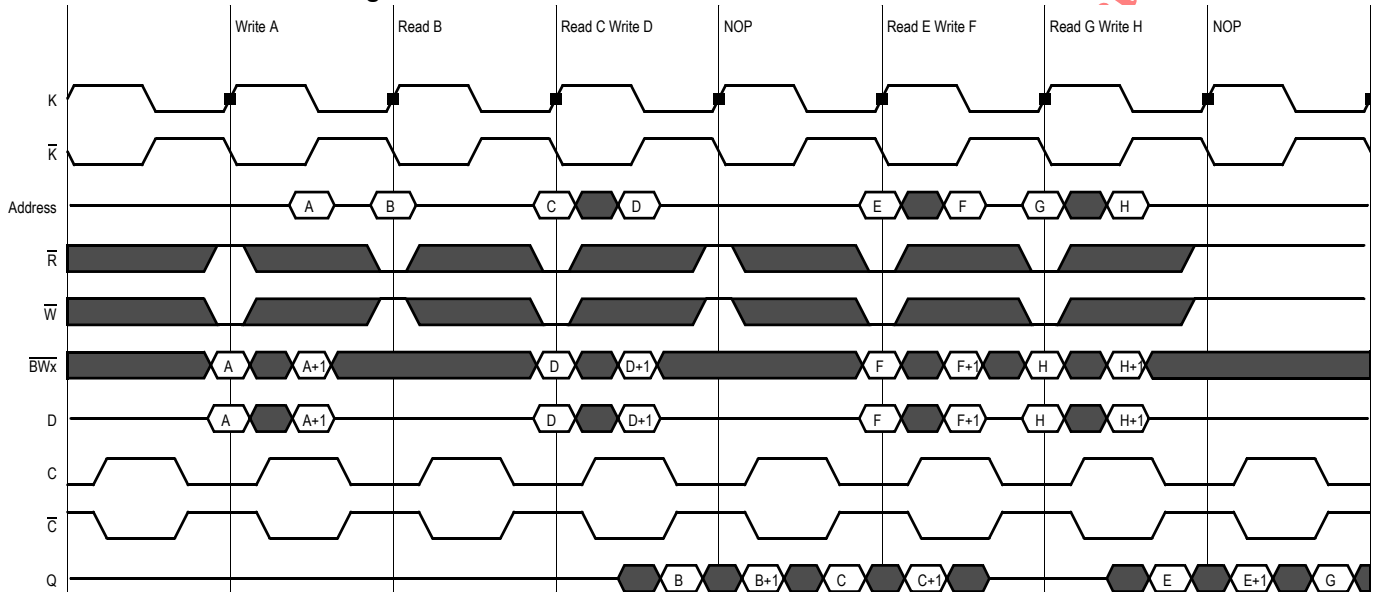
### Burst of 2 Double Data Rate SigmaQuad SRAM Read First



**Burst of 2 SigmaQuad SRAM DDR Write**

The write port samples the status of the  $\overline{W}$  pin at each rising edge of K and the Address Input pins on the following rising edge of  $\overline{K}$ . A low on the Write Enable-bar pin,  $\overline{W}$ , begins a write cycle. The first of the data-in pairs associated with the write command is clocked in with the same rising edge of K used to capture the write command. The second of the two data in transfers is captured on the rising edge of  $\overline{K}$  along with the write address. A high on  $\overline{W}$  causes a write port deselection cycle.

**Burst of 2 Double Data Rate SigmaQuad SRAM Write First**



**Special Functions**

**Byte Write Control**

Byte Write Enable pins are sampled at the same time that Data In is sampled. A high on the Byte Write Enable pin associated with a particular byte (e.g.,  $\overline{BW0}$  controls D0–D8 inputs) will inhibit the storage of that particular byte, leaving whatever data may be stored at the current address at that byte location undisturbed. Any or all of the Byte Write Enable pins may be driven high or low during the data in sample times in a write sequence.

Each write enable command and write address loaded into the RAM provides the base address for a 2 beat data transfer. The x18 version of the RAM, for example, may write 36 bits in association with each address loaded. Any 9-bit byte may be masked in any write sequence.

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**Example x18 RAM Write Sequence using Byte Write Enables**

Data In Sample Time	$\overline{BW0}$	$\overline{BW1}$	D0–D8	D9–D17
Beat 1	0	1	Data In	Don't Care
Beat 2	1	0	Don't Care	Data In

**Resulting Write Operation**

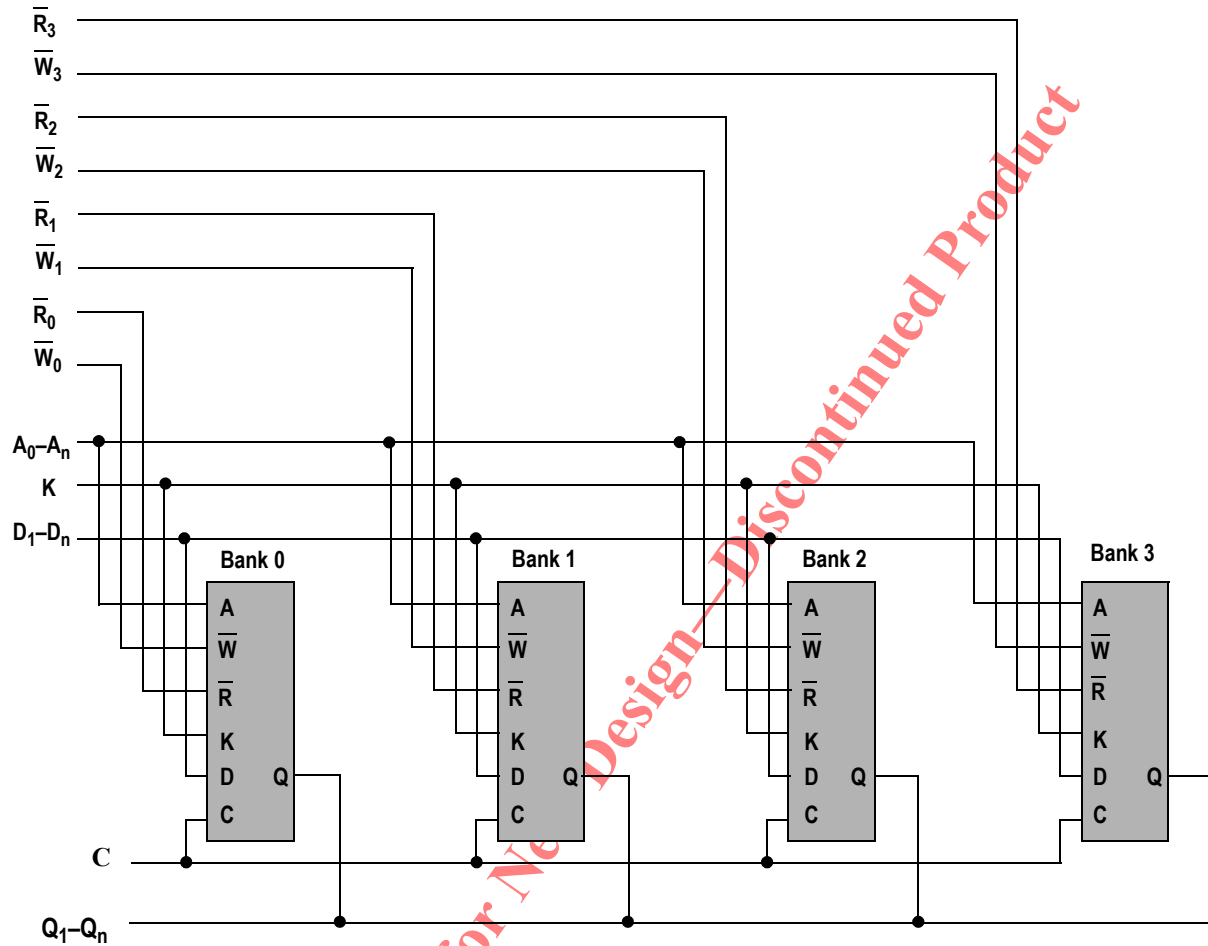
Beat 1 D0–D8	Beat 1 D9–D17	Beat 2 D0–D8	Beat 2 D9–D17
Written	Unchanged	Unchanged	Written

**Output Register Control**

SigmaQuad SRAMs offer two mechanisms for controlling the output data registers. Typically, control is handled by the Output Register Clock inputs, C and  $\overline{C}$ . The Output Register Clock inputs can be used to make small phase adjustments in the firing of the output registers by allowing the user to delay driving data out as much as a few nanoseconds beyond the next rising edges of the K and  $\overline{K}$  clocks. If the C and  $\overline{C}$  clock inputs are tied high, the RAM reverts to K and  $\overline{K}$  control of the outputs, allowing the RAM to function as a conventional pipelined read SRAM.

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Example Four Bank Depth Expansion Schematic

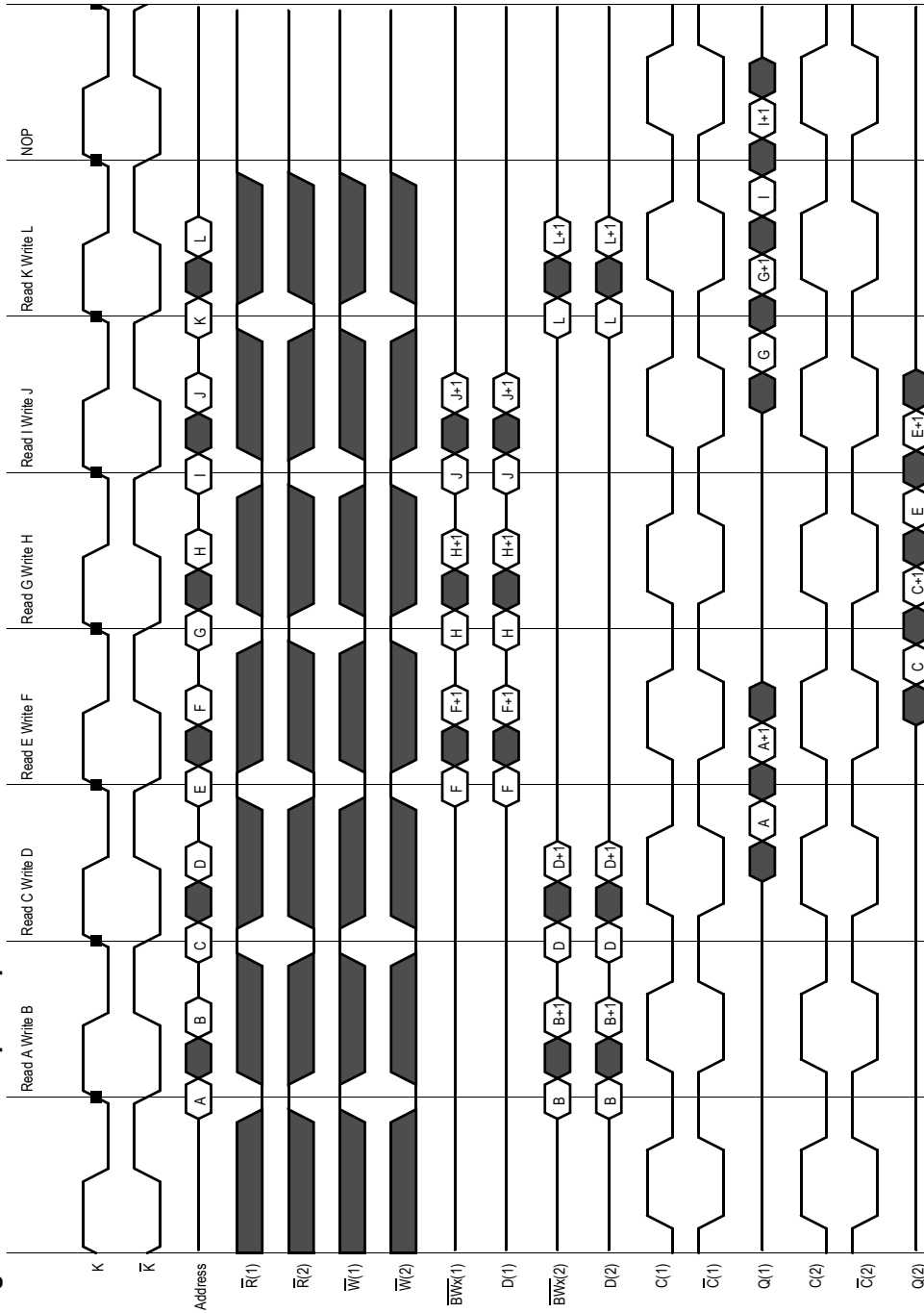


Note: For simplicity  $\overline{B}W_n$ ,  $\overline{K}$ , and  $\overline{C}$  are not shown.

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**Burst of 2 SigmaQuad SRAM Depth Expansion**



*Product*

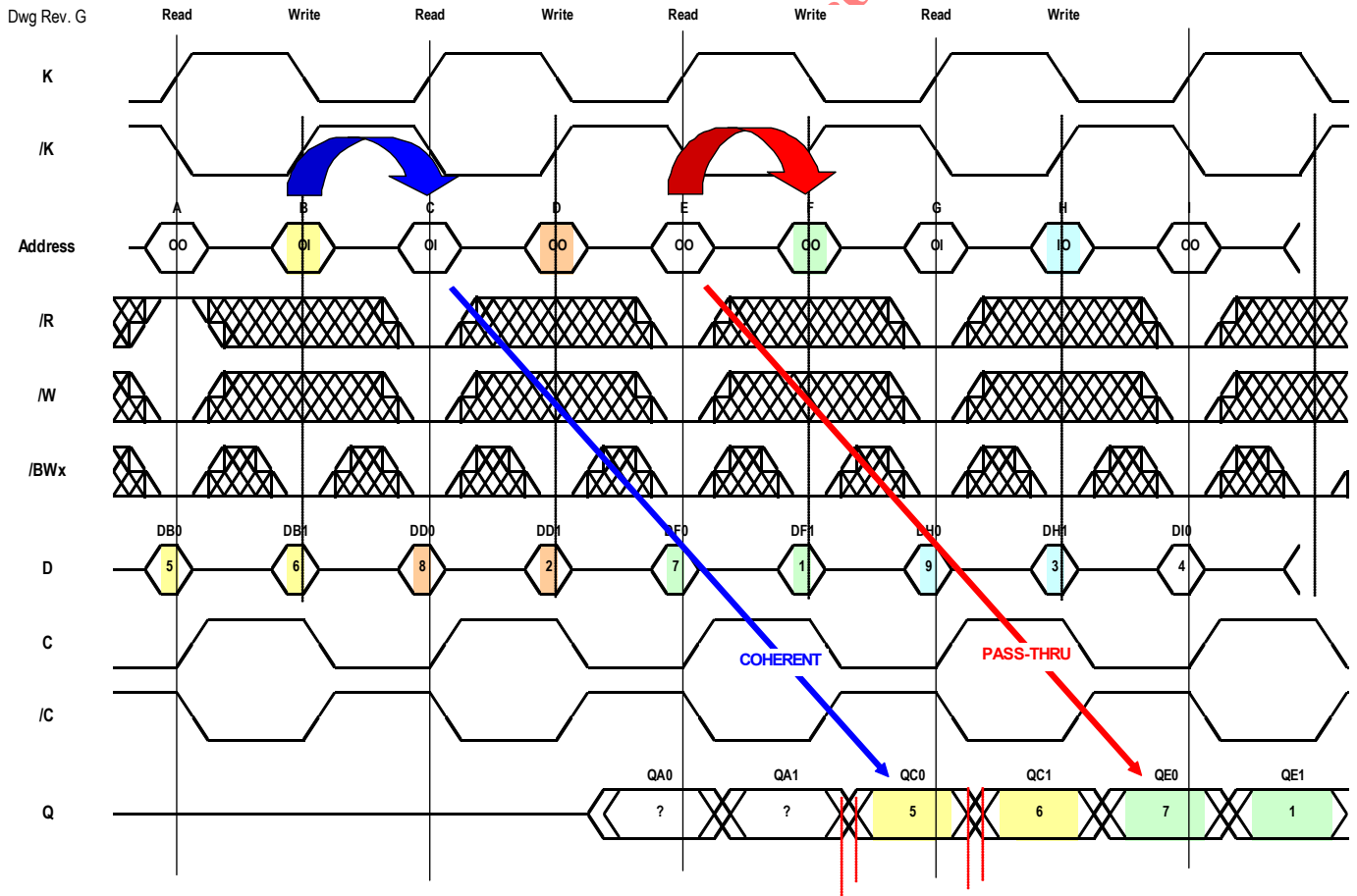
**FLXDrive-II Output Driver Impedance Control**

HSTL I/O SigmaQuad SRAMs are supplied with programmable impedance output drivers. The ZQ pin must be connected to  $V_{SS}$  via an external resistor,  $R_Q$ , to allow the SRAM to monitor and adjust its output driver impedance. The value of  $R_Q$  must be 5X the value of the intended line impedance driven by the SRAM. The allowable range of  $R_Q$  to guarantee impedance matching with a vendor-specified tolerance is between  $150\Omega$  and  $300\Omega$ . Periodic readjustment of the output driver impedance is necessary as the impedance is affected by drifts in supply voltage and temperature. A clock cycle counter periodically triggers an impedance evaluation, resets and counts again. Each impedance evaluation may move the output driver impedance level one step at a time towards the optimum level. The output driver is implemented with discrete binary weighted impedance steps. The SRAM requires 32K start-up cycles, selected or deselected, after  $V_{DD}$  reaches its operating range to reach its programmed output driver impedance.

**Burst of 2 Coherency and Pass Through Functions**

Because the Burst of 2 read and write commands are loaded at the same time, there may be some confusion over what constitutes “coherent” operation. Normally, one would expect a RAM to produce the just-written data when it is read immediately after a write. This is true of the Burst of 2 except in one case, as is illustrated in the following diagram. If the user holds the same address value in a given K clock cycle, loading the same address as a read address and then as a matching write address, the Burst of 2 will read or “Pass-thru” the latest data input, rather than the data from the previously completed write operation.

**Burst of 2 Coherency and Pass Through Functions**



**Separate I/O Burst of 2 SigmaQuad SRAM Read Truth Table**

A	$\bar{R}$	Output Next State	Q	Q
$K \uparrow$ ( $t_n$ )	$K \uparrow$ ( $t_n$ )	$K \uparrow$ ( $t_n$ )	$K \uparrow$ ( $t_{n+1}$ )	$\bar{K} \uparrow$ ( $t_{n+1/2}$ )
X	1	Deselect	Hi-Z	Hi-Z
V	0	Read	Q0	Q1

**Notes:**

1. X = Don't Care, 1 = High, 0 = Low, V = Valid.
2.  $\bar{R}$  is evaluated on the rising edge of K.
3. Q0 and Q1 are the first and second data output transfers in a read.

**Separate I/O Burst of 2 SigmaQuad SRAM Write Truth Table**

A	$\bar{W}$	$\overline{BWn}$	$\overline{BWn}$	Input Next State	D	D
$\bar{K} \uparrow$ ( $t_n + 1/2$ )	$K \uparrow$ ( $t_n$ )	$K \uparrow$ ( $t_n$ )	$\bar{K} \uparrow$ ( $t_n + 1/2$ )	$K \uparrow$ , $\bar{K} \uparrow$ ( $t_n$ ), ( $t_n + 1/2$ )	$K \uparrow$ ( $t_n$ )	$\bar{K} \uparrow$ ( $t_n + 1/2$ )
V	0	0	0	Write Byte Dx0, Write Byte Dx1	D0	D1
V	0	0	1	Write Byte Dx0, Write Abort Byte Dx1	D0	X
V	0	1	0	Write Abort Byte Dx0, Write Byte Dx1	X	D1
X	0	1	1	Write Abort Byte Dx0, Write Abort Byte Dx1	X	X
X	1	X	X	Deselect	X	X

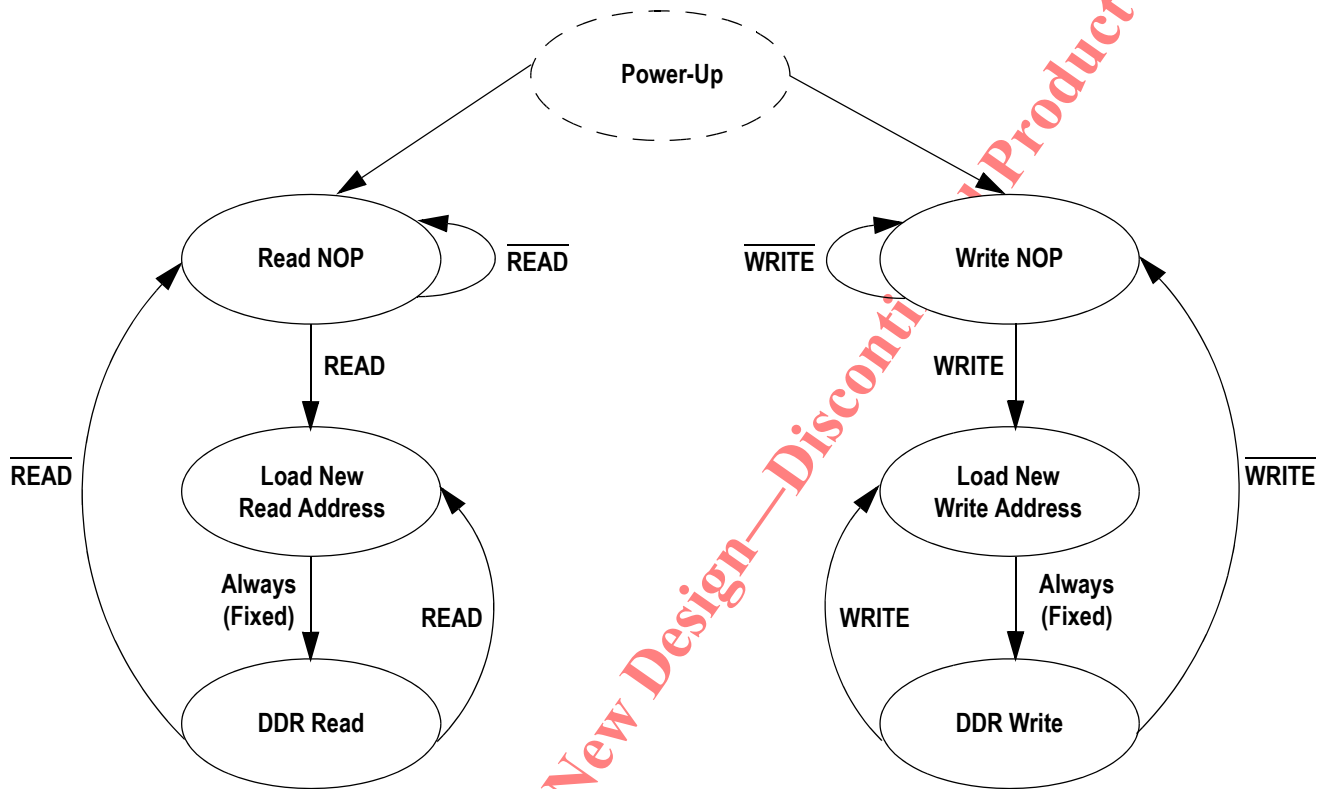
**Notes:**

1. X = Don't Care, H = High, L = Low, V = Valid.
2.  $\bar{W}$  is evaluated on the rising edge of K.
3. D0 and D1 are the first and second data input transfers in a write.
4.  $\overline{BWn}$  represents any of the Byte Write Enable inputs ( $\overline{BW0}$ ,  $\overline{BW1}$ , etc.).

**x18 Byte Write Enable ( $\overline{BWn}$ ) Truth Table**

$\overline{BW0}$	$\overline{BW1}$	D0–D8	D9–D17
1	1	Don't Care	Don't Care
0	1	Data In	Don't Care
1	0	Don't Care	Data In
0	0	Data In	Data In

State Diagram



Notes:

1. Internal burst counter is fixed as 2-bit linear (i.e., when first address is A0), next internal burst address is A0+1.
2. "READ" refers to read active status with  $\overline{R}$  = Low, " $\overline{READ}$ " refers to read inactive status with  $\overline{R}$  = High. The same is true for "WRITE" and " $\overline{WRITE}$ ".
3. Read and write state machine can be active simultaneously.
4. State machine control timing sequence is controlled by K.

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**Absolute Maximum Ratings**

 (All voltages reference to  $V_{SS}$ )

Symbol	Description	Value	Unit
$V_{DD}$	Voltage on $V_{DD}$ Pins	-0.5 to 3.6	V
$V_{DDQ}$	Voltage in $V_{DDQ}$ Pins	-0.5 to 3.6	V
$V_{REF}$	Voltage in $V_{REF}$ Pins	-0.5 to $V_{DDQ}$	V
$V_{I/O}$	Voltage on I/O Pins	-0.5 to $V_{DDQ} + 0.5$ ( $\leq 3.6$ V max.)	V
$V_{IN}$	Voltage on Other Input Pins	-0.5 to $V_{DDQ} + 0.5$ ( $\leq 3.6$ V max.)	V
$I_{IN}$	Input Current on Any Pin	+/-100	mA dc
$I_{OUT}$	Output Current on Any I/O Pin	+/-100	mA dc
$T_J$	Maximum Junction Temperature	125	$^{\circ}\text{C}$
$T_{STG}$	Storage Temperature	-55 to 125	$^{\circ}\text{C}$

**Note:**

Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Recommended Operating Conditions, for an extended period of time, may affect reliability of this component.

**Recommended Operating Conditions**
**Power Supplies**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply Voltage	$V_{DD}$	2.4	2.5	2.6	V	
1.8 V I/O Supply Voltage	$V_{DDQ}$	1.7	1.8	1.95	V	1
1.5 V I/O Supply Voltage	$V_{DDQ}$	1.4	1.5	1.6	V	1
Ambient Temperature (Commercial Range Versions)	$T_A$	0	25	70	$^{\circ}\text{C}$	2
Ambient Temperature (Industrial Range Versions)	$T_A$	-40	25	85	$^{\circ}\text{C}$	2

**Notes:**

- Unless otherwise noted, all performance specifications quoted are evaluated for worst case at both  $1.4 \text{ V} \leq V_{DDQ} \leq 1.6 \text{ V}$  (i.e., 1.5 V I/O) and  $1.7 \text{ V} \leq V_{DDQ} \leq 1.95 \text{ V}$  (i.e., 1.8 V I/O) and quoted at whichever condition is worst case.
- The power supplies need to be powered up simultaneously or in the following sequence:  $V_{DD}$ ,  $V_{DDQ}$ ,  $V_{REF}$ , followed by signal inputs. The power down sequence must be the reverse.  $V_{DDQ}$  must not exceed  $V_{DD}$ .
- Most speed grades and configurations of this device are offered in both Commercial and Industrial Temperature ranges. The part number of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.

**HSTL I/O DC Input Characteristics**

Parameter	Symbol	Min	Max	Units	Notes
DC Input Logic High	$V_{IH} (dc)$	$V_{REF} + 200$		mV	1
DC Input Logic Low	$V_{IL} (dc)$		$V_{REF} - 200$	mV	1
$V_{REF}$ DC Voltage	$V_{REF} (dc)$	$V_{DDQ} (min)/2$	$V_{DDQ} (max)/2$	V	1

**Note:**

Compatible with both 1.8 V and 1.5 V I/O drivers

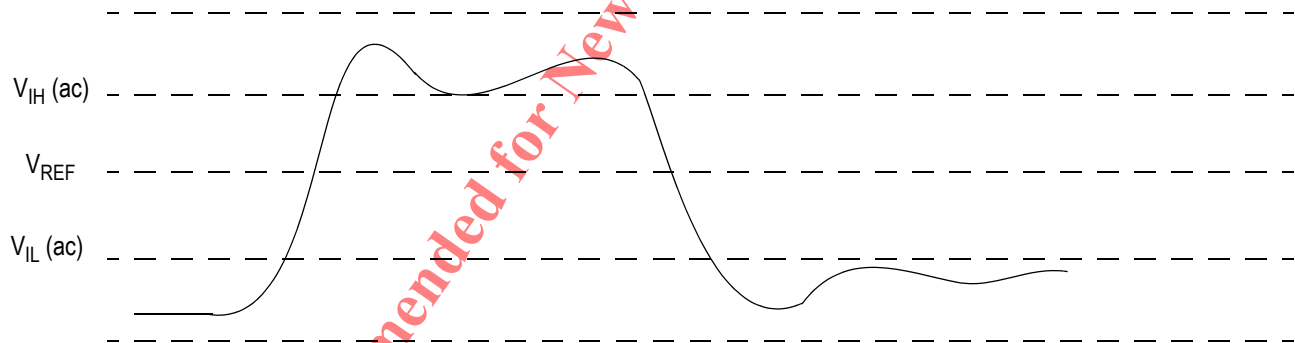
**HSTL I/O AC Input Characteristics**

Parameter	Symbol	Min	Max	Units	Notes
AC Input Logic High	$V_{IH} (ac)$	$V_{REF} + 400$		mV	3,4
AC Input Logic Low	$V_{IL} (ac)$		$V_{REF} - 400$	mV	3,4
$V_{REF}$ Peak to Peak AC Voltage	$V_{REF} (ac)$		5% $V_{REF}$ (DC)	mV	1

**Notes:**

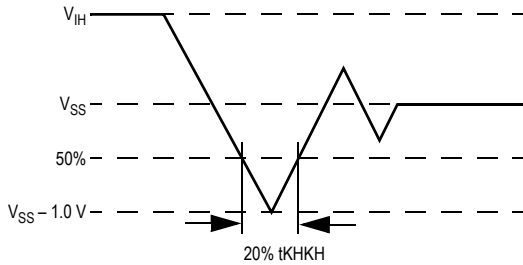
1. The peak to peak AC component superimposed on  $V_{REF}$  may not exceed 5% of the DC component of  $V_{REF}$ .
2. To guarantee AC characteristics,  $V_{IH}$ ,  $V_{IL}$ ,  $T_{rise}$  and  $T_{fall}$  of inputs and clocks must be within 10% of each other.
3. For devices supplied with HSTL I/O input buffers. Compatible with both 1.8 V and 1.5 V I/O drivers.
4. See AC Input Definition drawing below.

**HSTL I/O AC Input Definitions**

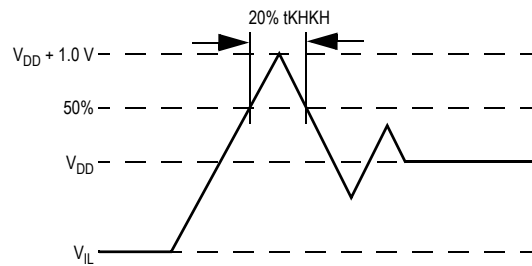


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### Undershoot Measurement and Timing



### Overshoot Measurement and Timing



### Capacitance

( $T_A = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ ,  $V_{DD} = 3.3\text{ V}$ )

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	$C_{IN}$	$V_{IN} = 0\text{ V}$	4	5	pF
Output Capacitance	$C_{OUT}$	$V_{OUT} = 0\text{ V}$	6	7	pF

**Note:**

This parameter is sample tested.

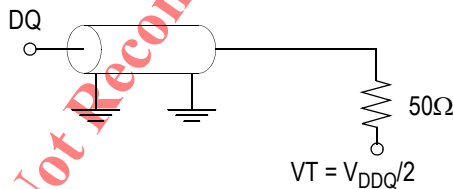
### AC Test Conditions

Parameter	Conditions
Input high level	$V_{DDQ}$
Input low level	0 V
Max. input slew rate	2 V/ns
Input reference level	$V_{DDQ}/2$
Output reference level	$V_{DDQ}/2$

**Notes:**

Test conditions as specified with output loading as shown unless otherwise noted.

### AC Test Load Diagram



$R_Q = 250\ \Omega$  (HSTL I/O)  
 $V_{REF} = 0.75\text{ V}$

**Input and Output Leakage Characteristics**

Parameter	Symbol	Test Conditions	Min.	Max	Notes
Input Leakage Current (except mode pins)	$I_{IL}$	$V_{IN} = 0$ to $V_{DD}$	-2 $\mu$ A	2 $\mu$ A	
Output Leakage Current	$I_{OL}$	Output Disable, $V_{OUT} = 0$ to $V_{DDQ}$	-2 $\mu$ A	2 $\mu$ A	

**Programmable Impedance HSTL Output Driver DC Electrical Characteristics**

Parameter	Symbol	Min.	Max.	Units	Notes
Output High Voltage	$V_{OH1}$	$V_{DDQ}/2$	$V_{DDQ}$	V	1, 3
Output Low Voltage	$V_{OL1}$	$V_{SS}$	$V_{DDQ}/2$	V	2, 3
Output High Voltage	$V_{OH2}$	$V_{DDQ} - 0.2$	$V_{DDQ}$	V	4, 5
Output Low Voltage	$V_{OL2}$	$V_{SS}$	0.2	V	4, 6

**Notes:**

- $I_{OH} = (V_{DDQ}/2) / (RQ/5) \pm 15\%$  @  $V_{OH} = V_{DDQ}/2$  (for:  $175\Omega \leq RQ \leq 350\Omega$ ).
- $I_{OL} = (V_{DDQ}/2) / (RQ/5) \pm 15\%$  @  $V_{OL} = V_{DDQ}/2$  (for:  $175\Omega \leq RQ \leq 350\Omega$ ).
- Parameter tested with  $RQ = 250\Omega$  and  $V_{DDQ} = 1.5$  V or 1.8 V
- Minimum Impedance mode,  $ZQ = V_{SS}$
- $I_{OH} = -1.0$  mA
- $I_{OL} = 1.0$  mA

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**Operating Currents**

Parameter	Symbol	Org.	-200		-167		-133		-100		Test Conditions
			0°C to 70°C	-40°C to +85°C	0°C to 70°C	-40°C to +85°C	0°C to 70°C	-40°C to +85°C	0°C to 70°C	-40°C to +85°C	
Operating Current	IDD	x18	515 mA	525 mA	450 mA	460 mA	375 mA	385 mA	320 mA	330 mA	$\bar{R}$ and $\bar{W} \leq V_{IL}$ Max. $t_{KHKH} \geq t_{KHKH}$ Min. All other inputs $V_{IN} \leq V_{IL}$ Max. or $V_{IN} \geq V_{IH}$ Min.
Operating Current	IDD	x36	630 mA	640 mA	545 mA	555 mA	475 mA	485 mA	390 mA	400 mA	
Chip Disable Current	ISB1	x18	180 mA	190 mA	170 mA	180 mA	165 mA	175 mA	150 mA	160 mA	$\bar{R}$ and $\bar{W} \geq V_{IH}$ Min. $t_{KHKH} \geq t_{KHKH}$ Min. All other inputs $V_{IN} \leq V_{IL}$ Max. or $V_{IN} \geq V_{IH}$ Min.
Chip Disable Current	ISB1	x36	220 mA	230 mA	210 mA	220 mA	195 mA	205 mA	180 mA	190 mA	

**Note:**

Power measured with output pins floating.

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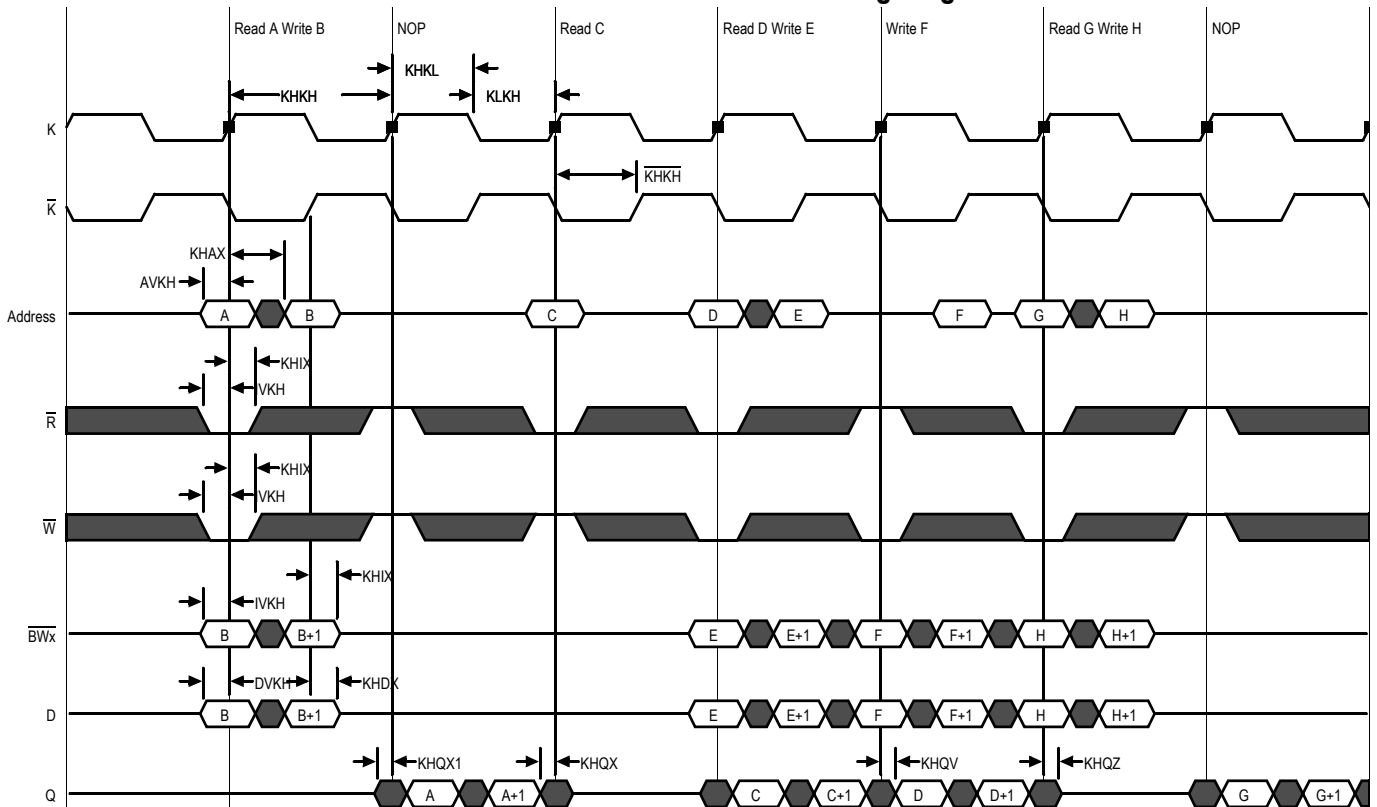
**AC Electrical Characteristics**

Parameter	Symbol	-200		-167		-133		-100		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
K, $\bar{K}$ Clock Cycle Time C, C Clock Cycle Time	$t_{KHKH}$ $t_{CHCH}$	5.0	—	6.0	—	7.5	—	10	—	ns	
K, $\bar{K}$ Clock High Pulse Width C, C Clock High Pulse Width	$t_{KHKL}$ $t_{CHCL}$	2.0	—	2.4	—	3.0	—	3.5	—	ns	
K, $\bar{K}$ Clock Low Pulse Width C, C Clock Low Pulse Width	$t_{KLKH}$ $t_{CLCH}$	2.0	—	2.4	—	3.0	—	3.5	—	ns	
K Clock High to $\bar{K}$ Clock High C Clock High to C Clock High	$t_{KH\bar{K}H}$ $t_{CH\bar{C}H}$	2.2	—	2.7	—	3.4	—	4.6	—	ns	4
$\bar{K}$ Clock High to K Clock High C Clock High to C Clock High	$t_{\bar{K}KH}$ $t_{\bar{C}CH}$	2.2	—	2.7	—	3.4	—	4.6	—	ns	
K, $\bar{K}$ Clock High to C, $\bar{C}$ Clock High	$t_{KHCH}$	0	1.7	0	2.0	0	2.5	0	3.0	ns	
Address Input Setup Time	$t_{AVKH}$	0.6	—	0.7	—	0.8	—	1.0	—	ns	
Address Input Hold Time	$t_{KHAX}$	0.6	—	0.7	—	0.8	—	1.0	—	ns	
Control Input Setup Time	$t_{BVKH}$	0.6	—	0.7	—	0.8	—	1.0	—	ns	1
Control Input Hold Time	$t_{KHBX}$	0.6	—	0.7	—	0.8	—	1.0	—	ns	1
Data and Byte Write Input Setup Time	$t_{DVKH}$	0.6	—	0.7	—	0.8	—	1.0	—	ns	
Data and Byte Write Input Hold Time	$t_{KHDX}$	0.6	—	0.7	—	0.8	—	1.0	—	ns	
K, $\bar{K}$ Clock High to Data Output Valid C, C Clock High to Data Output Valid	$t_{KHQV}$ $t_{CHQV}$	—	2.3	—	2.5	—	3.0	—	3.0	ns	
K, $\bar{K}$ Clock High to Data Output Hold C, C Clock High to Data Output Hold	$t_{KHQX}$ $t_{CHQX}$	1.2	—	1.2	—	1.2	—	1.2	—	ns	2
K Clock High to Data Output Low-Z C Clock High to Data Output Low-Z	$t_{KHQX1}$ $t_{CHQX1}$	1.2	—	1.2	—	1.2	—	1.2	—	ns	2,3
K Clock High to Data Output High-Z C Clock High to Data Output High-Z	$t_{KHQZ}$ $t_{CHQZ}$	—	2.3	—	2.5	—	3.0	—	3.0	ns	2,3

**Notes:**

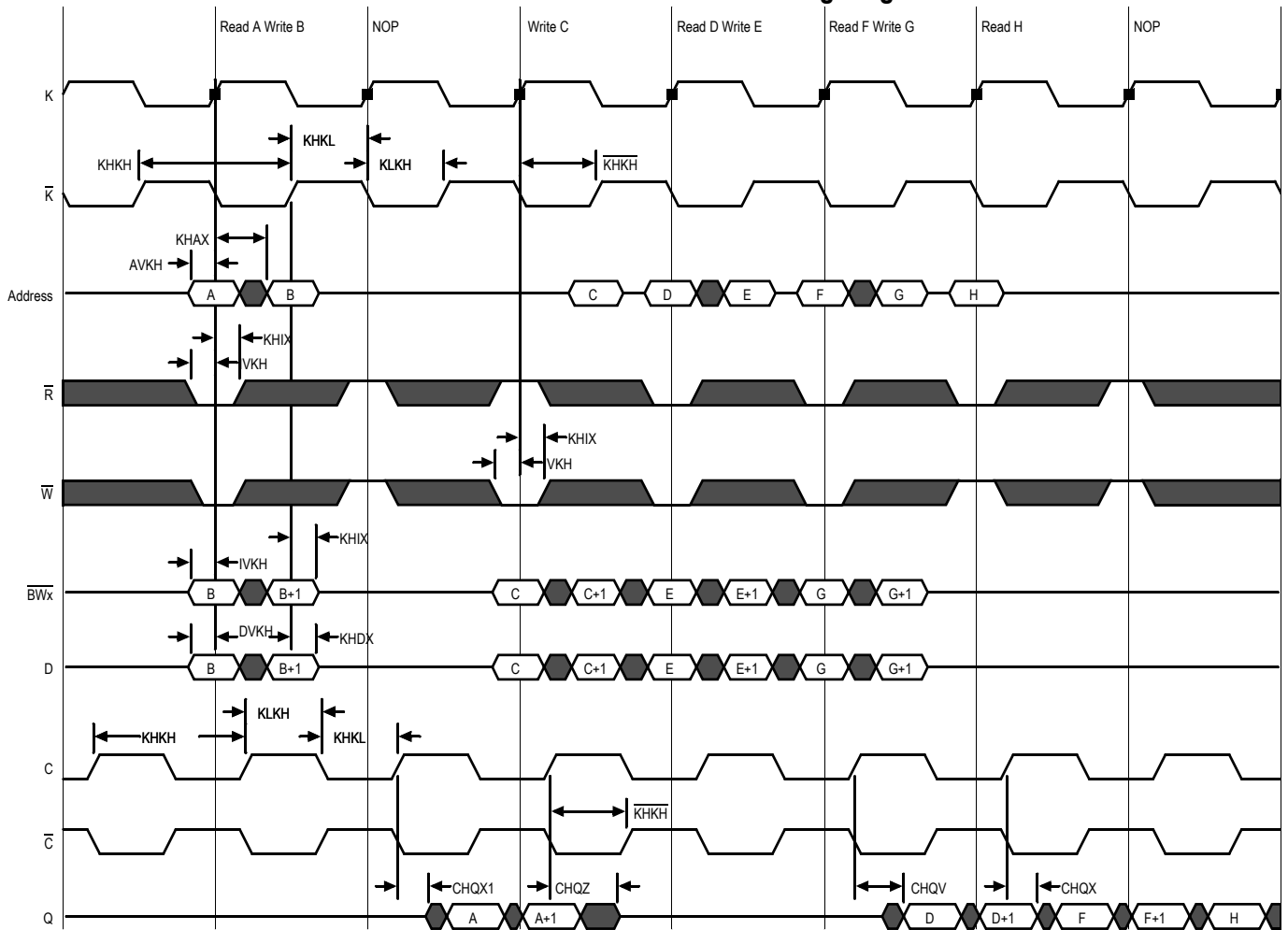
1. These parameters apply to control inputs  $\bar{R}$  and  $\bar{W}$ .
2. These parameters are guaranteed by design and characterization. Not 100% tested.
3. These parameters are measured at  $\pm 50\text{mV}$  from steady state voltage.
4.  $t_{KH\bar{K}H}$  Max is specified by  $t_{KHKH}$  Min.  $t_{CH\bar{C}H}$  Max is specified by  $t_{CHCH}$  Min.

### K and $\bar{K}$ Controlled Read-Write-Read Timing Diagram



Not Recommended for New Designs

### C and $\bar{C}$ Controlled Read-Write-Read Timing Diagram



*Not Recommended for*

## JTAG Port Operation

### Overview

The JTAG Port on this RAM operates in a manner that is compliant with IEEE Standard 1149.1-1990, a serial boundary scan interface standard (commonly referred to as JTAG). The JTAG Port input interface levels scale with  $V_{DD}$ . The JTAG output drivers are powered by  $V_{DDQ}$ .

### Disabling the JTAG Port

It is possible to use this device without utilizing the JTAG port. The port is reset at power-up and will remain inactive unless clocked. TCK, TDI, and TMS are designed with internal pull-up circuits. To assure normal operation of the RAM with the JTAG Port unused, TCK, TDI, and TMS may be left floating or tied to either  $V_{DD}$  or  $V_{SS}$ . TDO should be left unconnected.

## JTAG Pin Descriptions

Pin	Pin Name	I/O	Description
TCK	Test Clock	In	Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	Test Mode Select	In	The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.
TDI	Test Data In	In	The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP Controller state machine and the instruction that is currently loaded in the TAP Instruction Register (refer to the TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.
TDO	Test Data Out	Out	Output that is active depending on the state of the TAP state machine. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

### Note:

This device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1. The Test-Logic-Reset state is entered while TMS is held high for five rising edges of TCK. The TAP Controller is also reset automatically at power-up.

## JTAG Port Registers

### Overview

The various JTAG registers, referred to as Test Access Port or TAP Registers, are selected (one at a time) via the sequences of 1s and 0s applied to TMS as TCK is strobed. Each of the TAP Registers is a serial shift register that captures serial input data on the rising edge of TCK and pushes serial data out on the next falling edge of TCK. When a register is selected, it is placed between the TDI and TDO pins.

### Instruction Register

The Instruction Register holds the instructions that are executed by the TAP controller when it is moved into the Run, Test/Idle, or the various data register states. Instructions are 3 bits long. The Instruction Register can be loaded when it is placed between the TDI and TDO pins. The Instruction Register is automatically preloaded with the IDCODE instruction at power-up or whenever the controller is placed in Test-Logic-Reset state.

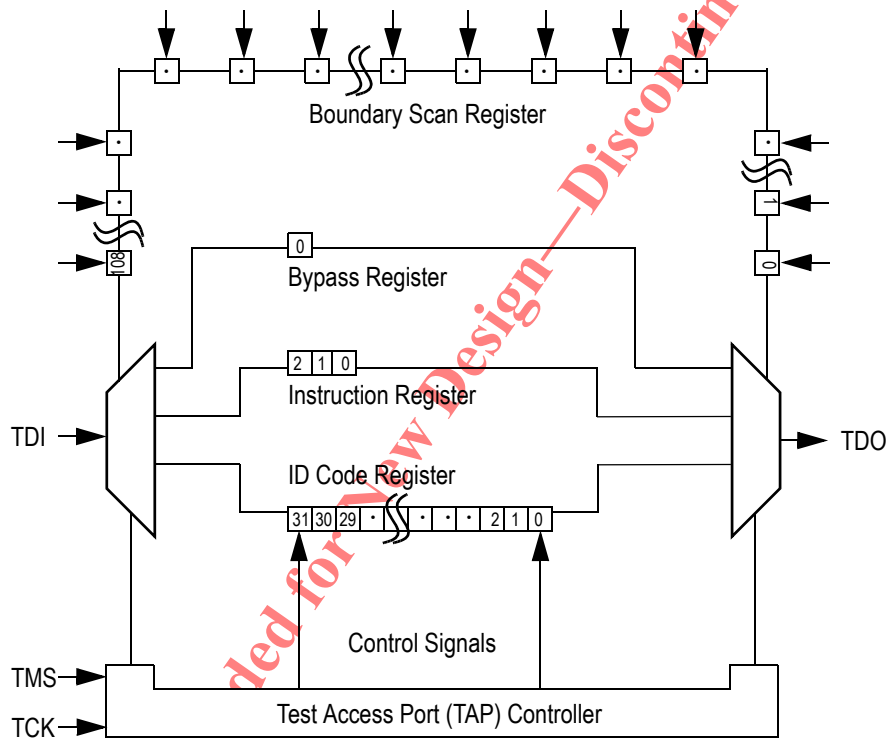
### Bypass Register

The Bypass Register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAM's JTAG Port to another device in the scan chain with as little delay as possible.

**Boundary Scan Register**

The Boundary Scan Register is a collection of flip flops that can be preset by the logic level found on the RAM’s input or I/O pins. The flip flops are then daisy chained together so the levels found can be shifted serially out of the JTAG Port’s TDO pin. The Boundary Scan Register also includes a number of place holder flip flops (always set to a logic 1). The relationship between the device pins and the bits in the Boundary Scan Register is described in the Scan Order Table following. The Boundary Scan Register, under the control of the TAP Controller, is loaded with the contents of the RAMs I/O ring when the controller is in Capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to Shift-DR state. SAMPLE-Z, SAMPLE/PRELOAD and EXTEST instructions can be used to activate the Boundary Scan Register.

**JTAG TAP Block Diagram**



**Identification (ID) Register**

The ID Register is a 32-bit register that is loaded with a device and vendor specific 32-bit code when the controller is put in Capture-DR state with the IDCODE command loaded in the Instruction Register. The code is loaded from a 32-bit on-chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into Shift-DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

**ID Register Contents**

Not Used																GSI Technology JEDEC Vendor ID Code										Presence Register						
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	1	1	0	1	1	0	0	1	1

**Tap Controller Instruction Set**

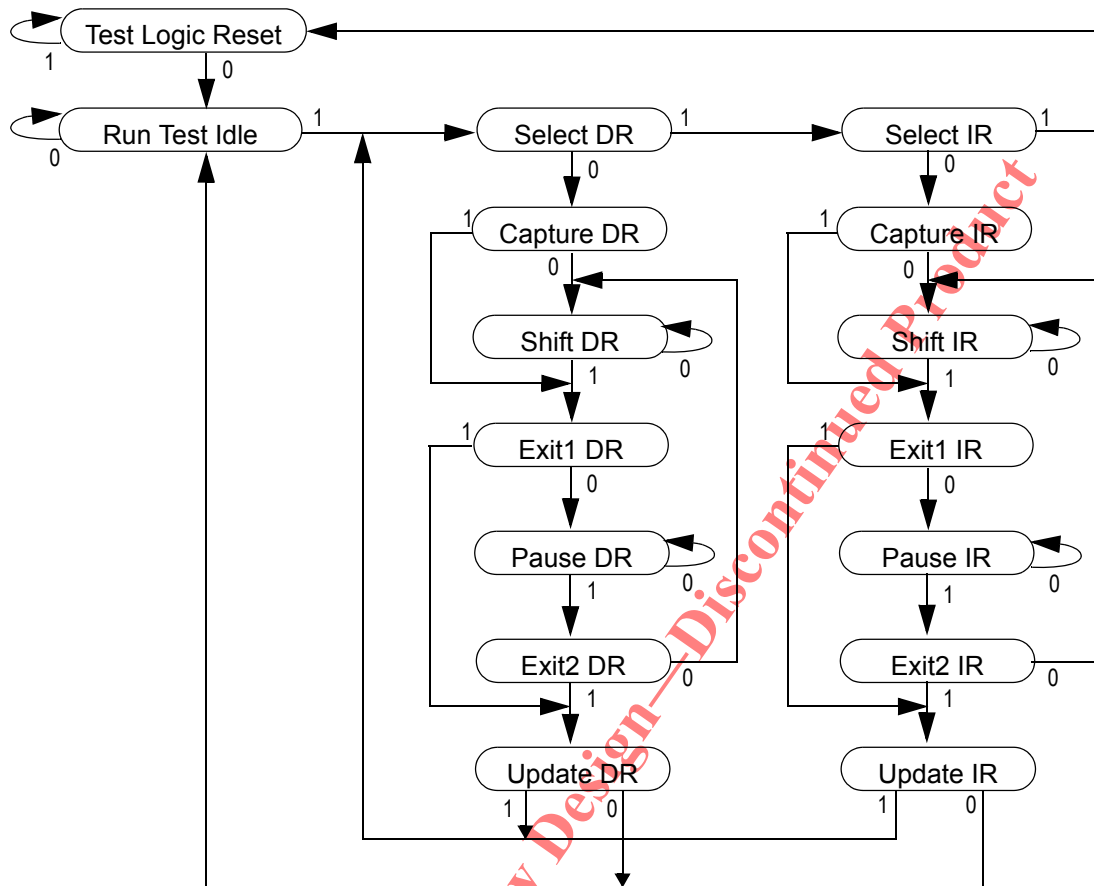
**Overview**

There are two classes of instructions defined in the Standard 1149.1-1990; the standard (Public) instructions, and device specific (Private) instructions. Some Public instructions are mandatory for 1149.1 compliance. Optional Public instructions must be implemented in prescribed ways. The TAP on this device may be used to monitor all input and I/O pads, and can be used to load address, data or control signals into the RAM or to preload the I/O buffers.

When the TAP controller is placed in Capture-IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the Shift-IR state the Instruction Register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to Update-IR state. The TAP instruction set for this device is listed in the following table.

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### JTAG Tap Controller State Diagram



#### Instruction Descriptions

##### BYPASS

When the BYPASS instruction is loaded in the Instruction Register the Bypass Register is placed between TDI and TDO. This occurs when the TAP controller is moved to the Shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

##### SAMPLE/PRELOAD

SAMPLE/PRELOAD is a Standard 1149.1 mandatory public instruction. When the SAMPLE / PRELOAD instruction is loaded in the Instruction Register, moving the TAP controller into the Capture-DR state loads the data in the RAMs input and I/O buffers into the Boundary Scan Register. Boundary Scan Register locations are not associated with an input or I/O pin, and are loaded with the default state identified in the Boundary Scan Chain table at the end of this section of the datasheet. Because the RAM clock is independent from the TAP Clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture set-up plus hold time ( $t_{TS}$  plus  $t_{TH}$ ). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the Boundary Scan Register. Moving the controller to Shift-DR state then places the boundary scan register between the TDI and TDO pins.

##### EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register is loaded with all logic 0s. The EXTEST command does not block or override the RAM's input pins; therefore, the RAM's internal state is



still determined by its input pins.

Typically, the Boundary Scan Register is loaded with the desired pattern of data with the SAMPLE/PRELOAD command. Then the EXTEST command is used to output the Boundary Scan Register's contents, in parallel, on the RAM's data output drivers on the falling edge of TCK when the controller is in the Update-IR state.

Alternately, the Boundary Scan Register may be loaded in parallel using the EXTEST command. When the EXTEST instruction is selected, the state of all the RAM's input and I/O pins, as well as the default values at Scan Register locations not associated with a pin, are transferred in parallel into the Boundary Scan Register on the rising edge of TCK in the Capture-DR state, the RAM's output pins drive out the value of the Boundary Scan Register location with which each output pin is associated.

#### IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in Capture-DR mode and places the ID register between the TDI and TDO pins in Shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the Test-Logic-Reset state.

#### SAMPLE-Z

If the SAMPLE-Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high-Z) and the Boundary Scan Register is connected between TDI and TDO when the TAP controller is moved to the Shift-DR state.

#### RFU

These instructions are Reserved for Future Use. In this device they replicate the BYPASS instruction.

#### JTAG TAP Instruction Set Summary

Instruction	Code	Description	Notes
EXTEST	000	Places the Boundary Scan Register between TDI and TDO.	1
IDCODE	001	Preloads ID Register and places it between TDI and TDO.	1, 2
SAMPLE-Z	010	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. Forces all RAM output drivers to High-Z.	1
RFU	011	Do not use this instruction; Reserved for Future Use. Replicates BYPASS instruction. Places Bypass Register between TDI and TDO.	1
SAMPLE/ PRELOAD	100	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO.	1
GSI	101	GSI private instruction.	1
RFU	110	Do not use this instruction; Reserved for Future Use. Replicates BYPASS instruction. Places Bypass Register between TDI and TDO.	1
BYPASS	111	Places Bypass Register between TDI and TDO.	1

#### Notes:

1. Instruction codes expressed in binary, MSB on left, LSB on right.
2. Default instruction automatically loaded at power-up and in test-logic-reset state.

**JTAG Port Recommended Operating Conditions and DC Characteristics**

Parameter	Symbol	Min.	Max.	Unit	Notes
Test Port Input Low Voltage	$V_{ILJ}$	-0.3	$0.3 * V_{DD}$	V	1
Test Port Input High Voltage	$V_{IHJ}$	$0.6 * V_{DD}$	$V_{DD} + 0.3$	V	1
TMS, TCK and TDI Input Leakage Current	$I_{INHJ}$	-300	1	uA	2
TMS, TCK and TDI Input Leakage Current	$I_{INLJ}$	-1	100	uA	3
TDO Output Leakage Current	$I_{OLJ}$	-1	1	uA	4
Test Port Output High Voltage	$V_{OHJ}$	1.7	—	V	5, 6
Test Port Output Low Voltage	$V_{OLJ}$	—	0.4	V	5, 7
Test Port Output CMOS High	$V_{OHJC}$	$V_{DDQ} - 100$ mV	—	V	5, 8
Test Port Output CMOS Low	$V_{OLJC}$	—	100 mV	V	5, 9

**Notes:**

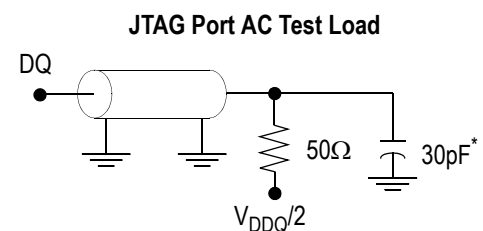
- Input Under/overshoot voltage must be  $-1\text{ V} < V_i < V_{DDn} + 1\text{ V}$  not to exceed 3.6 V maximum, with a pulse width not to exceed 20% tTKC.
- $V_{ILJ} \leq V_{IN} \leq V_{DDn}$
- $0\text{ V} \leq V_{IN} \leq V_{ILJn}$
- Output Disable,  $V_{OUT} = 0$  to  $V_{DDn}$
- The TDO output driver is served by the  $V_{DDQ}$  supply.
- $I_{OHJ} = -4\text{ mA}$
- $I_{OLJ} = +4\text{ mA}$
- $I_{OHJC} = -100\text{ uA}$
- $I_{OLJC} = +100\text{ uA}$

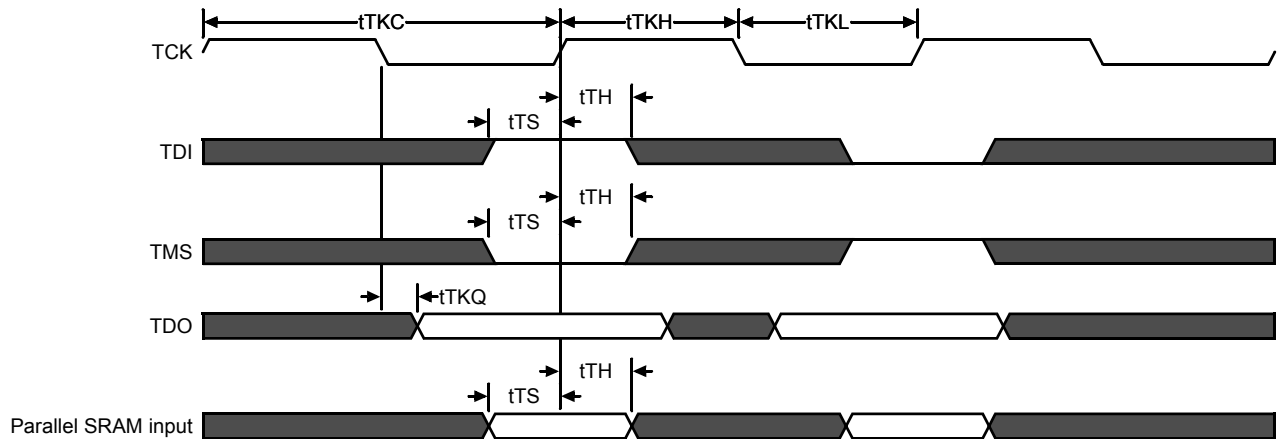
**JTAG Port AC Test Conditions**

Parameter	Conditions
Input high level	$V_{DD} - 0.2\text{ V}$
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	$V_{DDQ}/2$
Output reference level	$V_{DDQ}/2$

**Notes:**

- Include scope and jig capacitance.
- Test conditions as shown unless otherwise noted.

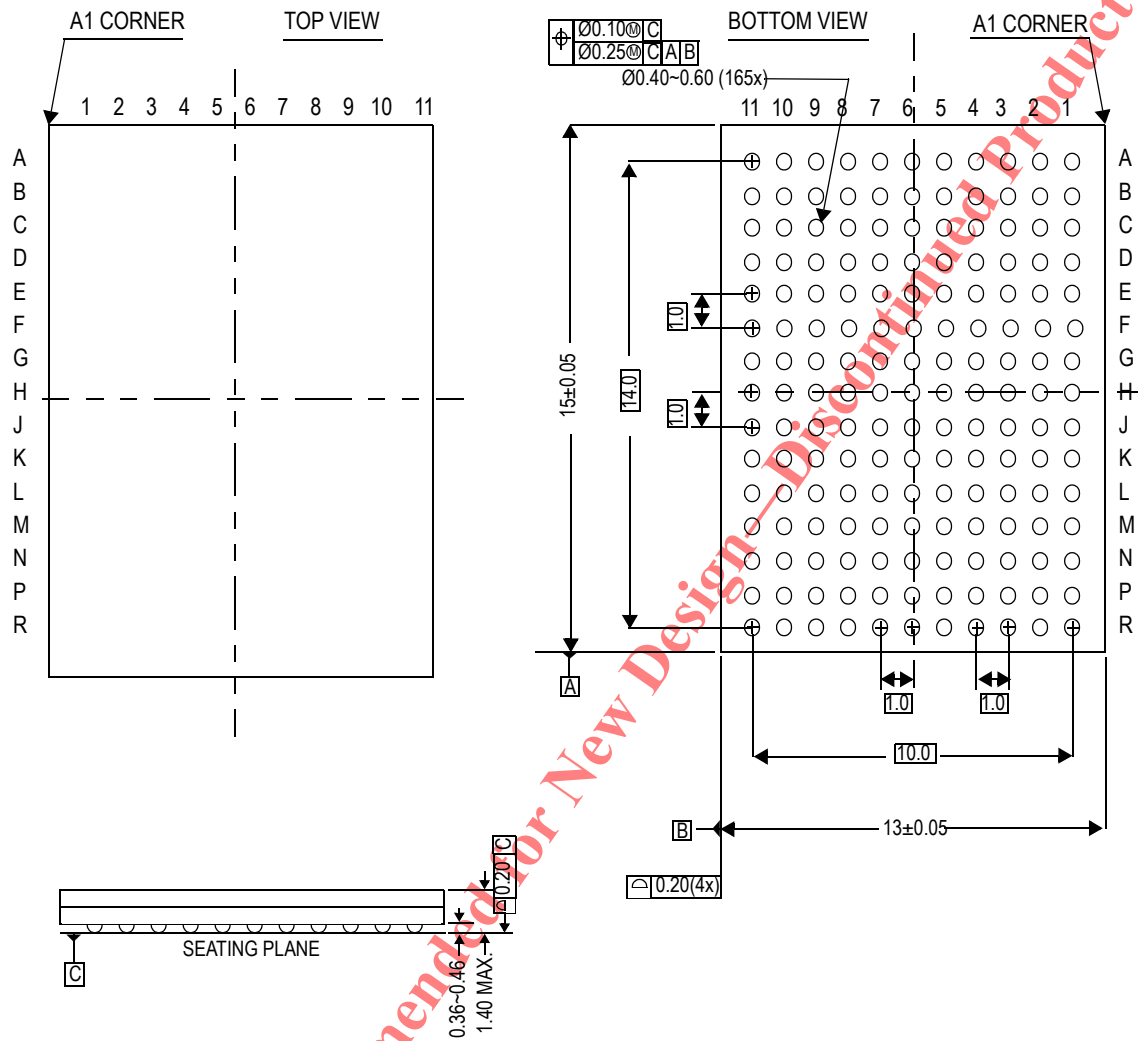


**JTAG Port Timing Diagram**

**JTAG Port AC Electrical Characteristics**

Parameter	Symbol	Min	Max	Unit
TCK Cycle Time	$t_{TKC}$	50	—	ns
TCK Low to TDO Valid	$t_{TKQ}$	—	20	ns
TCK High Pulse Width	$t_{TKH}$	20	—	ns
TCK Low Pulse Width	$t_{TKL}$	20	—	ns
TDI & TMS Set Up Time	$t_{TS}$	10	—	ns
TDI & TMS Hold Time	$t_{TH}$	10	—	ns

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Package Dimensions—165-Bump FPBGA (Package D)



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**Ordering Information—GSI SigmaQuad SRAM**

Org	Part Number <sup>1</sup>	Type	Package	Speed (MHz)	T <sub>A</sub> <sup>2</sup>	Status <sup>3</sup>
1M x 18	GS8180QV18D-200	SigmaQuad SRAM	165-Pin BGA	200	C	MP
1M x 18	GS8180QV18D-167	SigmaQuad SRAM	165-Pin BGA	167	C	MP
1M x 18	GS8180QV18D-133	SigmaQuad SRAM	165-Pin BGA	133	C	MP
1M x 18	GS8180QV18D-100	SigmaQuad SRAM	165-Pin BGA	100	C	MP
512K x 36	GS8180QV36D-200	SigmaQuad SRAM	165-Pin BGA	200	C	MP
512K x 36	GS8180QV36D-167	SigmaQuad SRAM	165-Pin BGA	167	C	MP
512K x 36	GS8180QV36D-133	SigmaQuad SRAM	165-Pin BGA	133	C	MP
512K x 36	GS8180QV36D-100	SigmaQuad SRAM	165-Pin BGA	100	C	MP
1M x 18	GS8180QV18D-200I	SigmaQuad SRAM	165-Pin BGA	200	I	MP
1M x 18	GS8180QV18D-167I	SigmaQuad SRAM	165-Pin BGA	167	I	MP
1M x 18	GS8180QV18D-133I	SigmaQuad SRAM	165-Pin BGA	133	I	MP
1M x 18	GS8180QV18D-100I	SigmaQuad SRAM	165-Pin BGA	100	I	MP
512K x 36	GS8180QV36D-200I	SigmaQuad SRAM	165-Pin BGA	200	I	MP
512K x 36	GS8180QV36D-167I	SigmaQuad SRAM	165-Pin BGA	167	I	MP
512K x 36	GS8180QV36D-133I	SigmaQuad SRAM	165-Pin BGA	133	I	MP
512K x 36	GS8180QV36D-100I	SigmaQuad SRAM	165-Pin BGA	100	I	MP
1M x 18	GS8180QV18GD-200	SigmaQuad SRAM	RoHS-compliant 165-Pin BGA	200	C	MP
1M x 18	GS8180QV18GD-167	SigmaQuad SRAM	RoHS-compliant 165-Pin BGA	167	C	MP
1M x 18	GS8180QV18GD-133	SigmaQuad SRAM	RoHS-compliant 165-Pin BGA	133	C	MP
1M x 18	GS8180QV18GD-100	SigmaQuad SRAM	RoHS-compliant 165-Pin BGA	100	C	MP
512K x 36	GS8180QV36GD-200	SigmaQuad SRAM	RoHS-compliant 165-Pin BGA	200	C	MP
512K x 36	GS8180QV36GD-167	SigmaQuad SRAM	RoHS-compliant 165-Pin BGA	167	C	MP
512K x 36	GS8180QV36GD-133	SigmaQuad SRAM	RoHS-compliant 165-Pin BGA	133	C	MP
512K x 36	GS8180QV36GD-100	SigmaQuad SRAM	RoHS-compliant 165-Pin BGA	100	C	MP
1M x 18	GS8180QV18GD-200I	SigmaQuad SRAM	RoHS-compliant 165-Pin BGA	200	I	MP
1M x 18	GS8180QV18GD-167I	SigmaQuad SRAM	RoHS-compliant 165-Pin BGA	167	I	MP
1M x 18	GS8180QV18GD-133I	SigmaQuad SRAM	RoHS-compliant 165-Pin BGA	133	I	MP
1M x 18	GS8180QV18GD-100I	SigmaQuad SRAM	RoHS-compliant 165-Pin BGA	100	I	MP

**Notes:**

- Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS818x18D-200T.
- T<sub>A</sub> = C = Commercial Temperature Range. T<sub>A</sub> = I = Industrial Temperature Range.
- MP = Mass Production.

Ordering Information—GSI SigmaQuad SRAM

Org	Part Number <sup>1</sup>	Type	Package	Speed (MHz)	T <sub>A</sub> <sup>2</sup>	Status <sup>3</sup>
512K x 36	GS8180QV36GD-200I	SigmaQuad SRAM	RoHS-compliant 165-Pin BGA	200	I	MP
512K x 36	GS8180QV36GD-167I	SigmaQuad SRAM	RoHS-compliant 165-Pin BGA	167	I	MP
512K x 36	GS8180QV36GD-133I	SigmaQuad SRAM	RoHS-compliant 165-Pin BGA	133	I	MP
512K x 36	GS8180QV36GD-100I	SigmaQuad SRAM	RoHS-compliant 165-Pin BGA	100	I	MP

**Notes:**

1. Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS818x18D-200T.
2. T<sub>A</sub> = C = Commercial Temperature Range. T<sub>A</sub> = I = Industrial Temperature Range.
3. MP = Mass Production.

Not Recommended for New Design—Discontinued Product