# DM9008AEP Product Brief

## Ethernet Controller with General Processor Interface

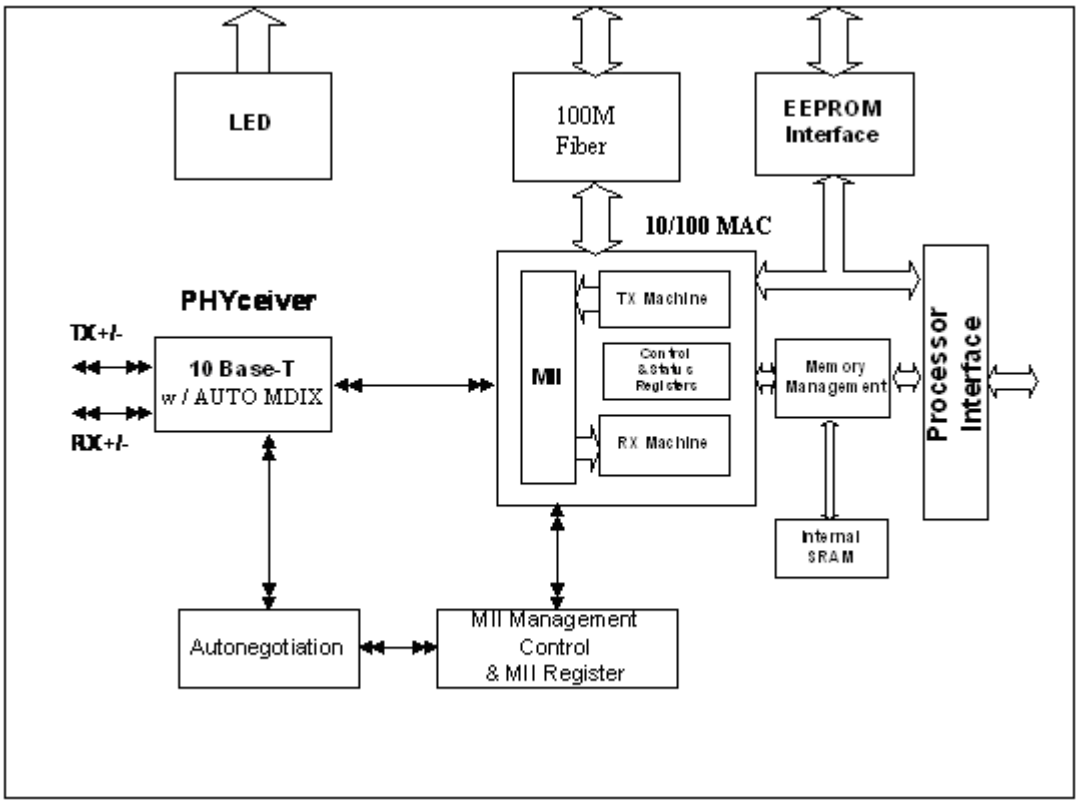
June 2008 Rev.1.0

The DM9008A is a fully integrated and cost-effective low pin count Ethernet controller with a general processor interface, a Medial Access Control (MAC), a 10Base-T PHY and 16K Byte SRAM. It is designed with low power and high performance process that support 3.3V with 5V IO tolerance.

The DM9008A supports 8-bit and 16-bit data interfaces to internal memory accesses for various processors. The DM9008A also supports full duplex mode

The PHY of the DM9008A can interface to the UTP3, 4, 5 in 10Base-T that is fully compliant with the IEEE 802.3 Spec.. The HP Auto-MDIX function of PHY is also supported to improve the media connection in convenience.

## Block Diagram



## Specifications

- 48-pin LQFP
- Supports processor interface: byte/word of I/O command to internal memory data operation
- Comply to 10BASE-T of IEEE 802.3 with HP Auto-MDIX
- Supports back pressure mode for half-duplex mode flow control
- Support 100M Fiber interface.
- IEEE802.3x flow control for full-duplex mode
- Supports wakeup frame, link status change and magic packet events for remote wake up
- Integrated 16K Byte SRAM
- Build in 3.3V to 2.5V regulator
- Supports early Transmit
- Supports automatically load vendor ID and product ID from EEPROM
- Optional EEPROM configuration
- Very low power consumption mode:
  - Power reduced mode (cable detection)
  - Power down mode
  - Selectable TX drivers for 1:1 or 1.25:1 transformers for additional power reduction.
- Compatible with 3.3V and 5.0V tolerant I/O

## Application

VoIP CPE (ATA, IP Phone, Video Phone)
IP STB, IPC, Internet Radio

## Ordering Information

| Part Number | Pin Count | Package |
|---|---|---|
| DM9008AEP | 48 | LQFP<br>(Pb-Free) |

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