AN1288
APPLICATION NOTE

STSRx FAMILY: MIXED-SIGNAL ICs TO DRIVE SYNCHRONOUS RECTIFIERS IN ISOLATED SMPSs

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1. ABSTRACT

A methodology capable to digitally control and, in particular, properly turn-off one or two MOSFETs used as rectifiers in switched mode power supply (SMPS) isolated topologies will be described in this application note. Basic circuit implementation of the proposed technique is also introduced. From a main input, denominated Clock, generically swinging from a low to a high value, in two different time intervals, one or two square wave outputs, swinging from low to high in phase or in opposite with respect to the clock signal are generated. The digital control method is able to generate an output signals timing, so to anticipate output transitions from high to low levels with respect to the clock signal transitions. This technique makes it possible to realize a smart driver IC family (STSRx) for isolated SMPS topologies with the PWM controller located on the primary side. These ICs, deriving the clock signal from the secondary output of the isolation transformer, are able to provide the proper gate drive signals to drive one or two synchronous rectifier MOSFETs gates, solving all the known problems in controlling synchronous rectification.

2. INTRODUCTION.

In the power conversion area, in low DC output voltage converters, the utilization of MOSFETs as rectifiers is a technique increasingly used for the beneficial effects on efficiency due to the reduced conduction losses on these devices.

The way the synchronous rectifiers (SRs) are controlled is fundamental for the correct operation of the circuit. Proper techniques must be used to drive the SRs according to the law of the diode that the SR is meant to replace. This driving signal has to be derived from the main PWM control signal, which determines the different states of the switch mode circuit and therefore the operating conditions for the diodes of the circuit.

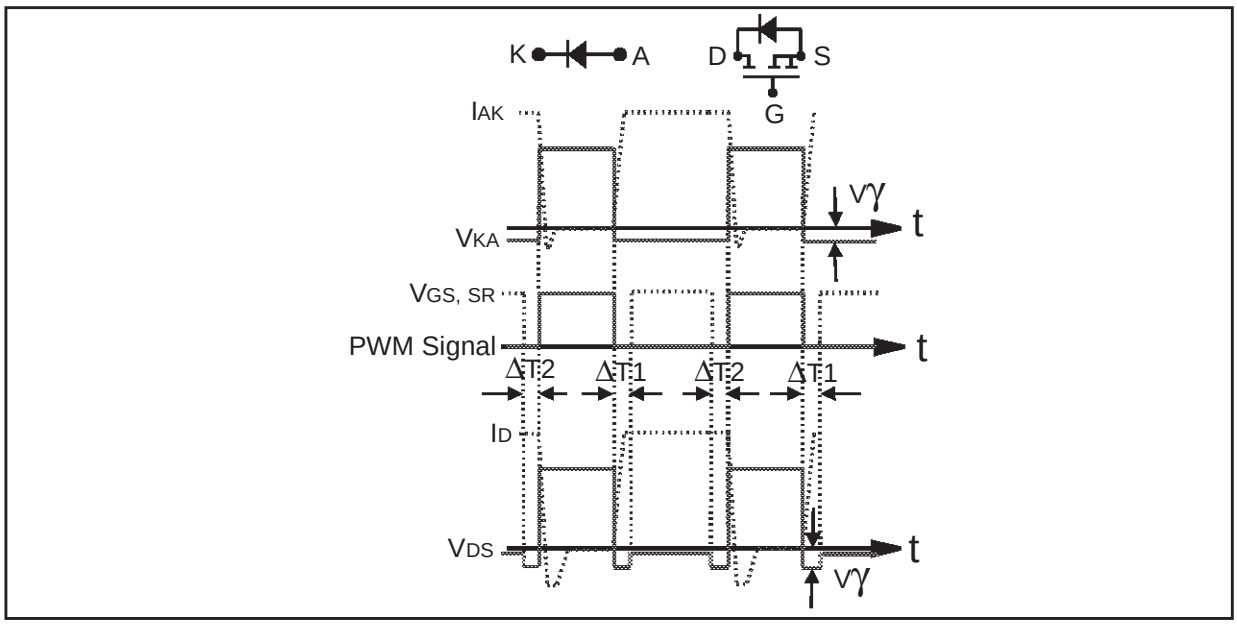
The way the driving signal is derived from the main PWM signal to properly control SRs depends on the kind of topology used, and the presence of galvanic isolation in it. In a non-isolated SMPS topology, the synchronous rectifiers control circuit can get the information about the switching transitions (turn-off and turn-on of the main switch) from the main control circuit in a very simple way.

In isolated topologies, with primary side control, the absence of PWM controlling signal in the secondary side of the isolation barrier makes the generation of the proper SRs control signals even more difficult.
If the equivalent diode law is not respected cross conduction or shoot-through between switches will

occur. This will be described in detail in the following. In all of these circumstances one of the switches is forced to conduct in the first quadrant, opposite its useful sense of conduction as a diode. Therefore, switching losses can become predominant, spoiling most of the benefits introduced by the reduction of conduction losses on the rectifiers, or even bringing to destructive operations.

The required timing of the driving signal for the synchronous rectifier is showed in figure 1, according to a general switch mode topology configuration with one switch and only one diode, where the conduction times possible for switch and diode are complementary.

Figure 1: Synchronous Rectification Concept



The dead time intervals carry out the function of preventing contemporary conduction (cross-conduction) of the main switch and the SR, but they must be reduced to the lowest possible value to minimize SR parasitic diode conduction times and consequent lost of efficiency. The switching losses caused by the reverse recovery current of the body-diode will be dependent of the carried current in the instant in which the voltage between anode and cathode reverses become negative.

3. SYNCHRONOUS RECTIFICATION IN ISOLATED TOPOLOGIES.

In isolated topologies, if the main PWM controller is located on the secondary side, the task of driving synchronous rectifiers can be easily solved. In fact, having PWM signals available on the secondary side it can be used to generate the driving signal for the SRs by adding proper delays to each transition to compensate the propagation delays which are suffered by the driving signal transferred to the primary side through a coupling device.

However, the secondary side control configuration shows several system disadvantages such as requirement of an auxiliary power supply for start-up of the converter, requirement of a crossing-isolation circuit able to transfer the PWM control driving signal to the primary switches and difficulties to transfer the information about the primary switch current to the PWM controller in current mode control loops.

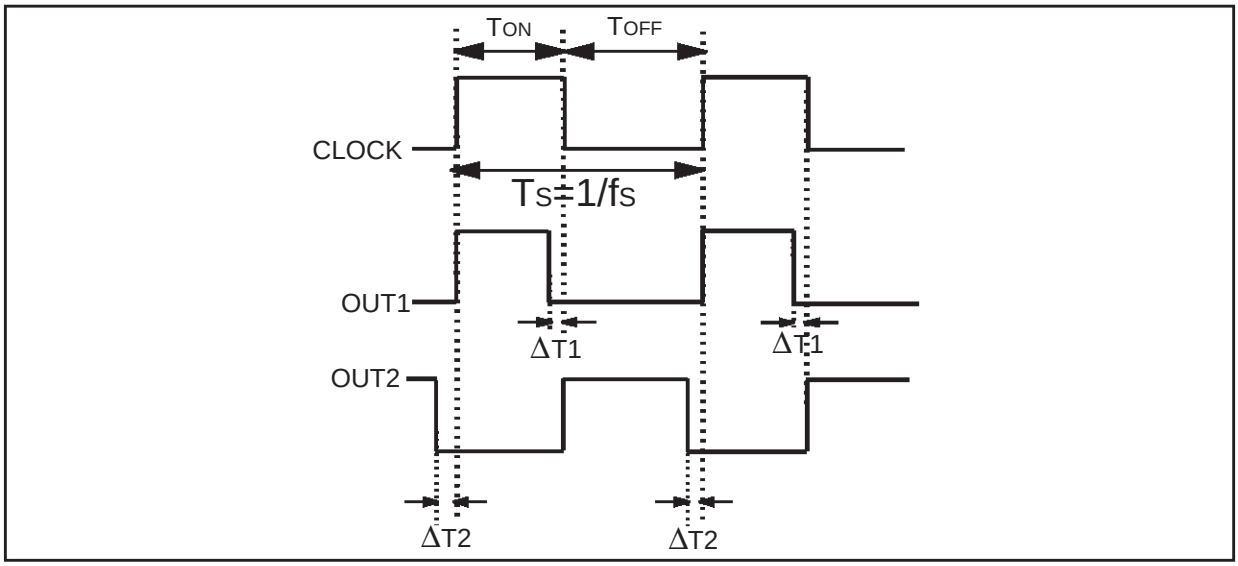
Therefore, the use of PWM control on the primary side is mandatory to realize SMPS with top performances in terms of high efficiency, small dimension and low cost.

In isolated topologies, if the main PWM control circuit is on the primary side, its output signal cannot be available on the secondary side in a simple, effective and cheap way. This information can be however derived on the secondary side from the output of the isolation transformer. Due to the parasitic elements of the circuit, the synchronizing signal withdrawn at the output of the isolation transformer is delayed with respect to the primary PWM signal and may present some oscillations especially in discontinuous conduction mode. Therefore, the control technique meant to provide SRs driving must be able to prevent eventual rising of wrong operative conditions derived by any timing effect on the synchronization of the signal available on the secondary (PWM synchronization signal) with respect to the primary PWM signal.

Using the output of the isolation transformer as the PWM synchronization signal, a very simple way to make MOSFETs operate as rectifiers in isolated topologies based on forward topology is the technique called “self-driven synchronous rectification”.

Unfortunately, this technique has a very serious inconvenience. In fact, the driving signal is depends on the way in which the main transformer is demagnetized (magnetic reset). As a consequence, the time in which the body diodes of the free-wheeling MOSFET is forced to conduct can be very large, due to the fact that the driving signal for the gate is missing. This fact damages the main benefits introduced by synchronous rectification, restricting the use of this method for driving SRs only in combination with some particular, and proprietary magnetic reset techniques.

Figure 2: Synchronous Rectifier Driving Signals



In addition, this technique is hard to implement when the primary input voltage varies (the common factors are 2:1) in difficulty to always provide a value of driving signal compatible with the gates ranges.

Therefore, in isolated topologies with primary side control, the most proper approach to drive synchronous rectifiers requires a control circuit able to handle the synchronization signal (Clock) withdrawn from the output of the isolation transformer, and to solve any other problem regarding the timing of the driving signals for the two mosfets with respect to the clock input. In figure 2 the general Clock signal is displayed at a fixed switching frequency with the primary On and Off switch time intervals together with two complementary SR driving signals (OUT1 and OUT2).

4. CROSS-CONDUCTION AND SHOOT-THROUGH PROBLEMS.

The control circuit, necessary to use synchronous rectifiers in isolated topologies in simple ways, has to deal with proper timing generation of the SR driving signal from the clock signal input. According to figure 2, as already explained, proper deadtimes between clock signal and SR driving signal must be provided to avoid cross conduction between devices.

Another well-known phenomenon to be dealt with by the controller is the so called “shoot through problem” that may happen on the secondary side of an isolated topology. The specific mechanism of this wrong operation condition is dependent on the circuit topology, and it will be dealt with in detail in the following. In general, while the transition in which a synchronous rectifier has to be turned on reveals to be easy to deal with, the turn-off transition requires a special treatment. In fact, the circuitry that generates the driving signal from the clock introduces a propagation delay which is added to the one coming from the isolation transformer. In generating the SR transition, this intrinsic delay creates the dead time necessary to avoid wrong circuit conditions. This delay has to be minimized, because it causes body diode conduction, bringing penalties in terms of loss of efficiency.

If the turn-off transitions for Out1 and Out2 (seen in figure 2) are not properly handled the circuit will show a very critical behavior. In fact, in this case, the intrinsic delay generates late turn-off of the bi-directional synchronous rectifiers switches creating wrong circuit conditions made normally impossible for the presence of the unidirectional diodes. The general condition can be defined as the creation of short circuit loops which can generate very high current peaks, limited only by the parasitic elements in the circuit. The particular analysis of this phenomenon will be described in details for each of the main isolated topology family.

Therefore, the introduction of a special deadtime is necessary in order to be able to avoid the generation of the wrong operation conditions. This can be realized by generating a proper anticipation of the turn-off transition that is able to guarantee that the SR can be off before the clock signal transition. This anticipation, however, as in the turn-on transition, has to be minimized to reduce the body-diode conduction time in order to avoid penalties on the efficiency. In particular, the amount of anticipation can be used as on optimization parameter to adjust the operation of the circuit to its physical implementation by design. In fact, the time slope of the decreasing current on the SR which has been turned off is dependent by several parameters, such as input and output voltage of the converter, the amount of previously driven current and, above all, by the parasitic elements in the circuit like the leakage inductance. The anticipation time can be adapted to the specific operation condition of the circuit to achieve the best performance in terms of efficiency, setting to minimum the conduction times of the body-diodes and the consequent reverse recovery currents.

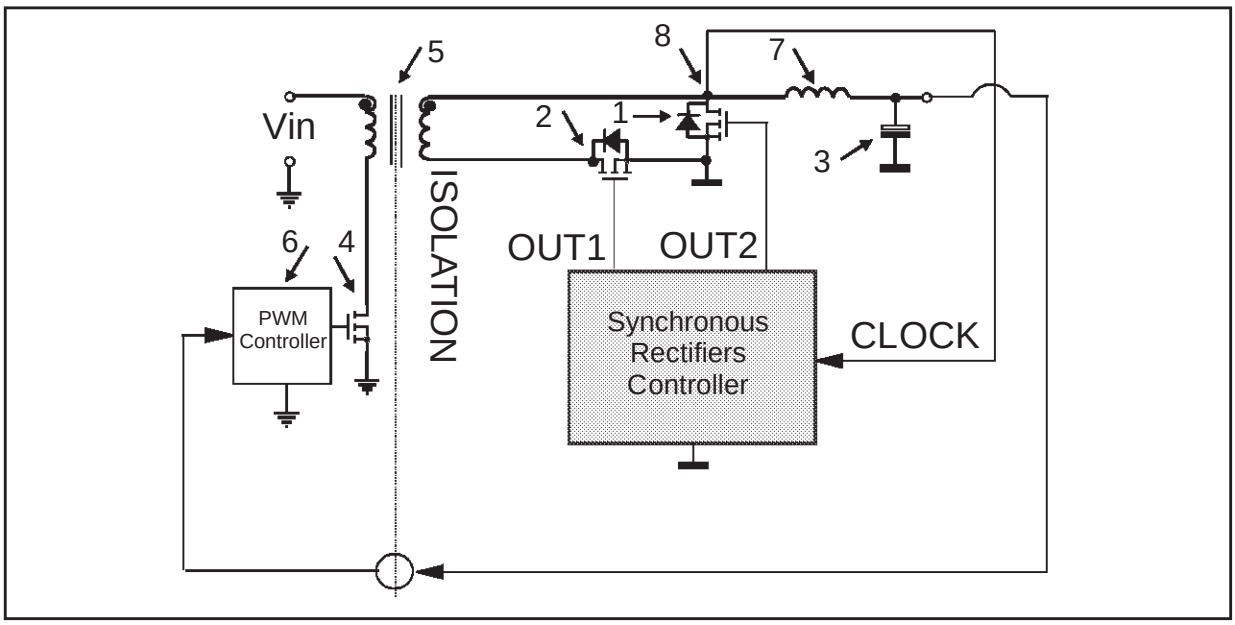
In figure 2 the required anticipation intervals, denominated by ΔT1 and ΔT2, are introduced in the most general case of two complementary SR driving signals generated from a clock input.

The mechanism of generation of the shoot-through will now be examined for the main isolated topologies of SMPS converters.

4a. Single Ended Forward Topology

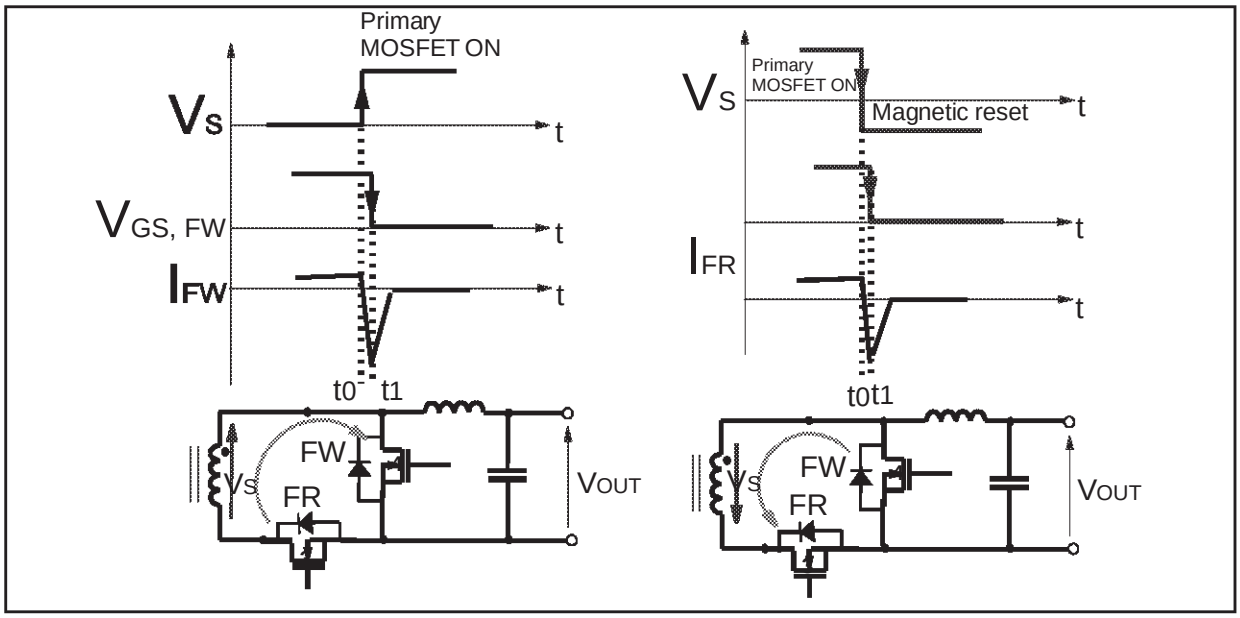
Now we will examine the operations in a single ended forward topology circuit pointing out in particular the eventual generation of the shoot-through, displayed in figure 3.

Figure 3: Control Driven Synchronous Rectification In Forward Topology



The synchronous rectifiers control circuit, achieving the clock information from the voltage on the node (8), generates the MOSFET driving signals for the forward rectifier (FR) and for free-wheeling (FW). The voltage formation on node (8) shows some delay with respect to the primary MOSFET (4) driving signal, mainly coming from the isolation transformer (5) parasitic. This delay, added to the propagation delay of the SRs Controller, causes a delayed turn-off of the SR(1) or of the SR(2), and as a consequence shoot-through on the secondary output of the isolation transformer loop occurs in both transitions in which the MOSFET (4) is turned on or off.

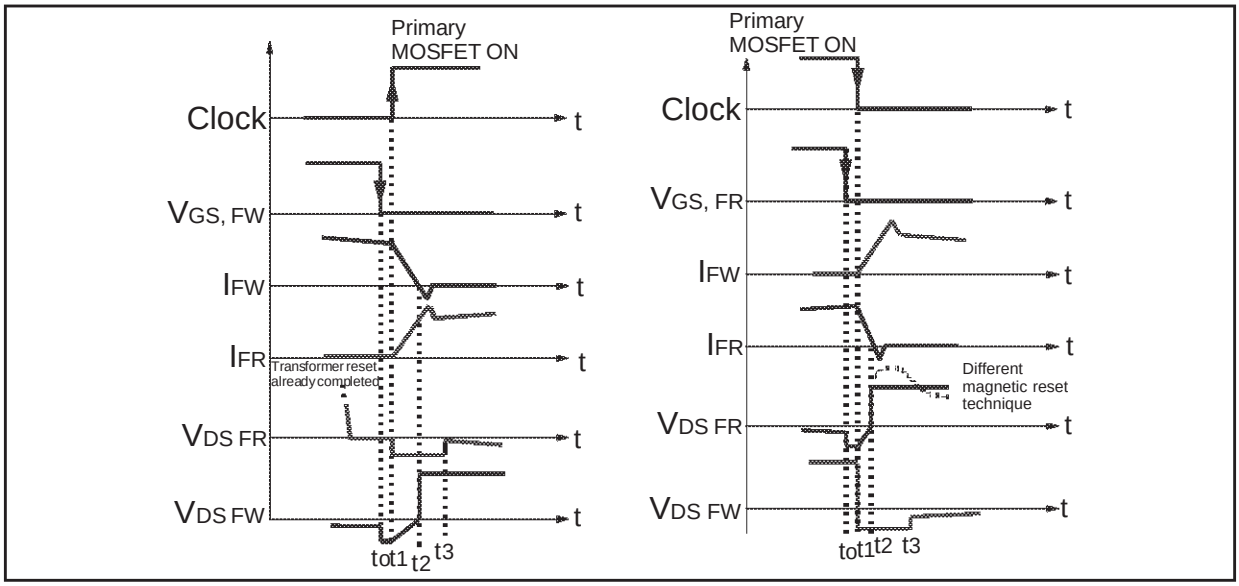
Figure 4: Shoot-Through Condition



Referring to figure 3, when the primary MOSFET (4) is turned-on, the voltage on node (8) tends to go positive. This voltage forward biases the body diode of the FR (2) and, due to the delay in turning-off the FW (1), an unlimited current can flow in the short circuit loop determined by the FW (1), the body-diode of the FR(2) and the secondary winding of the isolation transformer. The value of the short circuit current is only limited by the parasitic of the circuit and eventually by the primary side protection circuits included in the PWM (figure 4). In the other transition, when the MOSFET (4) is turned-off, the voltage on node (8) becomes negative. If the SR (2) is still on due to the delay of the Clock input information, this negative voltage forward biases the body-diode of the SR (1), and a short circuit loop is formed by the body-diode of the SR (1), the SR (2) (still on) and the secondary winding of the isolation transformer (5).

In order to avoid this bad condition, an anticipation in turning off the FW and the FR MOSFETs is needed. The detailed timing for a correct operation of the circuit, according to the concept of anticipation is shown in figure 5. In both of the two SR turn-off transistions for the free-wheeling FW (1) (FW) and the FR (2) (FR), the time interval t_0-t_1 is the amount of anticipation, while t_0-t_3 is the entire dead time between the two complementary driving signals. In the interval t_0-t_2 the body-diode conducts, reversing after t_2.

Figure 5: FW Turn-Off Transition and Anticipation Time in Forward Topology



4b. Flyback Topology

We will now examine the operations in a Flyback topology circuit, displayed in figure 6. Most of the considerations made for the forward topology are still valid, but, in this case, the topology shows only one MOSFET working as a rectifier.

The SR(1) has to be turned-on when the main primary switch (4) is off and viceversa. When the MOSFET (4) is turned on the voltage at the output of the isolation transformer, referenced to node (2), goes from Vo to -Vin, and if the SR(1) is not already off, a short circuit loop is generated with the output capacitor (3) put in parallel to a negative voltage that tries to impulsively discharge the capacitor with an unlimited current. This causes an unavoidable serious drop in the regulated output voltage. Even in this case, an anticipation in turning-off the SR solves the problem. (figure 7)

Figure 6: Control Driven Synchronous Rectification in Flyback Topology

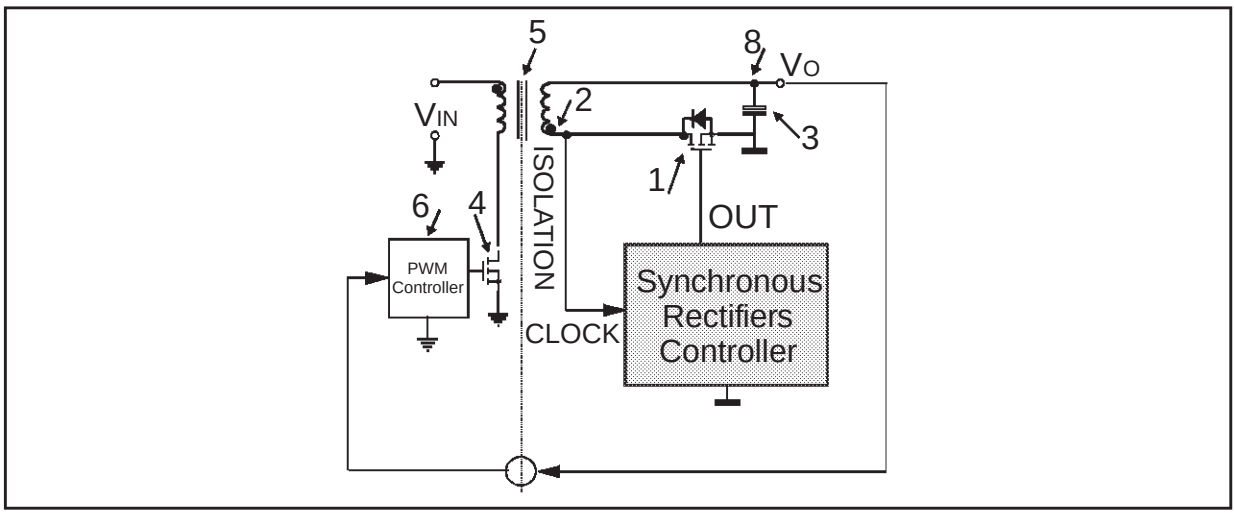


Figure 7: SR. Turn-Off Transition and Anticipation Time in Flyback Topology

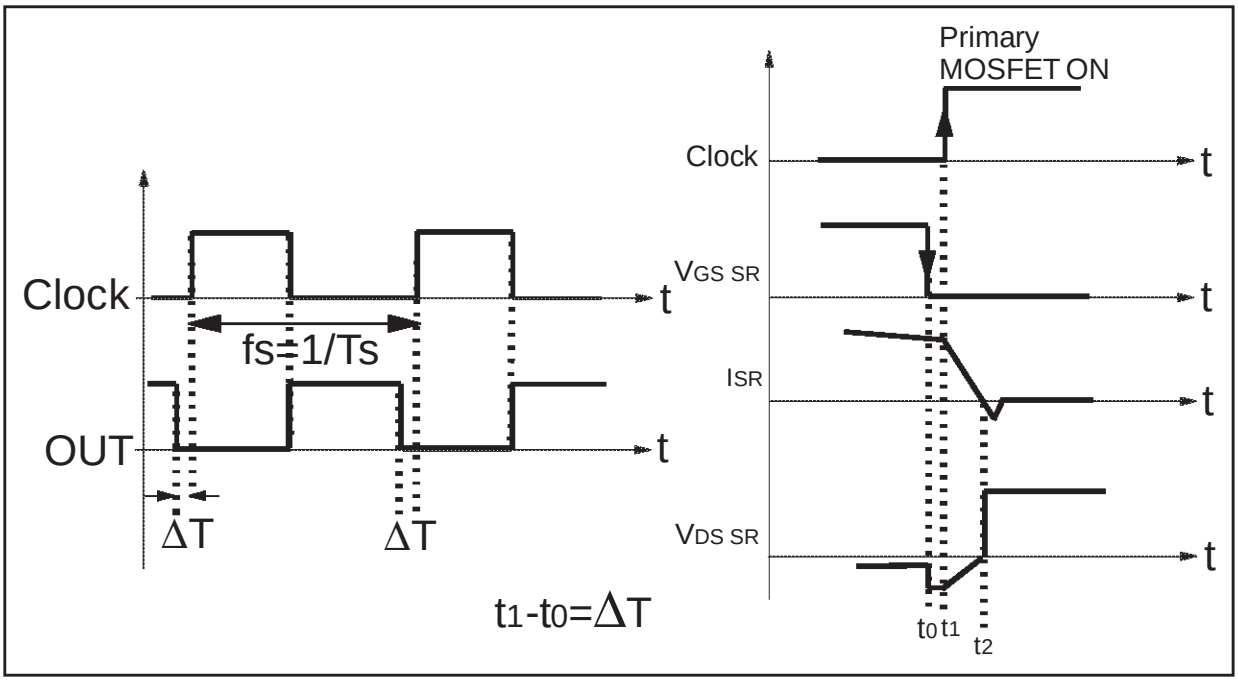
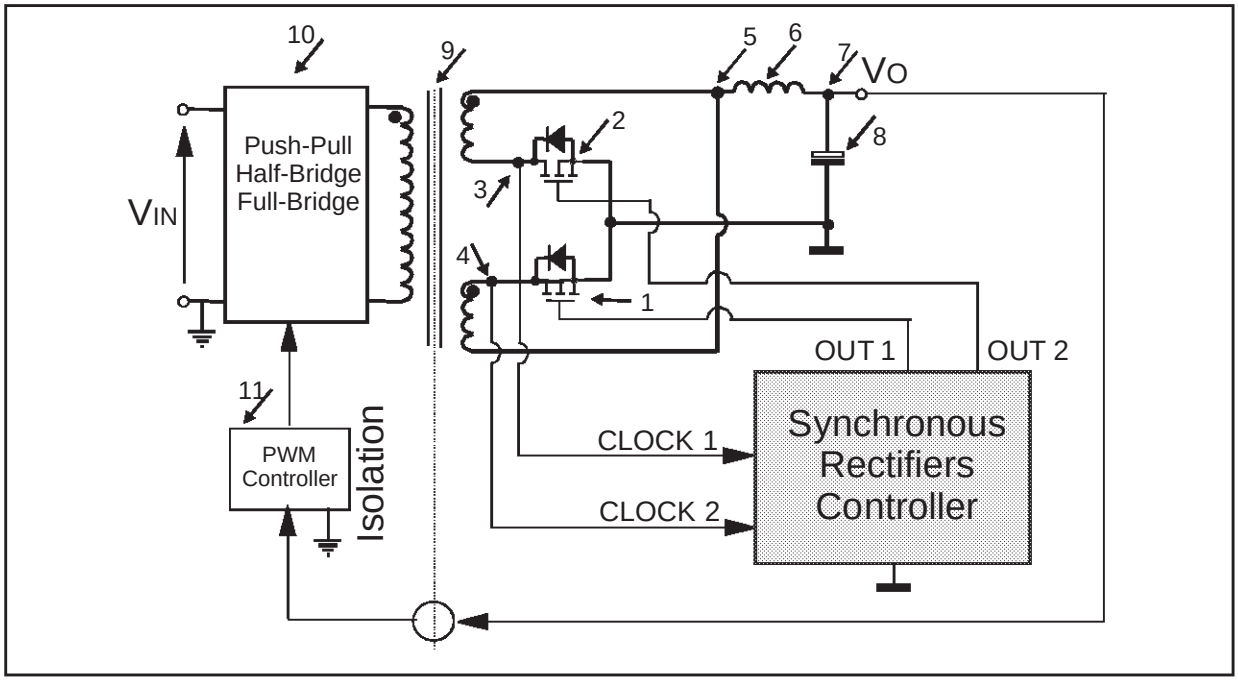


Figure 8: Control Driven Synchronous Rectification in Double-Ended Topologies



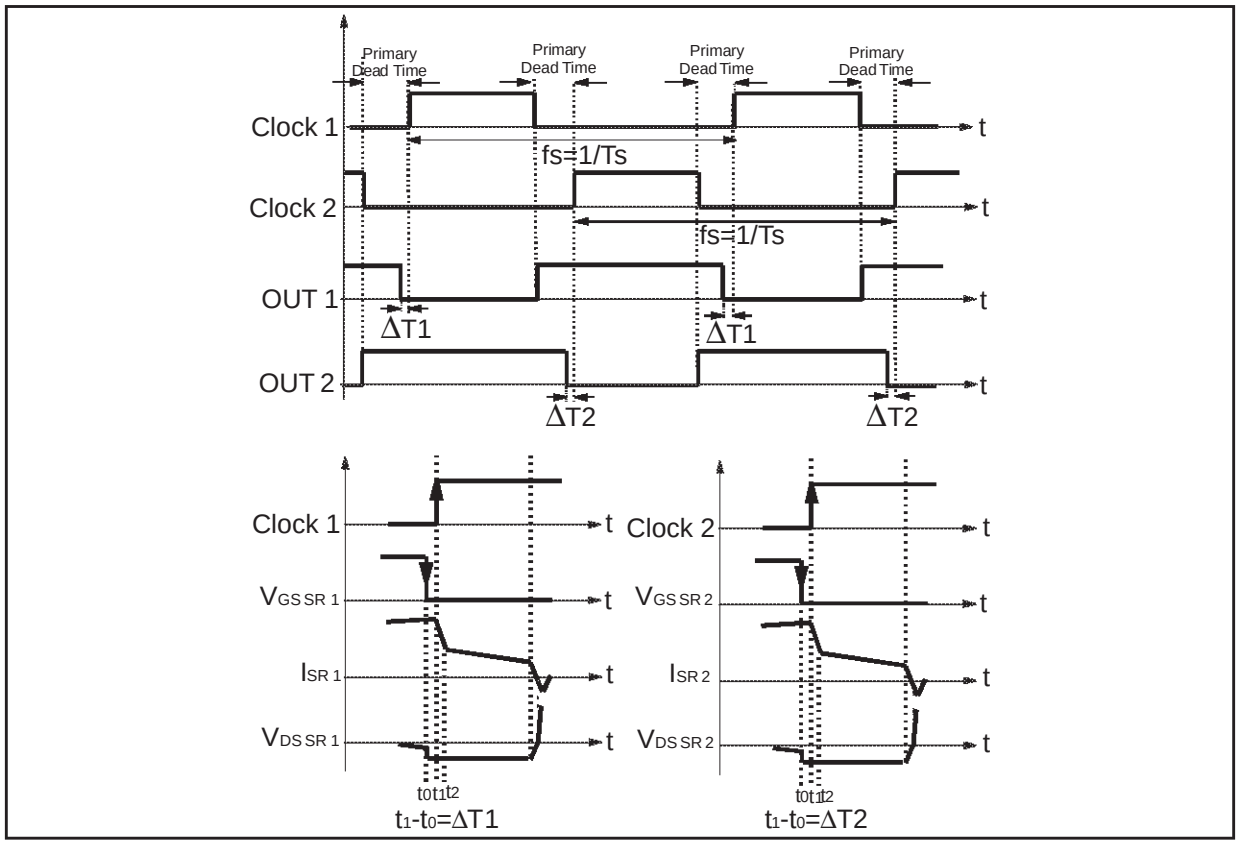
4c. Double-Ended Topologies

Similar consideration are valid for all the forward derived double ended isolated topologies (push-pull, half bridge, full bridge), displayed in figure 8. The synchronization clock input withdrawn at node (3) is used by the SR control circuit to generate the proper timing signal for the SR(2). In a similar way, the synchronization clock input withdrawn at node (4) is used to generate the proper timing signal for the

SR(1). In both cases the synchronization clock and the relative output driving signal are displayed in figure 9. In this case, the anticipation times in turning-off the MOSFETs are necessary to avoid short circuit loops formed in both transitions by the two SRs (one SR and one body-diode) and the secondary winding of the isolation transformer, with a worsening of the converter efficiency.

The detailed timing of the SRs turn-off transitions (two identical) relative to the forward double-ended topologies circuit is showed in figure 9.

Figure 9: Synchronous Rectifiers Turn-Off Transition and Anticipation Time in Double Ended Topologies



5. DESCRIPTION OF THE DIGITAL METHOD TO GENERATE THE SRs DRIVING SIGNALS.

The proposed method is meant to generate the proper driving signals for Synchronous Rectifiers from a Clock signal input, related to the main PWM signal of the switch-mode circuit.

In particular, it is able to operate according to the timing displayed in figure 2, realizing proper anticipation times in correspondence of the turning-off transitions of the outputs.

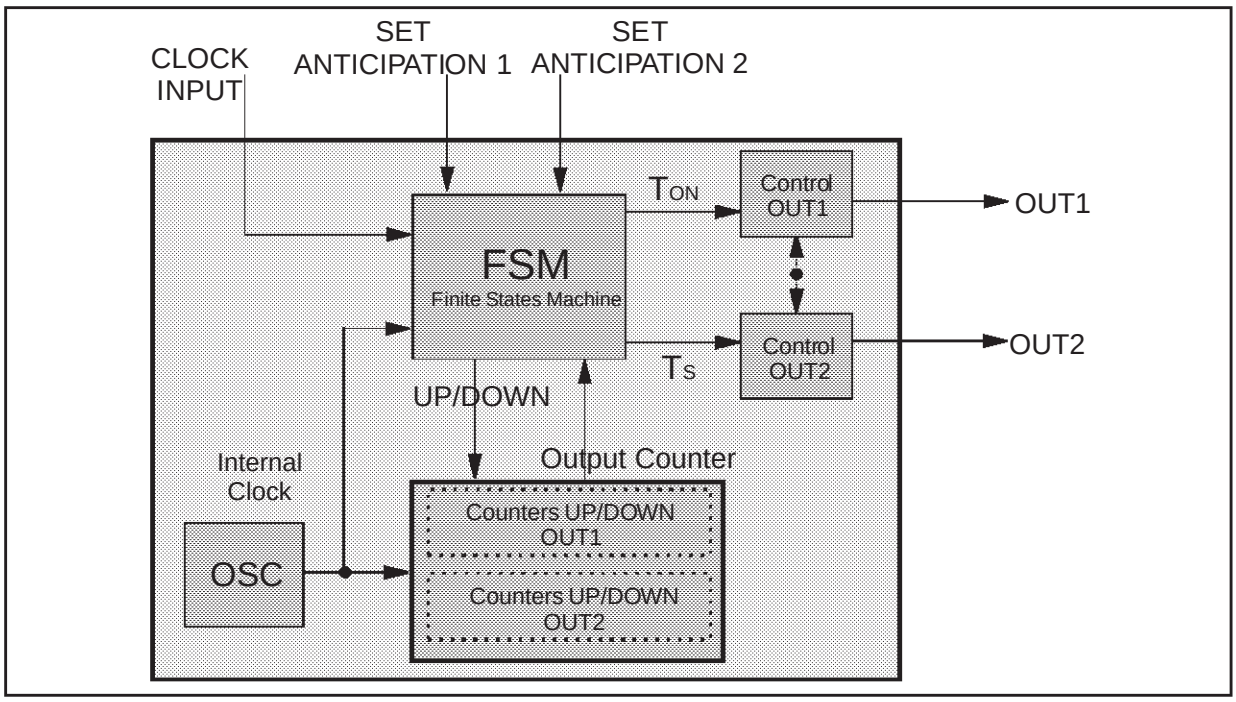
These functions are implemented through the basic concept of synchronizing the operation of the control circuit to the clock signal at the converter switching frequency, and, in particular, to its transitions. This is realized by means of an oscillator at a frequency much higher than the switching frequency of the

converter (f_S) and of two digital counters blocks which play different roles: one operates the measure of the entire switching period, cycle-by-cycle, storing this information for the next cycle. The other one makes the same revelation for the On or Off time of the clock signal, according to the specific need of the circuit topology. The precision and resolution of the system is related to the internal digital frequency of operation, used to implement this method. Being available the period and On/Off time intervals parameters of the previous cycle, a proper timing of the outputs can be easily generated in the following cycle, and in particular a proper anticipation on the turning-off transitions can be set. The amount of the anticipation can be set accordingly with the resolution of the system, in terms of discrete quantities of minimum digital pulse period.

Timing of the proposed control technique will be shown in the following, together with the detailed explanation of the control method operation, according to the description of the apparatus through which it is implemented.

In the more general case of two complementary signals on the secondary side, the general structure of the system is composed by an internal oscillator, a finite states machine, two couple of UP/DOWN Counters, two control output logic blocks (figure 10). This system structure has three inputs and two outputs: the outputs are the driving signals for the two MOSFETs on the secondary side of the converter; the inputs are the clock (CK), the anticipation time setting for the OUT1 and the anticipation time setting for the OUT2.

Figure 10: General Structure of the System



The *finite states machine*, synchronized with the rising edges of the internal oscillator clock signal (CKI) at frequency *fI>fS* (period *TI*), is the *brain* of the system and generates the two signals OUT1 and OUT2

without any overlap in turn-on and turn-off conditions. A square wave signal of frequency *fS* (period *TS*), said switching frequency is present at the clock input; the anticipation times are externally set through the relative inputs. The two counters work in a different way, DOWN to anticipate the turn-off of the outputs and UP in order to continuously get the information about the duration of the switching period for the OUT2 or the duration of the TON time for the OUT1. In this way, the output anticipation in a switching period in turn-off is based on the information stored in the previous switching period. A continuous monitoring of the switching period and of the TON time is obtained cycle by cycle. The bit number of the counters relative to the OUT2 are chosen according to the minimum and the maximum operating switching frequency of the converter. The bit numbers of the counters relative to the OUT1 are chosen according to the minimum and the maximum *TON* of the converter.

5a. Steady Conditions

In steady state conditions (fixed switching frequency and fixed duty-cycle), for the two following switching period, the part of the system relative to the OUT2 operates as follow (figure 11):

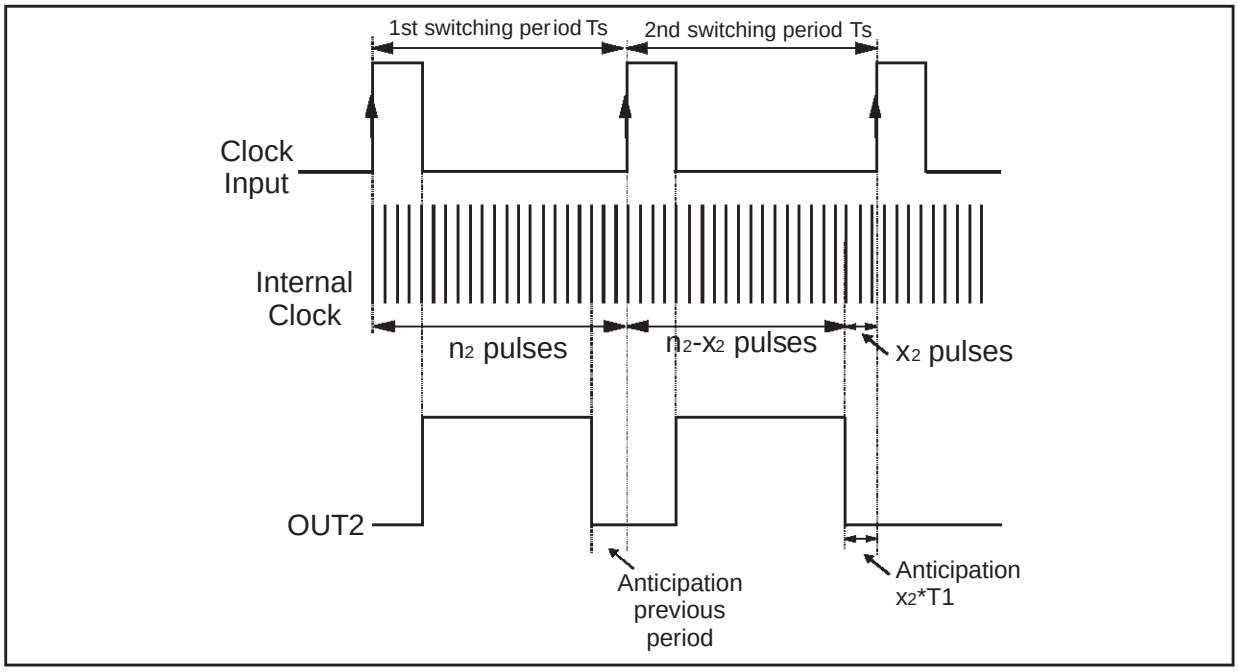
- First switching period:

On the rising edge of the clock input, the first of the two UP/DOWN counters starts to count UP the pulses of the internal clock (CKI). On the next rising edge of the clock input (end of the first period *TS*) the counter stops its calculation. The number of pulses counted (*n2*) takes account of the duration of the switching period. This information is stored in order to be used in the next switching period.

- Second switching period:

On the rising edge of the CK input, the first counter counts DOWN the pulses of the internal clock stopping its calculation to *n2-x2*, at this time the OUT2 is turned off. The second counter, counting the new number of pulses of the internal clock, updates the information about the duration of the switching period *TS*. The amount of anticipation in turning-off the OUT2 is given by $x2 \cdot TI$, and is set by the OUT2 anticipation time input. In each period the function of the counters, UP or DOWN, is exchanged with respect to the previous period.

Figure 11: OUT2 Anticipation Time Generation

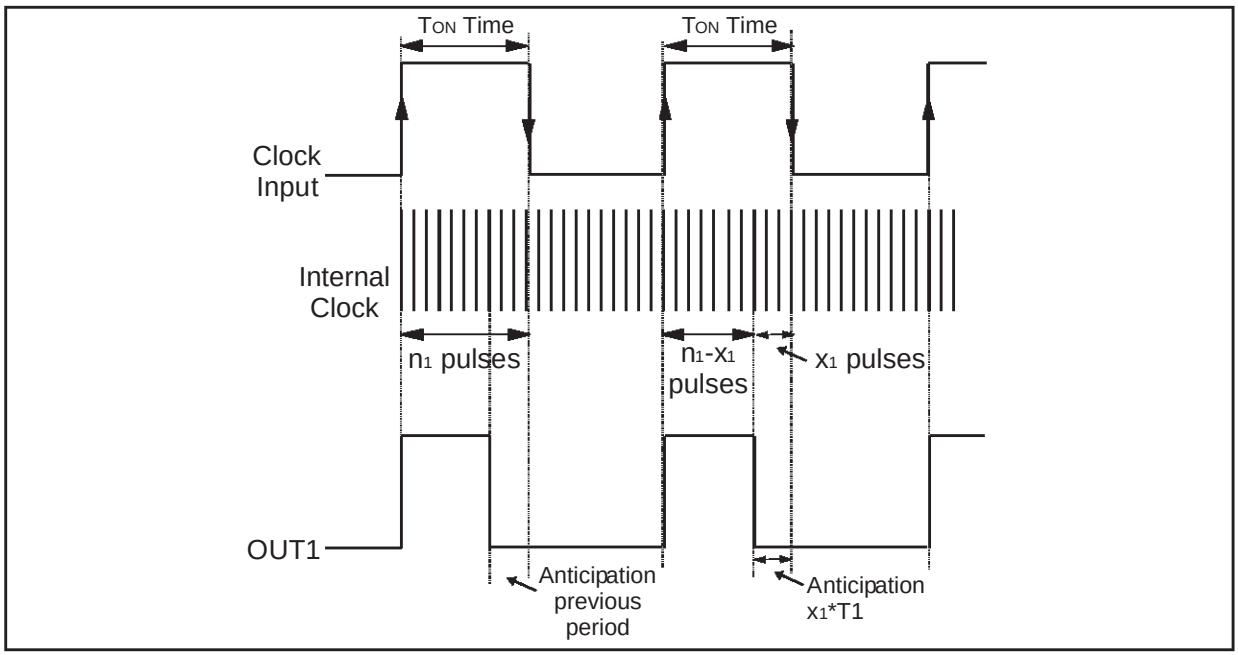


For the part of the system relative to the OUT1 the other two UP/DOWN counters take in account the information about the duration of the TON time in order to anticipate the turn-off of the OUT1 (figure 12):

- First switching period:

The first counter starts to count on the rising edge of the clock input and stops its calculation on the falling edge. The number of pulses counted are *n1* and this information takes in account of the *TON* time.

Figure 12: OUT1 Anticipation Time Generation



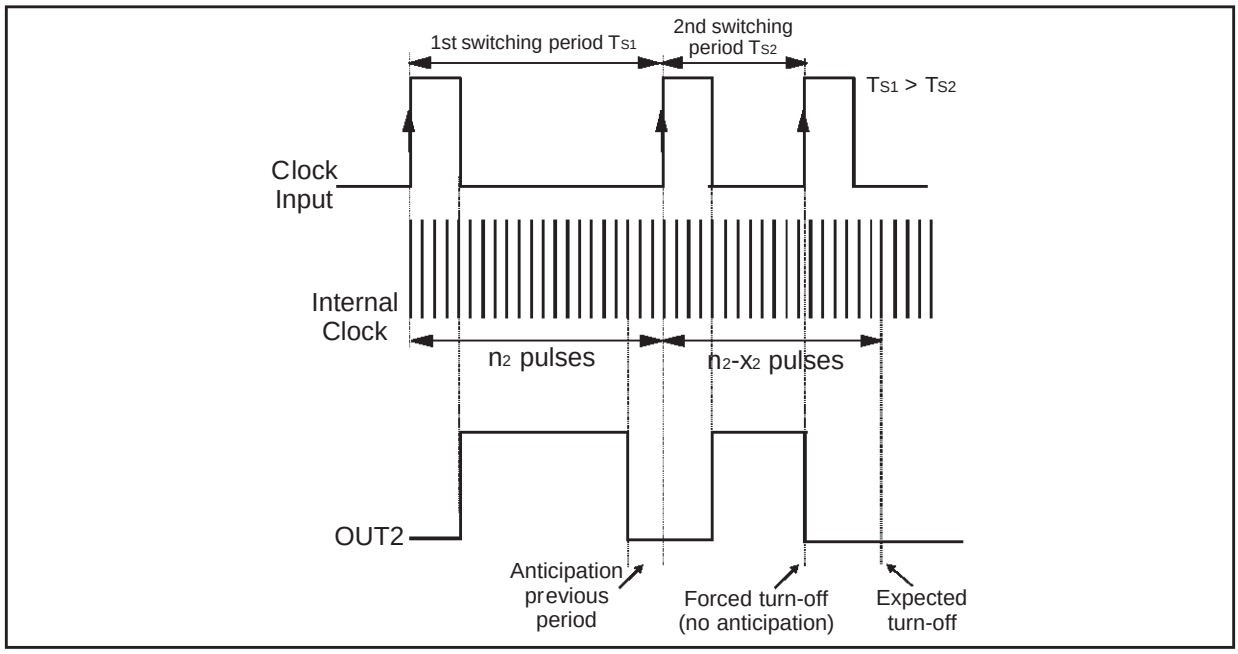
- Second switching period:
The first counter counts DOWN stopping its calculation to *n1-x1* giving an anticipation in turning-off the OUT1 equal to *x1·TI*, this anticipation is set through the OUT1 anticipation time input. The second counter counts upward the number of pulses of the internal clock between the rising edge and the falling edge of the clock input during the current period.

5b. Varying Conditions
For the OUT2, when a variation in the switching frequency occurs, three different cases are possible:

1. The switching period in which the anticipation is realized is smaller than the previous period (figure 13). In this case the turning-off of the OUT2 would be delayed and not anticipated with respect to the clock input. This condition is avoided forcing, in any case, the turn-off of the OUT2 with the rising edge of the clock input.

2. The switching period in which the anticipation is realized is larger than the previous period (figure 14). In this case an early turn-off of the OUT2 happens. The conduction time of the body-diode of the MOSFET is not minimized just for one cycle and the loss of efficiency is very low.

Figure 13: Switching Frequency Variation: Ts1 > Ts2



3. The switching period in which the anticipation is realized has a *Ton* time equal or larger than the previous period (figure 15). In this case the OUT2 is kept OFF. Even in this case the conduction time of the body-diode of the MOSFET is not minimized for only one cycle causing a very low loss of efficiency.

Figure 14: Switching frequency variation: Ts1< Ts2

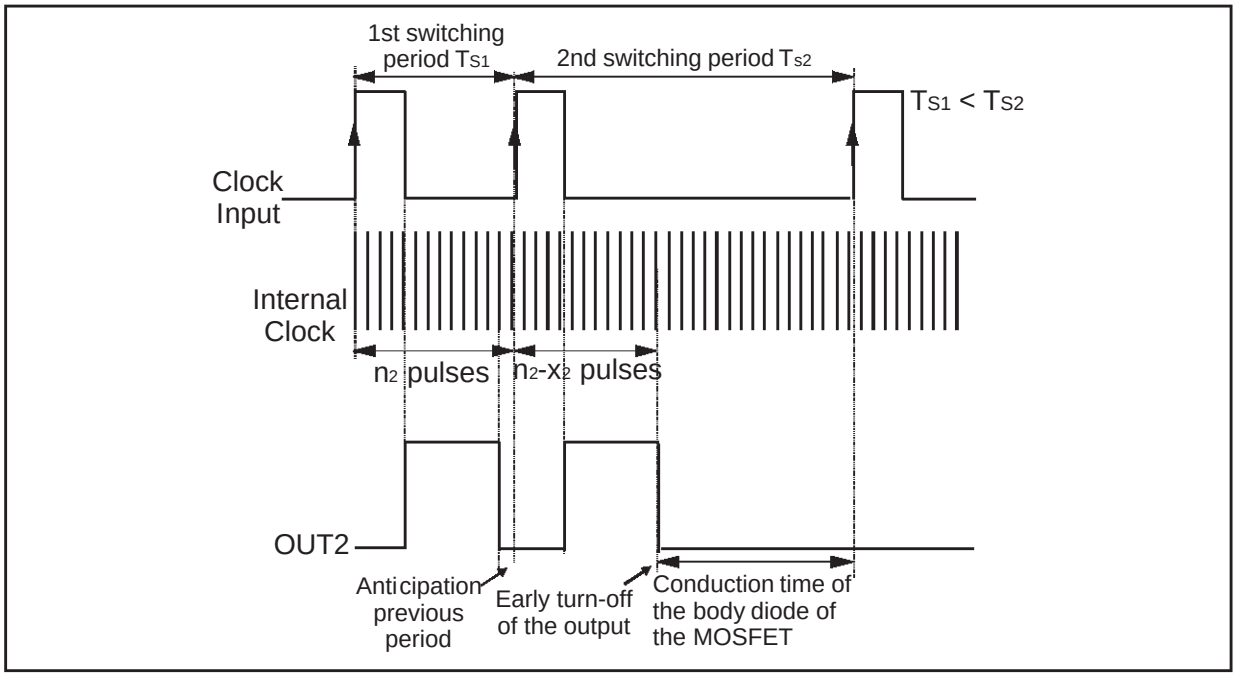
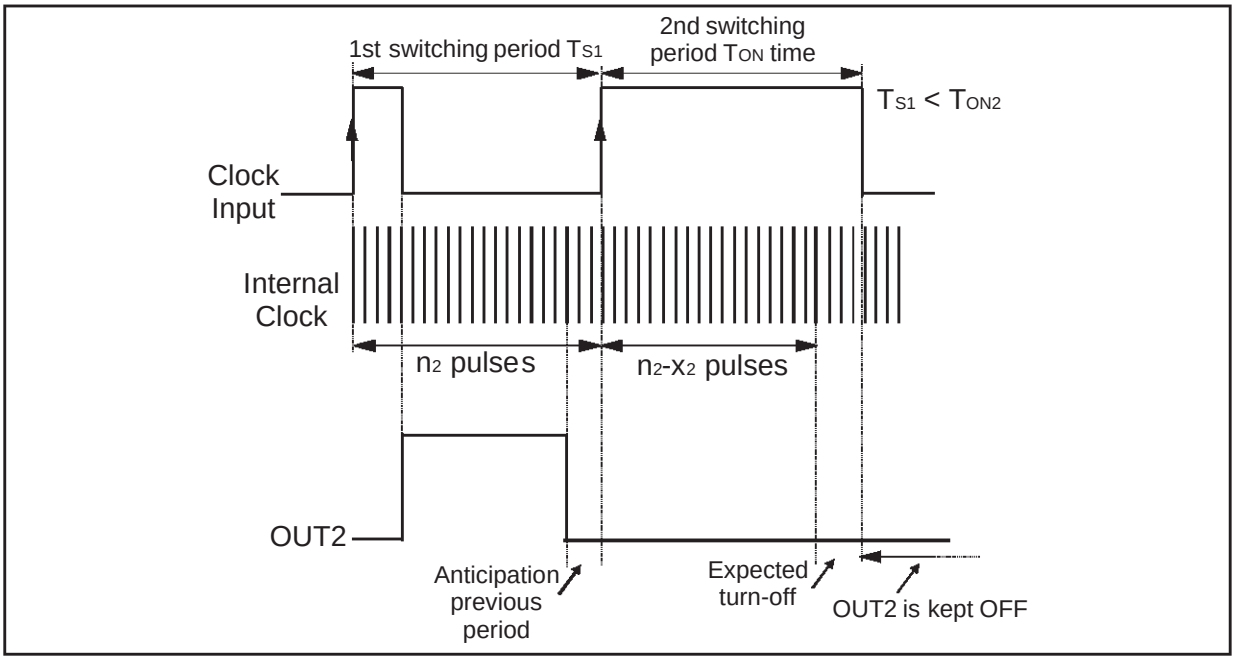


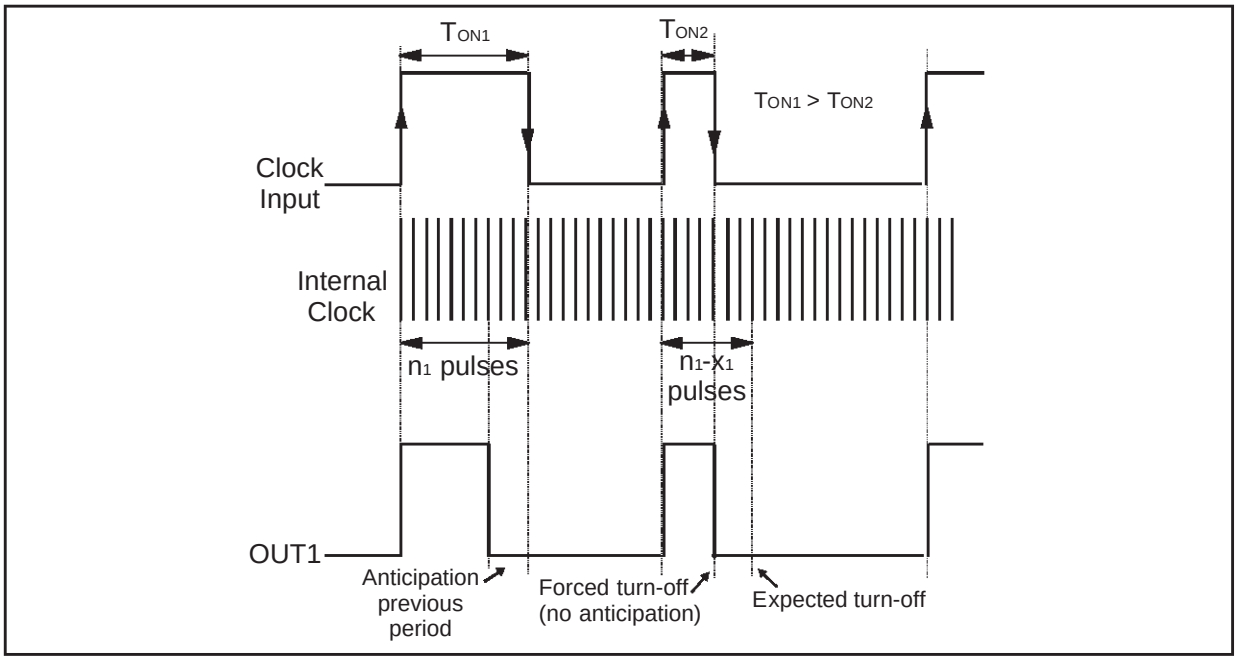
Figure 15: Switching frequency variation: Ts1 <Ton2



For the OUT1, when a variation in the *TON* time occurs two different cases are possible:

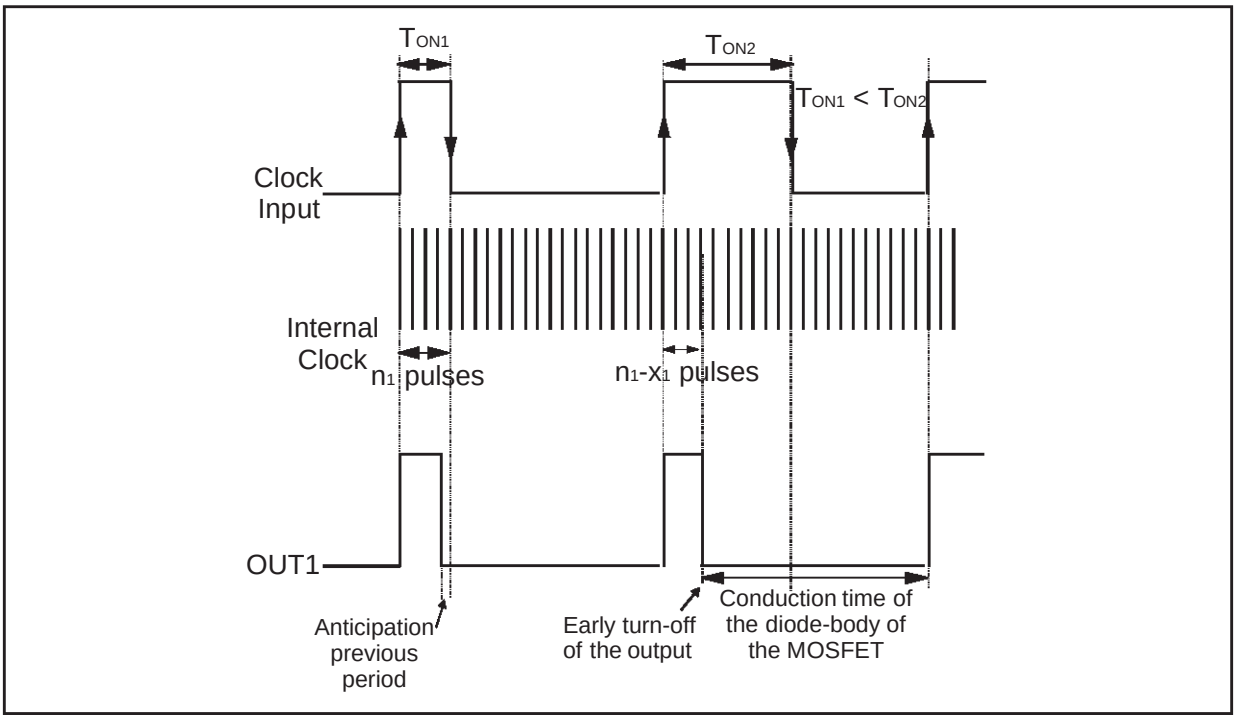
1. The *TON* time in which the anticipation is realized is smaller than the previous *TON* time (figure 16). In this case the turn-off of the OUT1 would be delayed and not anticipated with respect to the clock input. This condition is avoided forcing, in any case, the turn-off of the OUT1 with the falling edge of the clock input.

Figure 16: Duty-cycle variation: Ton1 > Ton2



2. The *TON* time in which the anticipation is realized is larger than the previous *TON* time (figure 17). In this case an early turn-off of the OUT1 happens. The conduction time of the body-diode of the MOSFET is not minimized just for one cycle and the loss of efficiency is very low.

Figure 17: Duty-cycle variation: Ton1 < Ton2



The described method implements a cycle-by-cycle control because the measurement taken in a period determines the action in the next period. By setting the value of *x1* (*x2*) the amount of anticipation in turning-off the synchronous rectifier MOSFET is chosen among different discrete values. The time step is *TI*, so the higher the internal oscillator frequency *fI* is the more accurate the anticipation time is.

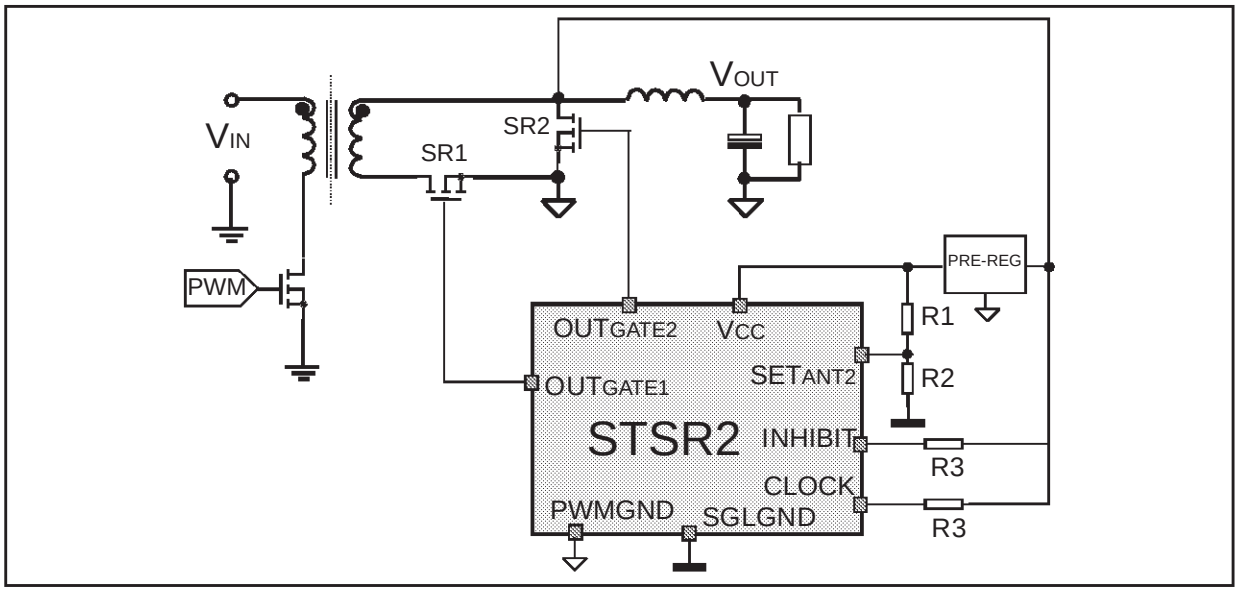
6. IMPLEMENTATION OF THE CONTROL METHOD IN THE STSRx FAMILY

The method of controlling the turn-off time of Synchronous Rectifiers is implemented in a silicon device family:

6a. STSR2

The STSR2 is the device designed to drive two Synchronous Rectifiers in Single Ended Forward Topology applications. The IC includes the described control system, two high-current N-Channel MOSFET drivers and a clock buffer circuit needed to adapt the clock signal to the accepted values, with the following pin output (figure 18):

Figure 18. STSR2 in Forward Converter



VCC: The supply input is from 4.5V to 5.5V which allows applications with logic MOSFETs. The UVLO feature proper start-up is guaranteed while it avoids undesirable driving during eventual dropping of the supply voltage.

PWRGND: Reference for power signals. This pin carries the full peak currents from the outputs.

SGLGND: Reference for all the control logic signals. This pin is completely separate from the PWRGND to prevent eventual disturbances that could affect the control logic.

CK: This input provides synchronization for IC operations, being the transitions between the two output conditions based on a positive threshold, equal for the two slopes. The smart clock revelation mechanism makes these operations independent by false triggering pulses generated in light load conditions and by particular demagnetization techniques.

OUTGATE1,2: The two high current outputs are complementary without any overlap between the

On-times due to the self generation of dead times of the IC.

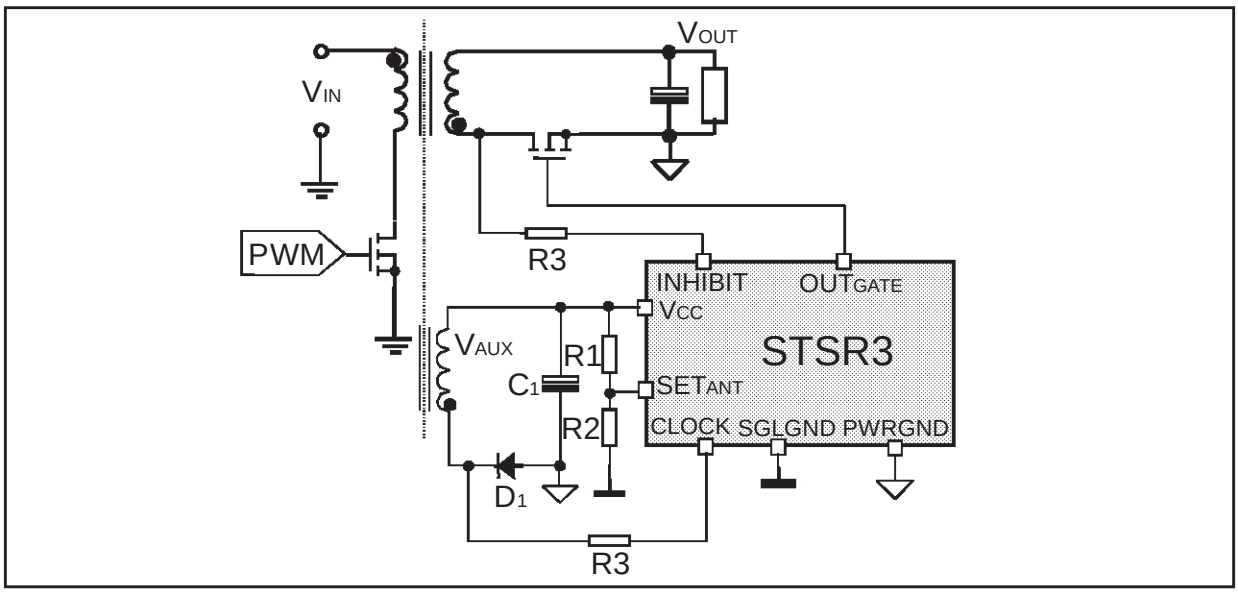
SETANT2: Sets the anticipation in turning-off the OUTGATE2. It is possible to choose among four different anticipation times by discrete partitioning of the supply voltage

INHIBIT: This input enables OUTGATE2 when kept to a negative value larger than the very low threshold voltage. Otherwise it forces the OUTGATE2 to a minimum conduction time. In typical forward converter applications it is possible to turn off the freewheeling synchronous rectifier when the current through it tends to reverse. This allows discontinuous conduction modes and providing protection to the converter from eventual sinking current from the load.

6b. STSR3

The STSR3 is the device designed to drive one Synchronous Rectifier in Flyback Topology applications. The IC includes the described control system, with the same logic operation, but only for the art relative to OUT2, one high-current N-Channel MOSFET driver and a clock buffer circuit needed to dapt the clock signal to the accepted values. The pin output is the same of the STSR2 one, but with only one OUTGATE (figure 19).

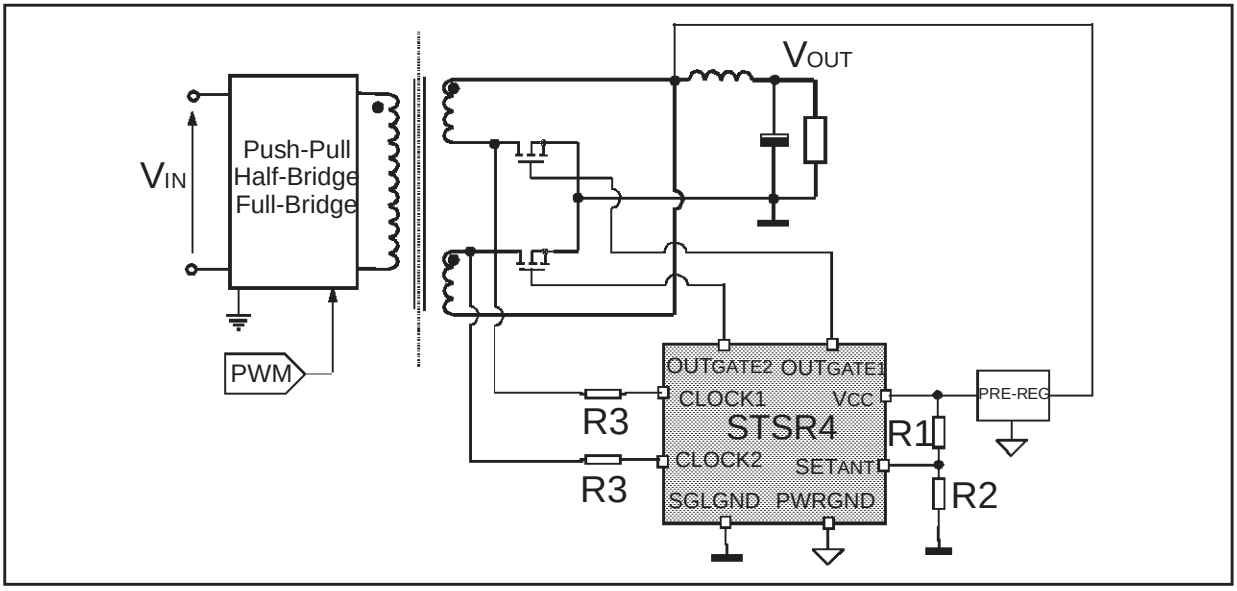
Figure 19: STSR3 in Flyback Converter



6c. STSR4

The STSR4 is the device designed to drive two Synchronous Rectifiers in Double-Ended Topology applications (Push Pull, Half Bridge, Full Bridge). The device includes a dual structure based on the duplication of the described control systems for the part relative to OUT2, two high-current N-Channel MOSFET drivers and two clock buffer circuits are needed to adapt the clock signal to the accepted values. The function of the pins is the same of STSR2 and the application circuit is displayed in figure 20.

Figure 20: STSR4 in Generic Double-Ended Converter



7. CONCLUSION

The technique here disclosed is meant to realize a control-driven approach for synchronous rectification in SMPS isolated topologies. The control-driven technique presents several advantages with respect to the self-driven approach. It realizes independence from the isolation transformer reset technique, being the conduction time of the body-diode of the minimized MOSFETs, while the driving signal values can always be made compatible with the gates ranges. Using some additional particular techniques, it is also possible to allow the discontinuous conduction mode operation of the converter.

The technique allows the convenience to use the PWM Controller on the primary side of the isolated topology, deriving synchronization information directly from the secondary side.

The method solves any of the known operation problems regarding the generation of Synchronous Rectifiers driving signals, like cross-conduction and shoot-through, while it allows the minimization of the body-diode conduction.

With respect to other techniques, which implement the same control driven approach, and also able to solve all the mentioned problems, the proposed method and the related implementing apparatus show several advantages and benefits.

In particular the proposed digital technique allows the implementation of a very simple circuit configuration required by the STSRX device to operate correctly when inserted in a SMPS topology circuit. The IC can be realized with a very minimal pin count. No particular accuracy or stability in time and temperature is required for the eventual external components, resistors, to be used to set the anticipation times.

In addition the method shows excellent characteristics in term of fast response to transients coming from the converter switching frequency and sudden duty-cycle variations.

All the other techniques, based on the analog approach to realize the turn-off transitions anticipation function, show weakness due to the need of several external components, mainly capacitors with very tight tolerance and stability. These are needed to allow the correct operation of the relative technique and apparatus.

Other techniques based on the PLL approach to realize the turn-off transitions anticipation function require a huge number of external components, with relative high pin count in the synthesizing device, to set all the parameters that are necessary to the proper operation of the control method, by means of complex design relations. In addition they show very slow response to transients, due to switching frequency and duty-cycle perturbations, which reflects negatively on the overall efficiency of the converter.

The described method is fast because the control is made cycle-by-cycle. Therefore it acts suddenly on the next cycle after a disturbance of the steady state occurs. In addition, due to the high flexibility of the digital approach, eventual correctional algorithms can be easily implemented in the switching frequency synchronization, generating error-correction procedures and similar improvements of the presented approach.

Due to the digital nature of the method, the anticipation time can be set only by discrete steps. However, by increasing the digital oscillator frequency the time step can be reduced and a more precise resolution can be achieved with a more flexible determination of switching timing.

REFERENCES

1. Franco Lentini, Fabrizio Librizzi, Pietro Scalia, Ignazio Calá – Method and apparatus to digitally control turn-off time of synchronous rectifiers in isolated topologies for switched mode power supplies – European Patent pending #00830274.7.
2. STSR2 Target Specification
3. STSR3 Target Specification
4. D. Jitaru - “High Efficiency DC/DC Converter” - HFPC Proceedings, April 1994
5. M. M. Jovanovic, M. T. Zhang, F. C. Lee - “Evaluation of Synchronous-Rectification Efficiency Improvement Limits in Forward Converter” - IEEE Transaction on Industrial Electronics, Vol. 42, No.4, August 1995
6. H. P. Yee, S. Sawahata - “A Balanced Review of Synchronous Rectifiers in DC/DC Converters” - PESC 1999