XR-9201

8-Bit Microprocessor Compatible Digital-To-Analog Converter

GENERAL DESCRIPTION

The XR-9201 is a monolithic 8-Bit μP compatible digital-to-analog converter with differential current outputs. It contains an internal data latch, making it suitable for interfacing with microprocessors. The chip contains a stable voltage reference (2.0 V Nominal) which is externally adjustable and can be used as a reference for other D/A and A/D converters.

The XR-9201 features non-linearity of ± ½ LSB maximum (±.19% of full scale current). The internal voltage reference maintains a temperature coefficient of 50 ppm/°C.

FEATURES

8-Bit Resolution	
Input Data Latches	
Internal Voltage Reference	
Microprocessor Compatible	
Non Linearity	± ½ LSB Maximum
Full Scale Current Stability	±50 ppm/°C
Reference Voltage Stability	±50 ppm/°C
Differential Current Outputs	
TTL Compatible	

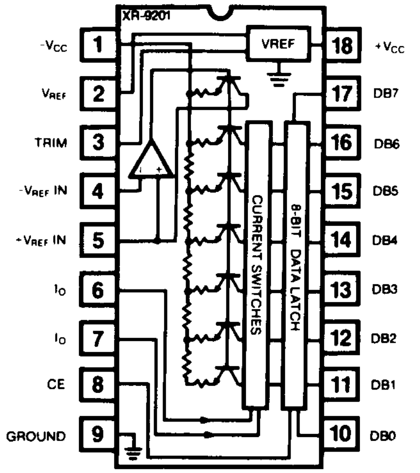
APPLICATIONS

Bipolar and Unipolar D/A Conversion
A/D Conversion
Test Equipment
Measuring Instruments
Programmable Current Source
Programmable Voltage Source

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ Positive Supply Voltage	+6V
$-V_{CC}$ Negative Supply Voltage	−8.5V
Logic Input Voltages	0 to +6V
Power Dissipation	500 mW
Derate Above 25°C	5 mW/°C
Storage Temperature	−55°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-9201 CP	Plastic	0° to +70°C

SYSTEM DESCRIPTION

To convert the output currents of the digital-to-analog converter to a voltage, an operational amplifier can be used as shown in Figure 12.

Care must be taken in selecting an operational amplifier to be used in D/A conversion. For accurate conversion, the operational amplifier should have low input offset voltage, low input bias and offset currents, and fast settling times. Input offset voltage contributes a DC error on the output and should be properly nulled. Input bias current contributes to the D/A converter current flowing through the feedback resistor, R_{FB}, and also causes a DC error on the output voltage. This error can be reduced by the addition of a resistor equal in value to R_{FB} from the noninverting input to ground. Settling time is important because it rules how fast the output reaches its prescribed voltage level. The OP-01 is suitable for D/A converter applications producing negligible errors.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = +5V, $-V_{CC}$ = −7V, T_A = 25°C, I_{REF} = 1.0 mA, unless otherwise specified.

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
	Resolution	8	8	8	Bits	
	Monotonicity	8	8	8	Bits	
	Non-linearity			±0.5 ±0.19	LSB %I_{FS}	
$+V_{CC}$	Positive Supply Voltage	4.5	5.0	5.5	V	
$-V_{CC}$	Negative Supply Voltage	−7.7	−7.0	−6.3	V	
V_{IH}	Data Input and Chip Enable "High" Voltage	2.0			V	
V_{IL}	Data Input and Chip Enable "Low" Voltage			0.8	V	
I_{IH}	Data Input and Chip Enable "High" Current			500	μA	
I_{IL}	Data Input and Chip Enable "Low" Current			±20	μA	
I_{FS}	Full Scale Output Current	1.914	1.992	2.070	mA	I_{REF} = 1.000 mA
I_{ZO}	Zero Scale Output Current			±10	μA	
TC_{IFS}	Full Scale Current Temperature Sensitivity		±50		ppm/°C	0°C ≤ T_A ≤ 75°C
I_{FSS}	Full Scale Symmetry			±10	μA	
V_{REF}	Internal Reference Voltage	2.005	2.000	1.990	V	R_{ADJ} = 50 KΩ R_{ADJ} = 0 Ω R_{ADJ} = 6 Ω
TC_{REF}	V_{REF} Temperature Stability		±50		ppm/°C	V_{REF} = 2.00 V
$+I_{CC}$	Positive Supply Current		15	25	mA	
$-I_{CC}$	Negative Supply Current	−25	−15		mA	
	Positive Output Voltage Compliance		+5.0		V	
	Negative Output Voltage Compliance		−1.0		V	
	Maximum Full Scale Current		3		mA	
t_S	Settling Time		600		nsec	
t_{SU}	Data Set-up Time		170		nsec	
t_H	Data Hold Time		40		nsec	
t_W	Minimum Chip Enable (CE) Pulse Width		170		nsec	
t_D	Propagation Delay Time		500		nsec	

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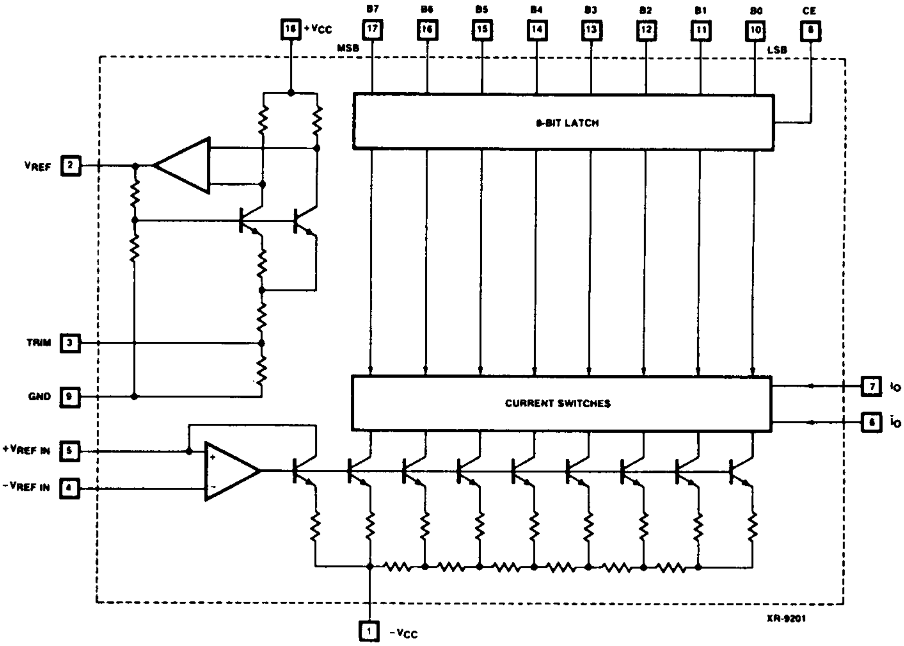

Figure 2. Functional Block Diagram

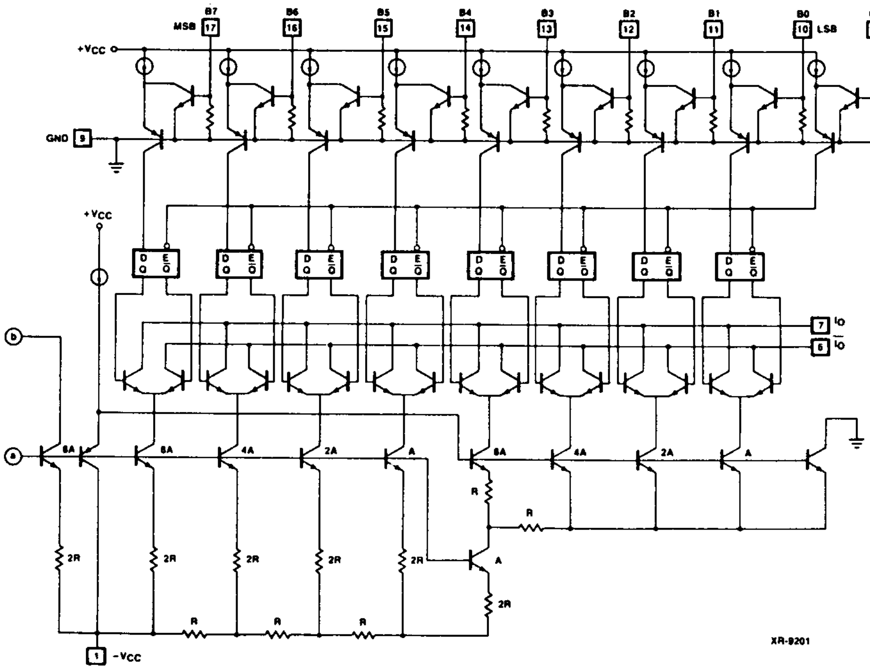

Figure 3A. Equivalent Circuit of Data Latches and Current Switches

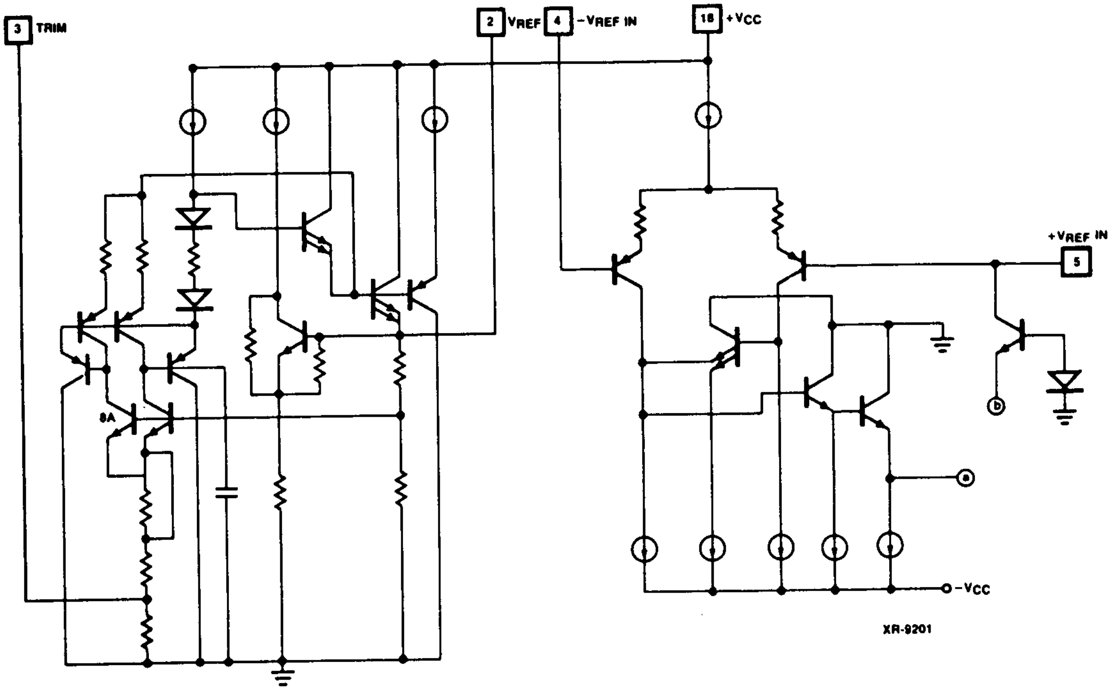

Figure 3B. Equivalent Circuit of Voltage Reference and Input Amplifier

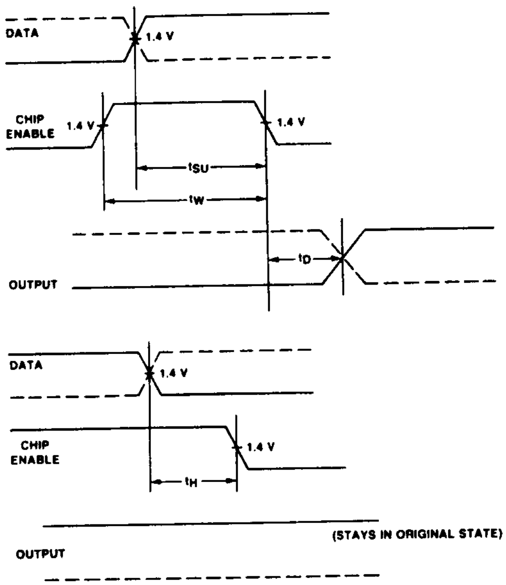

Figure 4. Timing Diagram

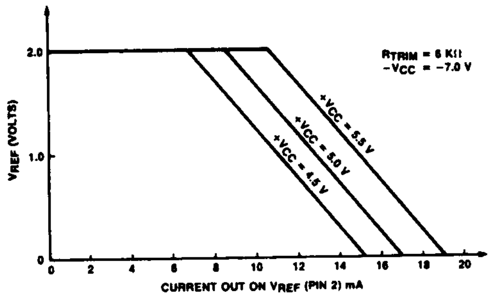

Figure 5. V_{REF} vs. Current Output

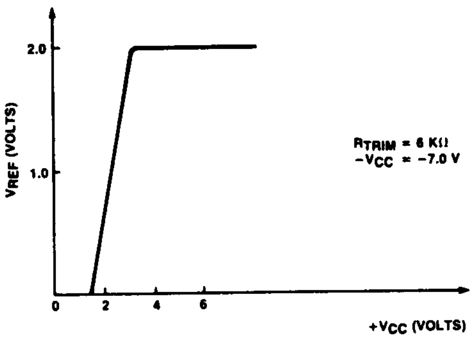

Figure 6. V_{REF} vs. $+V_{CC}$

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DEFINITIONS OF SWITCHING PARAMETERS

Settling Time (t_S): Time required for output to reach its final value (to within ±.19% of full scale output) after data is applied to the inputs. Chip enable, CE, is held "high."

Data Set-Up Time (t_{SU}): Minimum time required for data to be present at the inputs while CE is "high", in order to obtain valid output data. It is measured from when proper data is applied to the inputs to when CE goes "low".

Data Hole Time (t_h): Maximum time required for data to be present at the inputs before CE goes "low", in order to obtain valid output data. It is measured from when the input data changes state to when CE goes "low", and still obtain valid output data of the previous input state. Data hold time indicates that the input data does not have to be present during the latter part of the CE high state, and still have valid output data.

Chip Enable Pulse Width (t_W): Minimum pulse width required for chip enable signal in order to obtain valid output data.

Propagation Delay Time (t_d): Time required for output to reach its final value (50%) after CE is applied. It is measured from the falling edge of the CE pulse to 50% of the output pulse under minimum data set-up time conditions.

DESCRIPTION OF PIN CONTROLS

V_{REF} (PIN 2): Internal voltage reference output provides +2.00 V Nominal voltage. Can be used as reference voltage for other circuitry. Maximum output current capability is approximately 9 mA with V^+ = 5.0 V.

TRIM (PIN 3): V_{REF} can be adjusted by connecting a 10 KΩ potentiometer between the trim pin and ground. Temperature stability is optimized for V_{REF} = 2.00 V to 10–50 ppm/°C.

$-V_{REF}$ IN (PIN 4): This pin is tied to ground through a resistor, R, equal in value to that of Pin 5 and V_{REF}.

$+V_{REF}$ IN (PIN 5): Reference voltage is connected to this pin using a resistor, R, to provide the reference current, I_{REF}, for the D/A converter. Either the internal V_{REF} (Pin 2) or an external V_{REF} can be connected to this pin. I_{REF} is approximately equal to V_{REF}/R. Maximum value for I_{REF} is about 1.5 mA before internal saturation occurs.

$\bar{I}_O$ (PIN 6): Complement output current.

I_O (PIN 7): Output current. The sum of $\bar{I}_O$ and I_O is always equal to the full scale output current (I_{FS}).

CE (PIN 8): Chip enable pin controls the input data into the internal data latch. The latch is transparent in the "high" state.

DB0–DB7 (PIN 10–17): Data input pins. DB0 corresponds to the LSB. DB7 corresponds to the MSB.

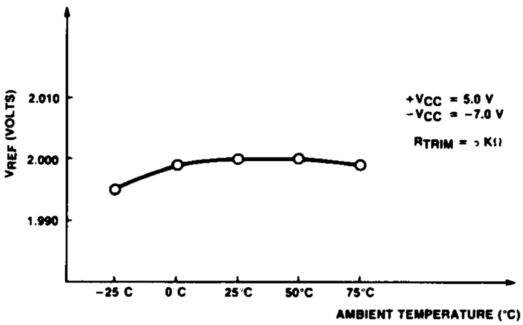


Figure 7. V_{REF} vs. Temperature

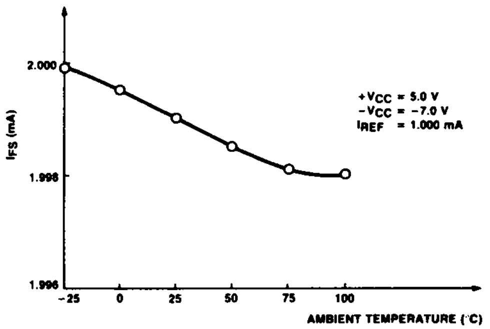


Figure 8. I_{FS} vs. Temperature

PRINCIPLES OF OPERATION

Figure 10 shows the basic configuration of the XR-9201 D/A converter. The input data bits to the chip can be latched (stored) in the D/A by controlling the chip enable (CE) pin. When CE is "high" (>2.0 volts), the latch is transparent and data bits present are passed through the latch and directly control the D/A converter switches. When CE is "low" (<0.8 volts), the data bits within the latch are retained and remain there until CE goes "high" again. When CE is "low", the data bits at the inputs are ignored until CE goes "high". This interval latch provides a useful interface with microprocessors.

The output currents, I_O and $\bar{I}_O$, are related to I_{REF} as follows:

$$I_O = 2\,I_{REF}\left[\frac{b_7}{2}+\frac{b_6}{4}+\frac{b_5}{8}+\frac{b_4}{16}+\frac{b_3}{32}+\frac{b_2}{64}+\frac{b_1}{128}+\frac{b_0}{256}\right]$$

Where: b_n = 1 if Bit N is "High"
= 0 if Bit N is "Low"
b_7 = MSB (Pin 17)
b_0 = LSB (Pin 10)

$\bar{I}_O$ is the complement current output of I_O. For all possible input data combinations,

$$I_O + \bar{I}_O = I_{FS} = \text{full scale output current.}$$

$$\text{where } I_{FS} = 2\,I_{REF}\left(\frac{255}{256}\right)$$

The XR-9201 D/A converter contains an internal reference voltage (V_{REF}) with nominal value of 2.00V using a 6 KΩ resistor to ground. V_{REF} can be adjusted using a 10 KΩ potentiometer tied between Pin 3 and ground. For maximum temperature stability, V_{REF} should be set to 2.00V. The maximum output current capability of V_{REF} is about 9 mA (see Figure 5) and can be used to provide a reference voltage for other DACs, as well as other circuitry.

The reference current (I_{REF}) for the D/A converter is established by a resistor, R, connected between V_{REF} and Pin 5 (+V_{REF} IN), or between an external reference source and Pin 5, and is approximately given as:

$$I_{REF} = \frac{V_{REF}}{R}$$

For $I_{REF} \leq 1$ mA. The maximum I_{REF} allowed is about 1.5 mA beyond which saturation occurs in the internal circuitry. To balance the internal operational amplifier, a resistor equal to R must be placed between Pin 4 (−V_{REF} IN) and ground.

NOTE:
When operating the XR-9201 D/A converter with an operational amplifier, care must be taken with the PC board layout. Specifically, connection between the current output terminals, I_O and $\bar{I}_O$, and the operational amplifier inputs needs to be as short as possible so as to minimize capacitance at the node. Oscillations on the operational amplifier output may result with long wires. A capacitor in the feedback loop of the operational amplifier can reduce these oscillations.

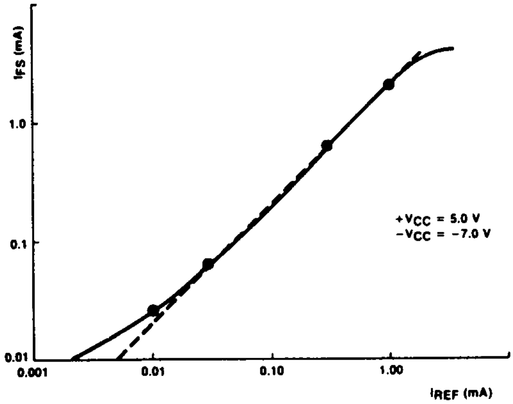


Figure 9. I_{FS} vs. I_{REF}

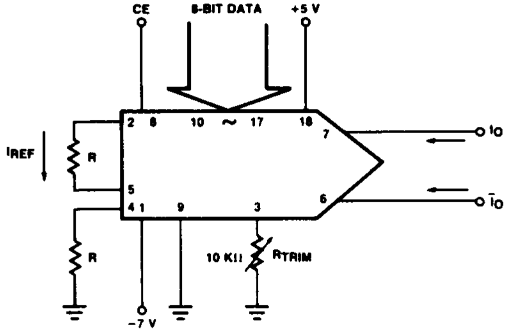


Figure 10. Basic Configuration

ZERO AND FULL SCALE ADJUSTMENTS

Figure 13 shows a circuit for zero and full scale adjustments. It allows the output voltage to be nulled with zero scale input conditions (0000,0000). This is done by shorting out R_{FB} and adjusting the VOS adjust potentiometer of the operational amplifier until the output reads zero volts. This is performed with all digital bits set to zeros. If $\bar{I}_O$ is the output being used, then all digital bits are set to ones and the zero scale is adjusted.

For full scale adjustment, all digital inputs are set to ones and the I_{REF} potentiometer, from Pin 2 to Pin 5, is adjusted until the output is at the desired voltage level (e.g., output is adjusted to 10.000 volts for nominal 9.960 volts output).

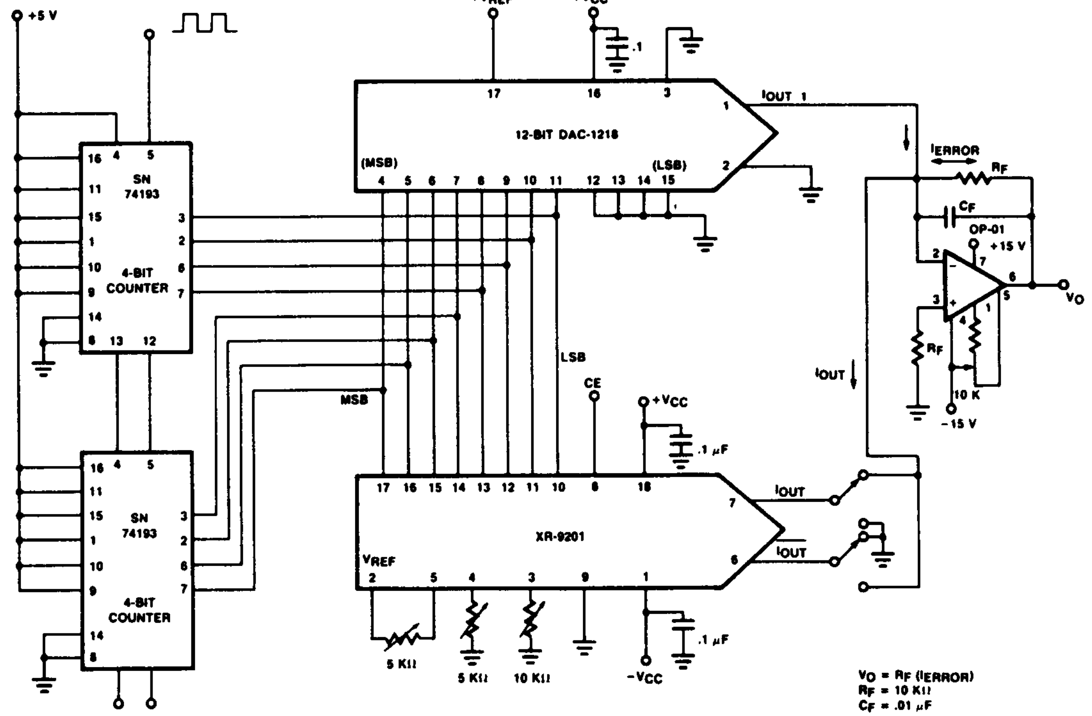
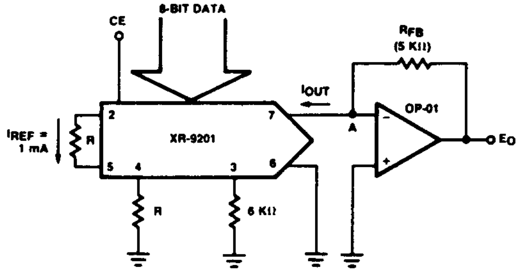


Figure 11. Relative Accuracy Test Circuit



0 V · EO · 10 V FOR RFB = 5 KΩ, IREF = 1 mA

IFS = 2(IREF) (255/256)

FOR OPERATION WITH NEGATIVE LOGIC D/A CONVERSION, I.E. ZERO FULL SCALE (0000 0000) CORRESPONDING TO FULL SCALE OUTPUT, CONNECT THE INVERTING INPUT OF OP AMP TO I_O (PIN 6) AND CONNECT $\overline{I_O}$ (PIN 7) TO GROUND.

Figure 12. Digital-to-Analog Conversion: Unipolar Operation

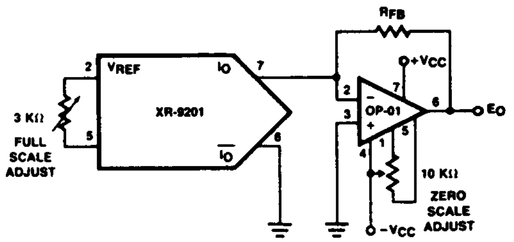


Figure 13. Full Scale and Zero Scale Adjustment

Table 1. Unipolar Operation — Input/Output Relationship

	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0	I_O (mA)	E_O (V)
Positive Full Scale	1	1	1	1	1	1	1	1	1.992	9.960
Pos. Full Scale – LSB	1	1	1	1	1	1	1	0	1.984	9.922
Pos. Full Scale – MSB	0	1	1	1	1	1	1	1	0.992	4.961
Zero Full Scale + LSB	0	0	0	0	0	0	0	1	0.008	0.039

Table 2. Bipolar Operation: Input/Output Relationship

	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0	E_1 (V)	E_0 (V)
Full Scale Output	1	1	1	1	1	1	1	1	0.000	10.00
Full Scale − LSB	1	1	1	1	1	1	1	0	0.016	9.921
Zero Scale + MSB	1	0	0	0	0	0	0	0	1.984	0.078
Full Scale − MSB	0	1	1	1	1	1	1	1	2.000	0.000
Zero Scale + LSB	0	0	0	0	0	0	0	1	3.968	−9.844
Zero Scale	0	0	0	0	0	0	0	0	3.984	−9.922

BIPOLAR OUTPUT OPERATION

Figure 14 shows a basic bipolar output operation. For full scale input (1111,1111) the output voltage is equal to 1.0V. For zero scale input (0000,0000), output voltage is equal to −1.0V. Due to the internal circuitry of the XR-9201, the current output terminals should not be pulled below approximately −1.0 volt. Therefore the circuit shown in Figure 14 would not function for E_O less than −1.0V. For bipolar operation with larger output voltages, the circuit shown in Figure 15 is recommended. Note that the current outputs, I_O and $\overline{I_O}$, are held at zero volts for all digital inputs for greater accuracy.

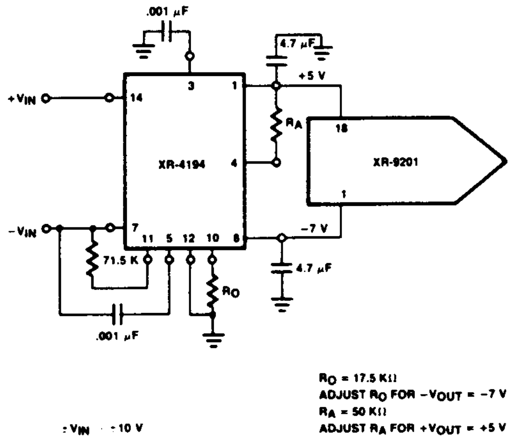


Figure 15. Digital-to-Analog Conversion — Bipolar Operation

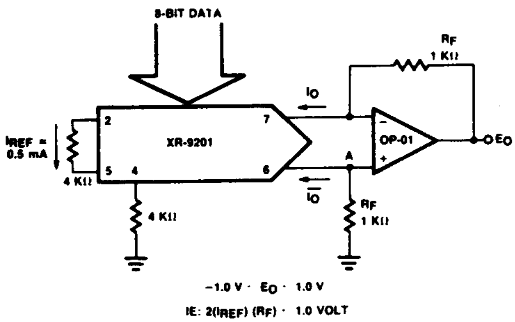
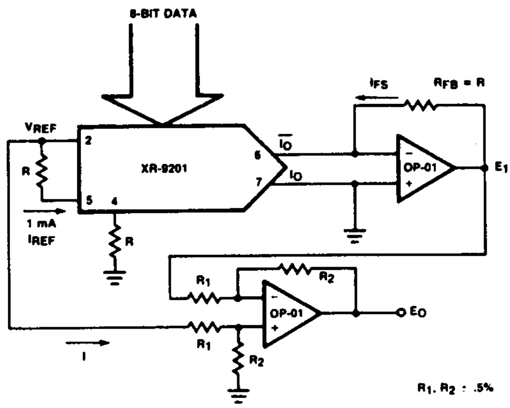


Figure 14. Digital-to-Analog Conversion — Bipolar Operation



$E_0 = \frac{R_2}{R_1}(V_{REF} - E_1)$

V_{REF} = 2 V, R = 2 K, R_{FB} = 2 K, R_2 = 50 K, R_1 = 10 K

NOTE: (I + I_{REF}) MUST BE LESS THAN 6 mA FOR PROPER OPERATION.

Figure 16. Regulated Supplies for XR-9201

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EXAR

XR-1488/1489A

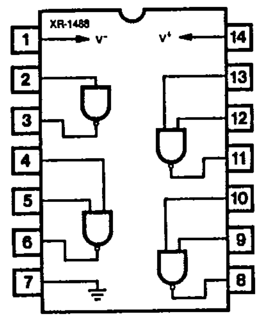
Quad Line Driver/Receiver

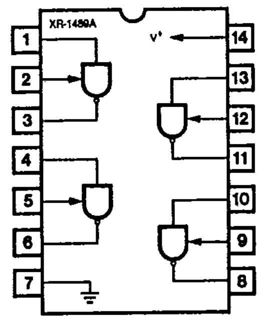
GENERAL DESCRIPTION

The XR-1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS232C. This extremely versatile integrated circuit can be used to perform a wide range of applications. Features such as output current limiting, independent positive and negative power supply driving elements, and compatibility with all DTL and TTL logic families greatly enhance the versatility of the circuit.

The XR-1489A is a monolithic quad line receiver designed to interface data terminal equipment with data communications equipment. the XR-1489A quad receiver along with its companion circuit, the XR-1488 quad driver, provide a complete interface system between DTL or TTL logic levels and the RS232C defined voltage and impedance levels.

FUNCTIONAL BLOCK DIAGRAMS





ABSOLUTE MAXIMUM RATINGS

Power Supply	
XR-1488	±15 Vdc
XR-1489A	+10 Vdc
Power Dissipation	
Ceramic Package	1000 mW
Derate above +25°C	6.7 mW/°C
Plastic Package	650 mW/°C
Derate above +25°C	5 mW/°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1488N	Ceramic	0°C to +70°C
XR-1488P	Plastic	0°C to +70°C
XR-1489AN	Ceramic	0°C to +70°C
XR-1489AP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-1488 and XR-1489A are a matched set of quad line drivers and line receivers designed for interfacing between TTL/DTL and RS232C data communication lines.

The XR-1488 contains four independent split supply line drivers, each with a ±10 mA current limited output. For RS232C applications, the slew rate can be reduced to the 30 V/μS limit by shunting the output to ground with a 410 pF capacitor. The XR-1489A contains four independent line receivers, designed for interfacing RS232C to TTL/DTL. Each receiver features independently programmable switching thresholds with hysteresis, and input protection to ±30 V. The output can typically source 3 mA and sink 20 mA.

XR-494

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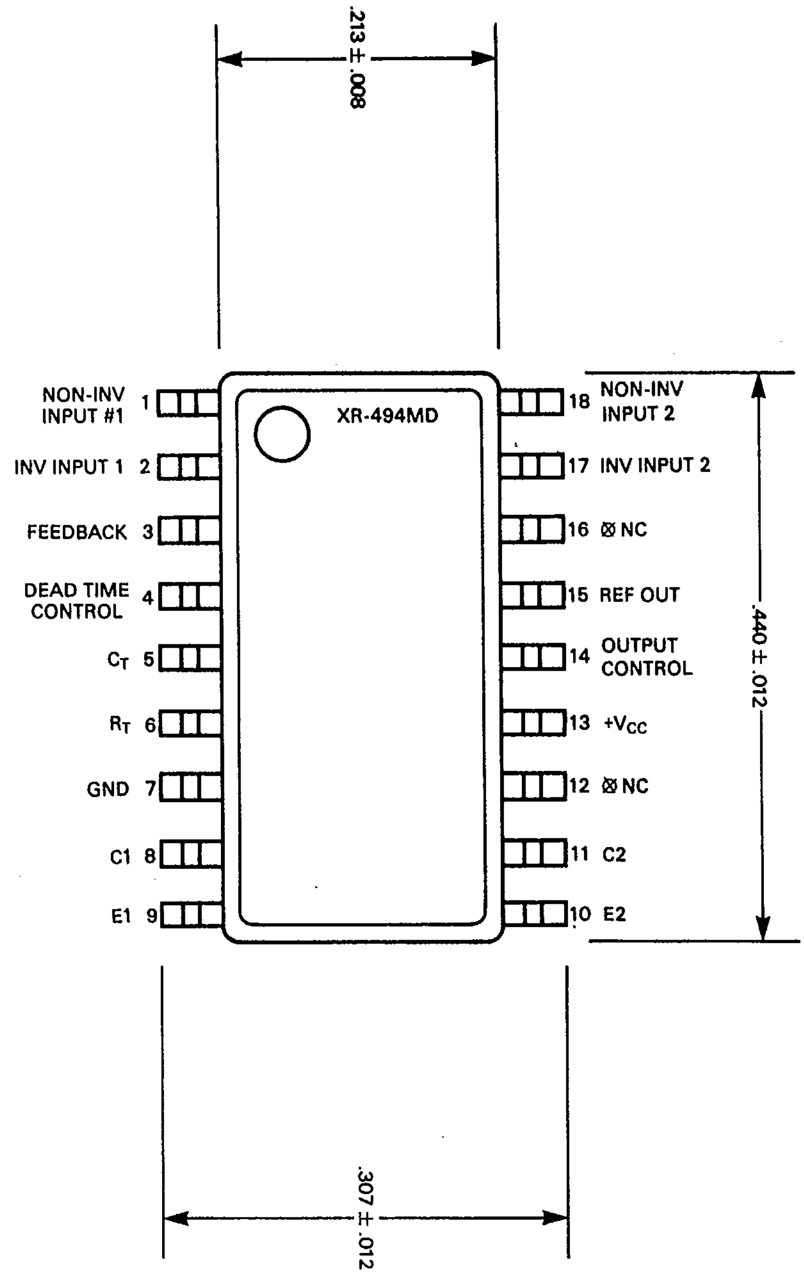


EXAR

XR-1468/1568

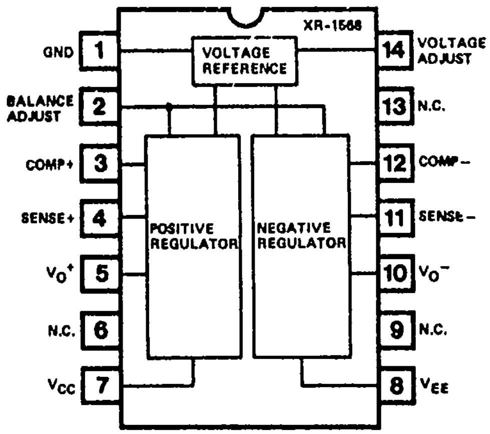
Dual-Polarity Tracking Voltage Regulator

GENERAL DESCRIPTION

The XR-1468/1568 is a dual polarity tracking voltage regulator, internally trimmed for symmetrical positive and negative 15V outputs. Current output capability is 100 mA, and may be increased by adding external pass transistors. The device is intended for local "on-card" regulation, which eliminates the distribution problems associated with single point regulation.

The XR-1468CN and XR-1568N are guaranteed over the 0°C to 70°C commercial temperature range. The XR-1568M is rated over the full military temperature range of −55°C to +125°C.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Internally Set for ±15V Outputs
±100 mA Peak Output Current
Output Voltages Balanced Within 1% (XR-1568)
0.06% Line and Load Regulation
Low Stand-By Current
Output Externally Adjustable from ±8 to ±20 Volts
Externally Adjustable Current Limiting
Remote Sensing

ORDERING INFORMATION

Part Number	Temperature	Output Offset	Package
XR-1568M	−55°C to +125°C	±150 mV max	Ceramic
XR-1568N	0°C to +70°C	±150 mV max	Ceramic
XR-1468CN	0°C to +70°C	±300 mV max	Ceramic

APPLICATIONS

Main Regulation in Small Instruments
On-Card Regulation in Analog and Digital Systems
Point-of-Load Precision Regulation

ABSOLUTE MAXIMUM RATINGS

Power Supply	±30 Volts
Minimum Short-Circuit Resistance	4.0 Ohms
Load Current, Peak	±100 mA
Power Dissipation	
Ceramic (N) Package	1.0 Watt
Derate Above +25°C	6.7 mW/°C
Operating Temperature	
XR-1568M	−55°C to +125°C
XR-1568/XR-1468C	0°C to +70°C
Storage Temperature	−65°C to +150°C

SYSTEM DESCRIPTION

The XR-1468/1568 is a dual polarity tracking voltage regulator combining two separate regulators with a common reference element in a single monolithic circuit, thus providing a very close balance between the positive and negative output voltages. Outputs are internally set to ±15 Volts but can be externally adjusted between ±8.0 to ±20 Volts with a single control. The circuit features ±100 mA output current, with externally adjustable current limiting, and provision for remote voltage sensing.

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