μPD9516AD/17AD
CMOS Serial Interface CODEC-Filter Combination

Description

The μPD9516AD and μPD9517AD are monolithic PCM codecs with integrated filters. These devices, which are limited-feature versions of the μPD9513AD/9514AD, provide transmit A/D and receive D/A conversions of vf signals using companded μ-law or A-law format.They interface the PCM highway through serial ports.

At the vf input, the transmit section includes an adjustable-gain operational amplifier, a lowpass antialiasing filter, and a 200-3400 Hz bandpass filter. The filtered signal is sampled and encoded using a very accurate dc reference voltage. An autozero circuit corrects for dc offset.

The receive section reconstructs an analog signal from the companded digital signal and passes the signal through a 3400-Hz lowpass filter that corrects for the (sin x)/x response of the decoder output. A balanced power amplifier at the analog vf receive port allows maximum flexibility in output configurations.

The μPD9516AD and 9517AD can operate in fixed or variable data rate mode. In the fixed data rate mode, the master clock and the PCM data clock are internally set to 2.048 MHz. In the variable data rate mode, the PCM data clock can vary from 64 kHz to 2.048 MHz.

The μPD9516AD and 9517AD are most suited to telecommunications applications. They are ideal for D3/D4 type channel banks and subscriber carrier systems, digital PBXs and central office switching systems, and digital telephone handsets. Their wide dynamic range makes them attractive for any application requiring digital processing of vf signals.

Packaged in 16-pin DIPs, the μPD9516AD and 9517AD are ideal for high-density applications.

Features

- Complete codec and filtering in a single chip
  - Transmit highpass and lowpass filters
  - Transmit op amp for gain adjustment
  - Receive lowpass filter with (sin x)/x correction
  - Receive output power amplifier
  - Autozero circuit
  - Highly-accurate reference voltage
  - μ-law (μPD9516AD) or A-law (μPD9517AD) companding
  - Serial digital I/O interface
- Two timing modes
  - Fixed data rate mode (2.048 MHz)
  - Variable data rate mode (64 kHz to 2.048 MHz)
- Meets or exceeds D3/D4 and CCITT specifications
- Low power consumption
  - 80 mW in normal operation
  - 8 mW in power-down mode
- Latchup-free during power-up sequence

Ordering Information

Part Number	Companding	Package
μPD9516AD	μ-law	16-pin ceramic DIP (300 mil)
μPD9517AD	A-law	

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Block Diagram