

# NDF02N60Z, NDP02N60Z, NDD02N60Z

## N-Channel Power MOSFET 600 V, 4.0 $\Omega$

### Features

- Low ON Resistance
- Low Gate Charge
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

### ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub> = 25°C unless otherwise noted)

Rating	Symbol	NDF	NDP	NDD	Unit
Drain-to-Source Voltage	V <sub>DSS</sub>	600			V
Continuous Drain Current R <sub>θJC</sub>	I <sub>D</sub>	2.4 (Note 1)	2.4	2.2	A
Continuous Drain Current R <sub>θJC</sub> T <sub>A</sub> = 100°C	I <sub>D</sub>	1.6 (Note 1)	1.6	1.4	A
Pulsed Drain Current, V <sub>GS</sub> @ 10 V	I <sub>DM</sub>	10 (Note 1)	10	9	A
Power Dissipation R <sub>θJC</sub>	P <sub>D</sub>	24	72	57	W
Gate-to-Source Voltage	V <sub>GS</sub>	30			V
Single Pulse Avalanche Energy, I <sub>D</sub> = 2.4 A	E <sub>AS</sub>	120			mJ
ESD (HBM) (JESD 22-A114)	V <sub>esd</sub>	2500			V
RMS Isolation Voltage (t = 0.3 sec., R.H. ≤ 30%, T <sub>A</sub> = 25°C) (Figure 17)	V <sub>ISO</sub>	4500			V
Peak Diode Recovery	dv/dt	4.5 (Note 2)			V/ns
Continuous Source Current (Body Diode)	I <sub>S</sub>	2.4			A
Maximum Temperature for Soldering Leads	T <sub>L</sub>	260			°C
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150			°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

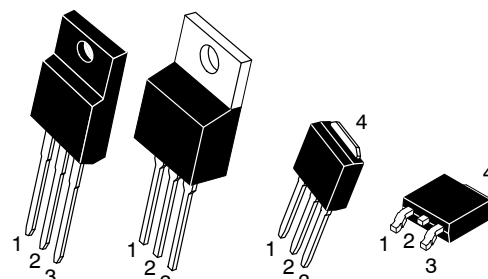
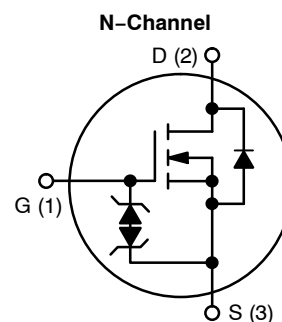
1. Limited by maximum junction temperature
2. I<sub>SD</sub> = 2.4 A, di/dt ≤ 100 A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, T<sub>J</sub> = +150°C



ON Semiconductor®

<http://onsemi.com>

V <sub>DSS</sub>	R <sub>DS(on)</sub> (TYP) @ 1 A
600 V	4.0 $\Omega$



TO-220FP TO-220AB IPAK DPAK  
CASE 221D CASE 221A CASE 369D CASE 369AA  
STYLE 1 STYLE 5 STYLE 2 STYLE 2

### MARKING AND ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

# NDF02N60Z, NDP02N60Z, NDD02N60Z

## THERMAL RESISTANCE

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	NDP02N60Z	1.7	°C/W
	NDF02N60Z	5.2	
	NDD02N60Z	2.2	
Junction-to-Ambient Steady State	(Note 3) NDP02N60Z	51	
	(Note 3) NDF02N60Z	51	
	(Note 4) NDD02N60Z	41	
	(Note 3) NDD02N60Z-1	80	

3. Insertion mounted

4. Surface mounted on FR4 board using 1" sq. pad size, (Cu area = 1.127 in sq [2 oz] including traces).

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 mA	BV <sub>DSS</sub>	600			V
Breakdown Voltage Temperature Coefficient	Reference to 25°C, I <sub>D</sub> = 1 mA	ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>		0.6		V/°C
Drain-to-Source Leakage Current	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V	25°C	I <sub>DSS</sub>		1	μA
		150°C			50	
Gate-to-Source Forward Leakage	V <sub>GS</sub> = ±20 V	I <sub>GSS</sub>			±10	μA

### ON CHARACTERISTICS (Note 5)

Static Drain-to-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.0 A	R <sub>DS(on)</sub>		4.0	4.8	Ω
Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 50 μA	V <sub>GS(th)</sub>	3.0		4.5	V
Forward Transconductance	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 1.2 A	g <sub>FS</sub>		1.7		S

### DYNAMIC CHARACTERISTICS

Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	C <sub>iss</sub>		274		pF
Output Capacitance		C <sub>oss</sub>		34		
Reverse Transfer Capacitance		C <sub>rss</sub>		7.0		
Total Gate Charge	V <sub>DD</sub> = 300 V, I <sub>D</sub> = 2.4 A, V <sub>GS</sub> = 10 V	Q <sub>g</sub>		10.1		nC
Gate-to-Source Charge		Q <sub>gs</sub>		2.4		
Gate-to-Drain ("Miller") Charge		Q <sub>gd</sub>		5.3		
Plateau Voltage	V <sub>DD</sub> = 300 V, I <sub>D</sub> = 2.4 A, V <sub>OS</sub> = 10 V	V <sub>GP</sub>		6.4		V
Gate Resistance		R <sub>g</sub>		4.9		Ω

### RESISTIVE SWITCHING CHARACTERISTICS

Turn-On Delay Time	V <sub>DD</sub> = 300 V, I <sub>D</sub> = 2.4 A, V <sub>GS</sub> = 10 V, R <sub>G</sub> = 5 Ω	t <sub>d(on)</sub>		9.0		ns
Rise Time		t <sub>r</sub>		7.0		
Turn-Off Delay Time		t <sub>d(off)</sub>		15		
Fall Time		t <sub>f</sub>		7.0		

### SOURCE-DRAIN DIODE CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Diode Forward Voltage	I <sub>S</sub> = 2.4 A, V <sub>GS</sub> = 0 V	V <sub>SD</sub>			1.6	V
Reverse Recovery Time	V <sub>GS</sub> = 0 V, V <sub>DD</sub> = 30 V I <sub>S</sub> = 2.4 A, di/dt = 100 A/μs	t <sub>rr</sub>		240		ns
Reverse Recovery Charge		Q <sub>rr</sub>		0.7		μC

5. Pulse Width ≤ 380 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

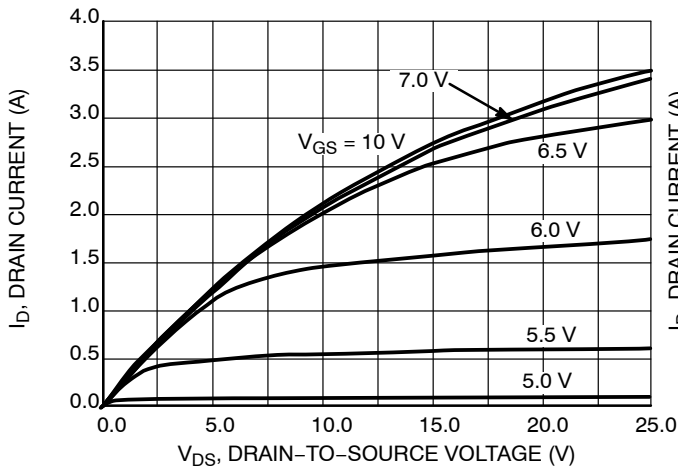


Figure 1. On-Region Characteristics

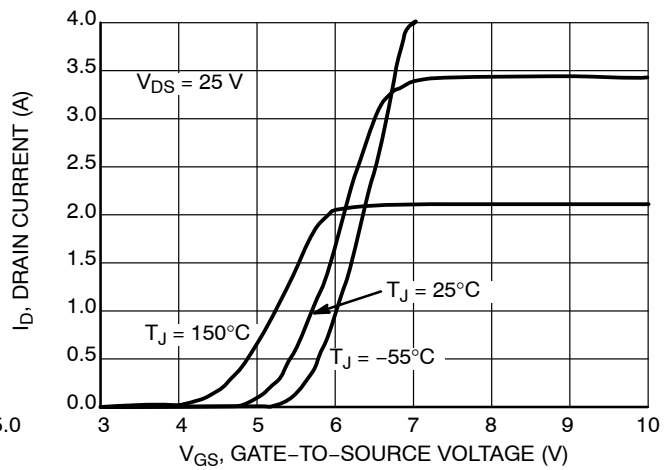


Figure 2. Transfer Characteristics

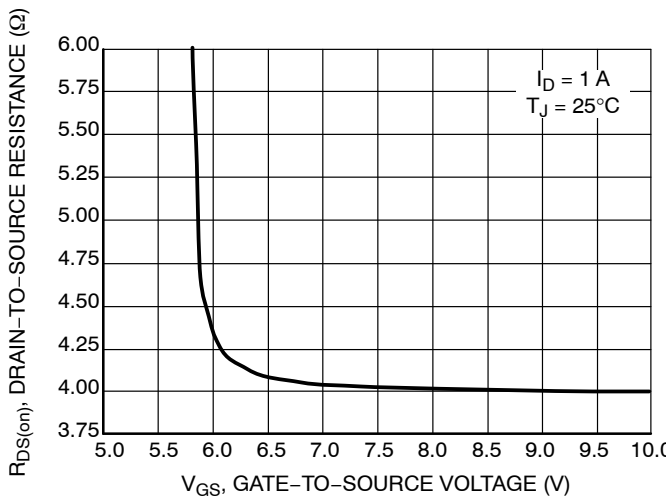


Figure 3. On-Region versus Gate-to-Source Voltage

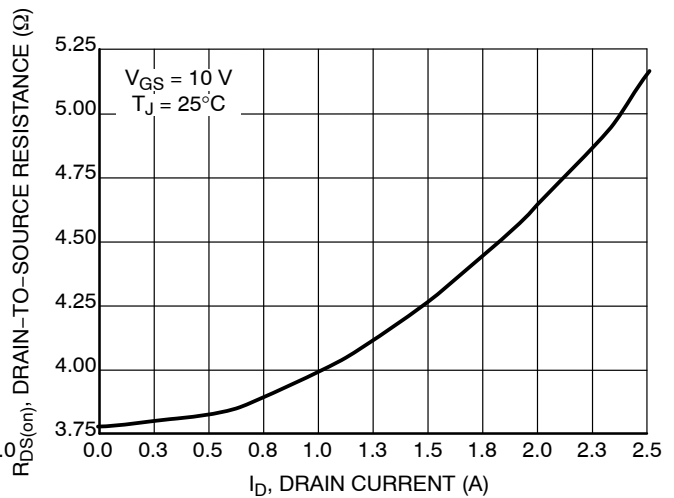


Figure 4. On-Resistance versus Drain Current and Gate Voltage

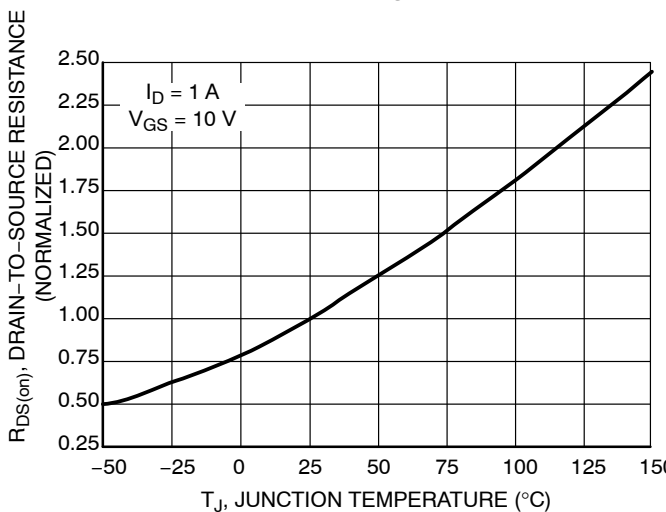


Figure 5. On-Resistance Variation with Temperature

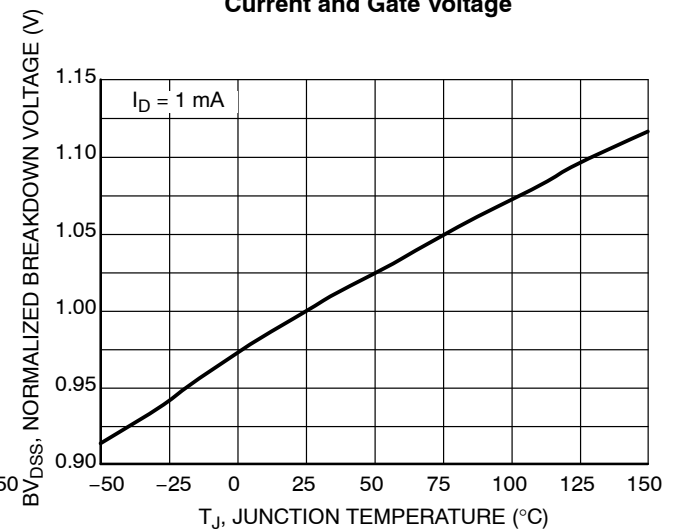


Figure 6.  $BV_{DSS}$  Variation with Temperature

TYPICAL CHARACTERISTICS

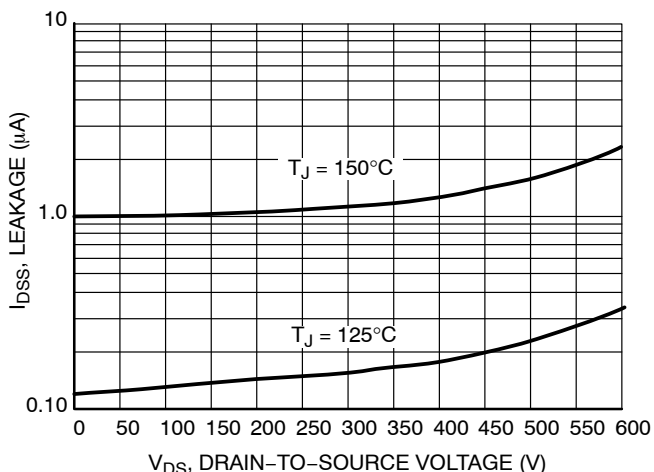


Figure 7. Drain-to-Source Leakage Current versus Voltage

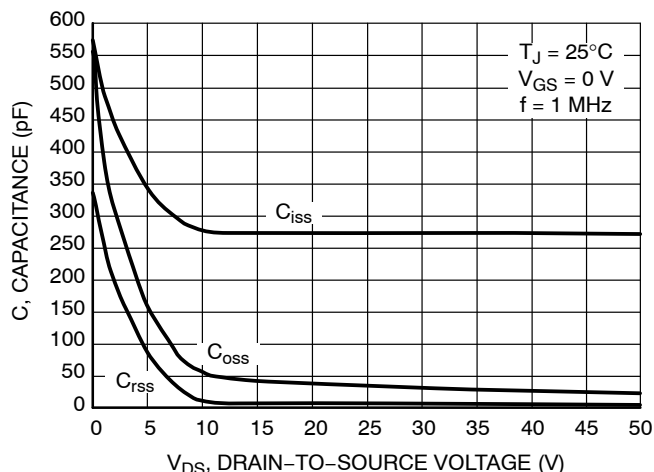


Figure 8. Capacitance Variation

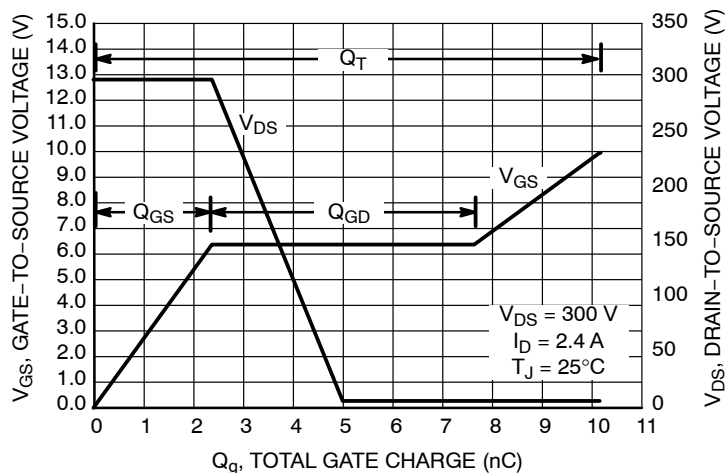


Figure 9. Gate-to-Source Voltage and Drain-to-Source Voltage versus Total Charge

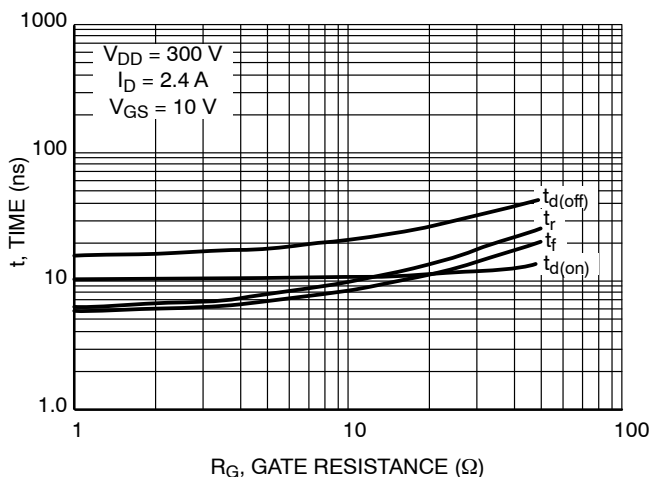


Figure 10. Resistive Switching Time Variation versus Gate Resistance

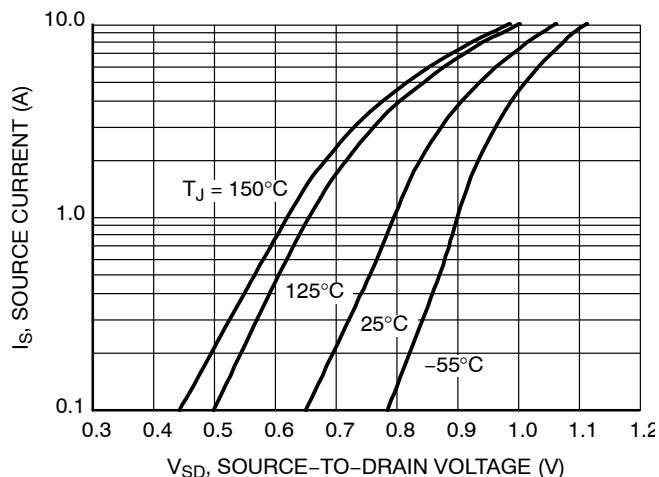


Figure 11. Diode Forward Voltage versus Current

TYPICAL CHARACTERISTICS

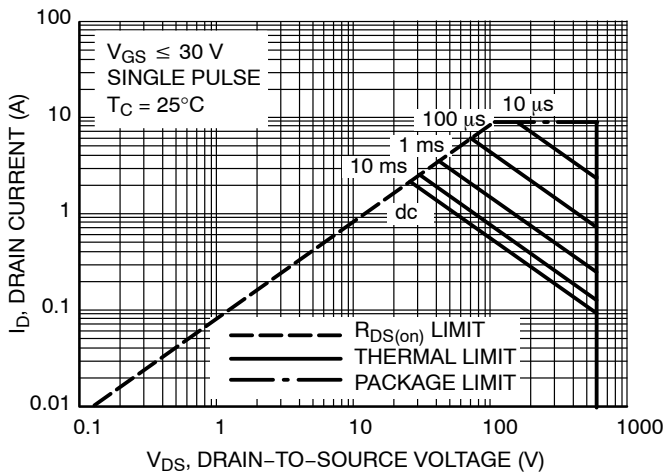


Figure 12. Maximum Rated Forward Biased Safe Operating Area NDD02N60Z

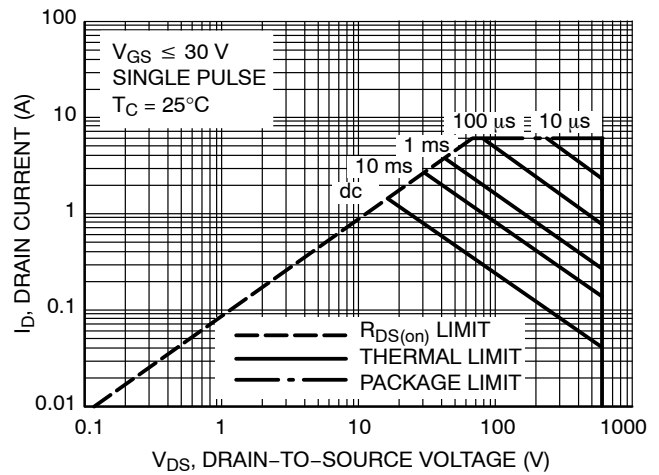


Figure 13. Maximum Rated Forward Biased Safe Operating Area NDF02N60Z

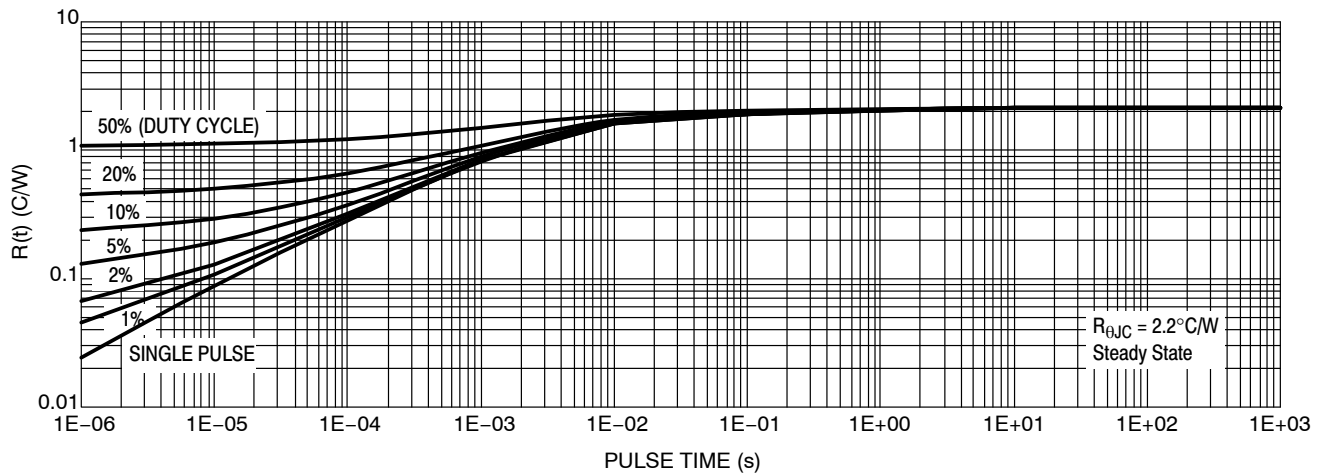


Figure 14. Thermal Impedance (Junction-to-Case) for NDD02N60Z

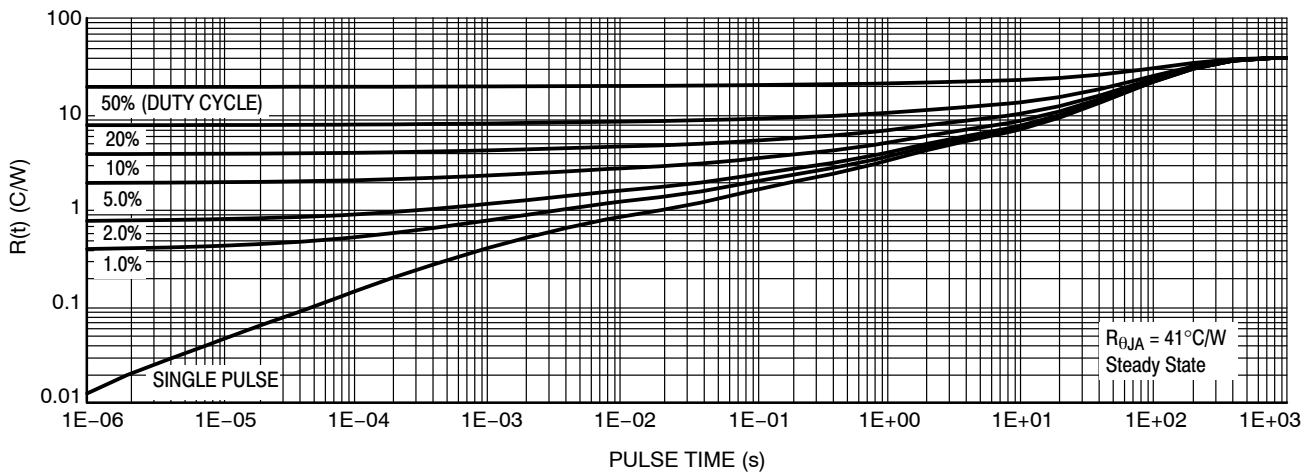


Figure 15. Thermal Impedance (Junction-to-Ambient) for NDD02N60Z

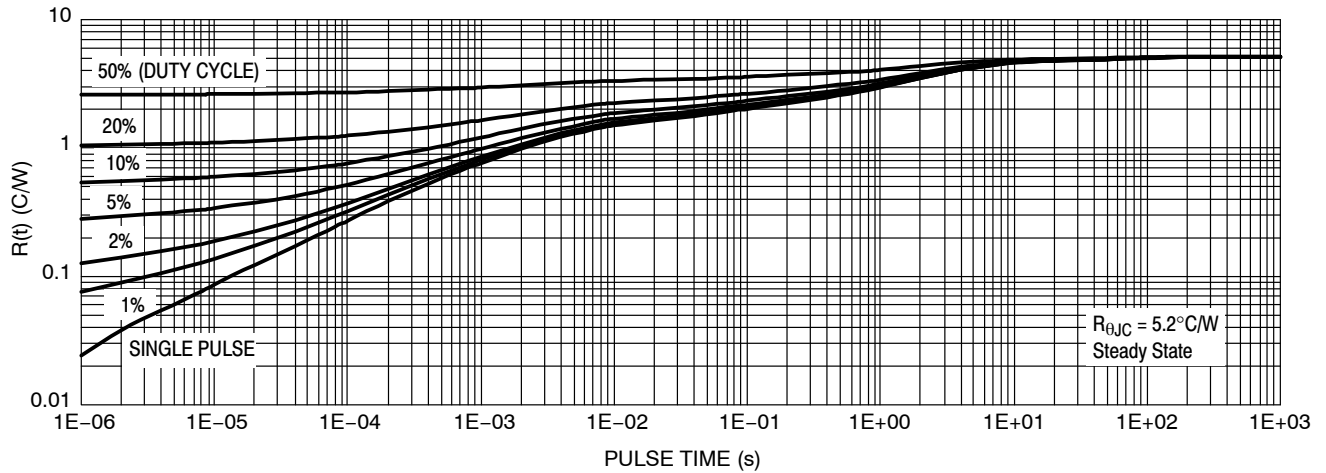


Figure 16. Thermal Impedance (Junction-to-Case) for NDF02N60Z

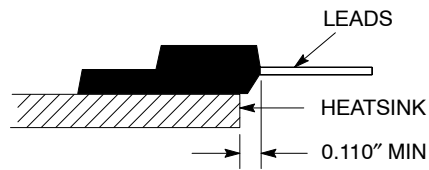


Figure 17. Isolation Test Diagram

Measurement made between leads and heatsink with all leads shorted together.

\*For additional mounting information, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

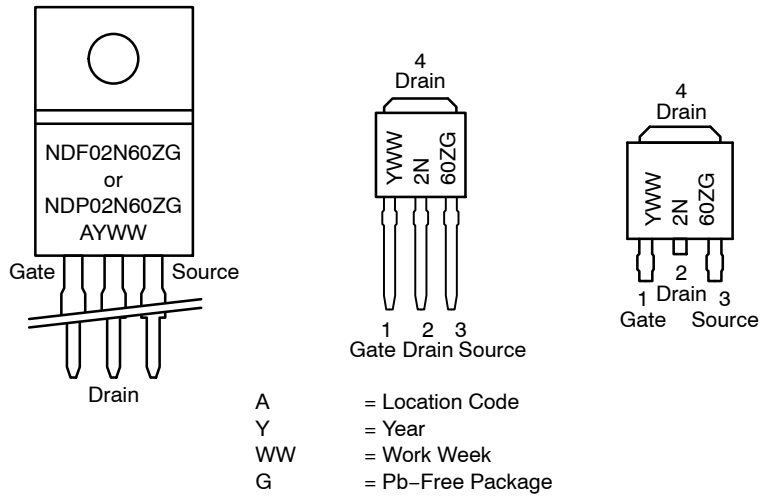
# NDF02N60Z, NDP02N60Z, NDD02N60Z

## ORDERING INFORMATION

Order Number	Package	Shipping†
NDF02N60ZG	TO-220FP (Pb-Free)	50 Units / Rail
NDP02N60ZG	TO-220AB (Pb-Free)	50 Units / Rail In Development
NDD02N60Z-1G	IPAK (Pb-Free)	75 Units / Rail
NDD02N60ZT4G	DPAK (Pb-Free)	2500 / Tape & Reel

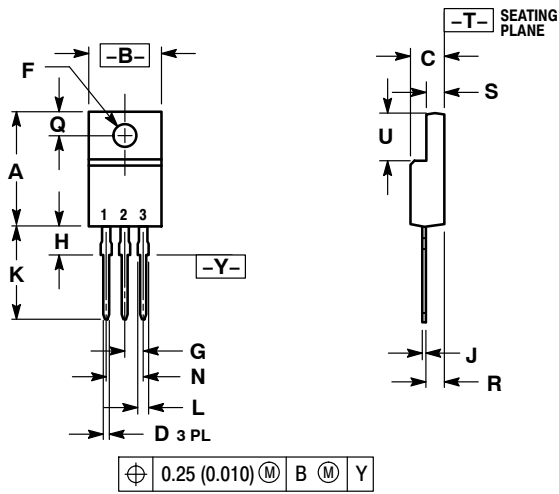
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## MARKING DIAGRAMS



PACKAGE DIMENSIONS

TO-220 FULLPAK  
CASE 221D-03  
ISSUE J

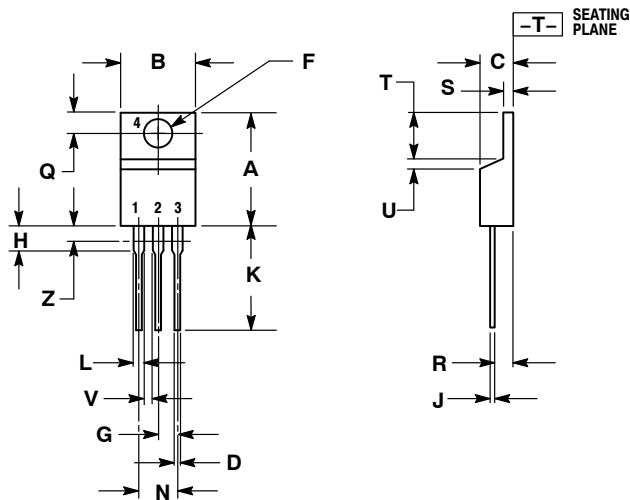


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH
  3. 221D-01 THRU 221D-02 OBSOLETE, NEW STANDARD 221D-03.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.617	0.635	15.67	16.12
B	0.392	0.419	9.96	10.63
C	0.177	0.193	4.50	4.90
D	0.024	0.039	0.60	1.00
F	0.116	0.129	2.95	3.28
G	0.100 BSC		2.54 BSC	
H	0.118	0.135	3.00	3.43
J	0.018	0.025	0.45	0.63
K	0.503	0.541	12.78	13.73
L	0.048	0.058	1.23	1.47
N	0.200 BSC		5.08 BSC	
Q	0.122	0.138	3.10	3.50
R	0.099	0.117	2.51	2.96
S	0.092	0.113	2.34	2.87
U	0.239	0.271	6.06	6.88

- STYLE 1:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE

TO-220AB  
CASE 221A-09  
ISSUE AE



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

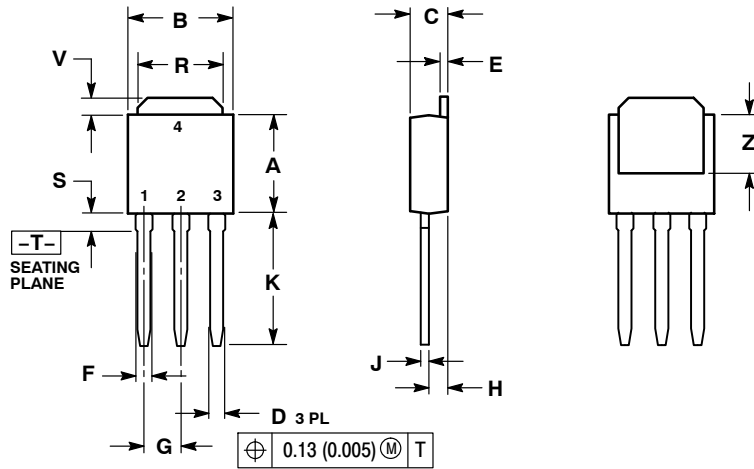
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.014	0.025	0.36	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

- STYLE 5:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN



PACKAGE DIMENSIONS

**IPAK**  
CASE 369D-01  
ISSUE B

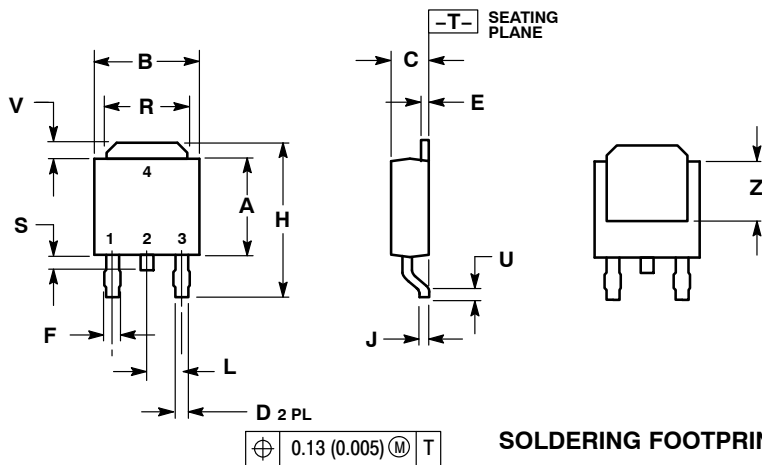


- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- STYLE 2:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

**DPAK**  
CASE 369AA-01  
ISSUE A

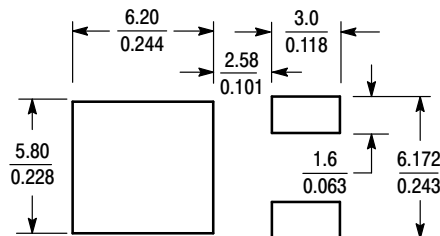


- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.025	0.035	0.63	0.89
E	0.018	0.024	0.46	0.61
F	0.030	0.045	0.77	1.14
H	0.386	0.410	9.80	10.40
J	0.018	0.023	0.46	0.58
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.024	0.040	0.60	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---


- STYLE 2:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

**SOLDERING FOOTPRINT\***



SCALE 3:1  $\left( \frac{\text{mm}}{\text{inches}} \right)$

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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