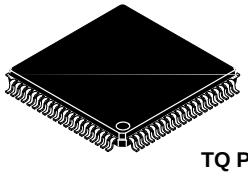
MCM67T415

Advance Information

16K x 15 Bit Cache Tag RAM for Pentium™ Processors



TQ PACKAGE
TQFP
CASE 917A–02

The MCM67T415 is a 245,760 bit cache–tag static RAM designed to support Pentium microprocessors at bus speeds up to 66 MHz. It is organized as 16K words of 15 bits each and is fabricated using Motorola's high performance, silicon gate BiCMOS technology. There are twelve common I/O tag bits and three separate I/O status bits. A 12–bit comparator is on–chip to allow fast comparison of the 12 stored tag bits with the current tag input data. An active high MATCH output is generated when the valid bit is true and these two groups of data are the same for a given address.

This high–speed MATCH signal, with t_{AVMV} times as fast as 9 ns, provides the fastest possible enabling of secondary cache accesses.

The three separate I/O status bits (VALID, DIRTY, and WT) can be configured for either dedicated or generic functionality, depending on the SFUNC input pin. With SFUNC low, the status bits are defined and used internally by the device, allowing easier determination of the validity and use of the given tag data. SFUNC high releases the defined internal status bit usage and control, allowing users to configure the status bit information to fit their system needs. A synchronous RESET pin, when held low at a rising clock edge, will reset all status bits in the array for easy invalidation of all tag addresses.

The MCM67T415 also provides the option for burst ready ($\overline{BRDY}$) generation within the cache tag itself, based upon MATCH, VALID bit, WT bit, and other external inputs provided by the user. This can significantly simplify cache controller logic and minimize cache decision time. Match and read operations are both asynchronous in order to provide the fastest access times possible, while write operations are synchronous for ease of system timing.

The MCM67T415 uses a 5 V power supply on V_{CC} and V_{SS}, with separate V_{CCQ} pins provided for the outputs to offer compliance with both 5 V TTL and 3.3 V LVTTL logic levels. The PWRDN pin offers a low–power standby mode, which provides significant system power savings.

The MCM67T415 is offered in a space saving 80–pin thin quad flat pack (TQFP) package.

- 16K x 15 Configuration:
  - 12 Tag Bits
  - Three Status Bits (Valid, Dirty, and WT)
- Valid Bit used to Qualify Match Output
- High–Speed Address–to–Match Comparison Times – 9/10/12 ns
- BRDY Circuitry Included Inside the Cache–Tag for the Highest Speed Operation
- Asynchronous Read/Match Operation and Synchronous Write and Reset Operation
- Separate Write Enable for Tag Bits and Status Bits
- Separate Output Enable for Tag Bits, Status Bits, and $\overline{BRDY}$
- Synchronous RESET Pin for Invalidation of all Tag Entries
- Dual Chip Selects for Easy Depth Expansion with No Performance Degradation
- I/O Pins Both 5 V TTL and 3.3 V LVTTL Compatible with V_{CCQ} Pins
- PWRDN Pin to Place Device in Low–Power Mode
- Drop–In Replacement for IDT71215
- Packaged in an 80–Pin Thin Quad Flat Pack (TQFP)

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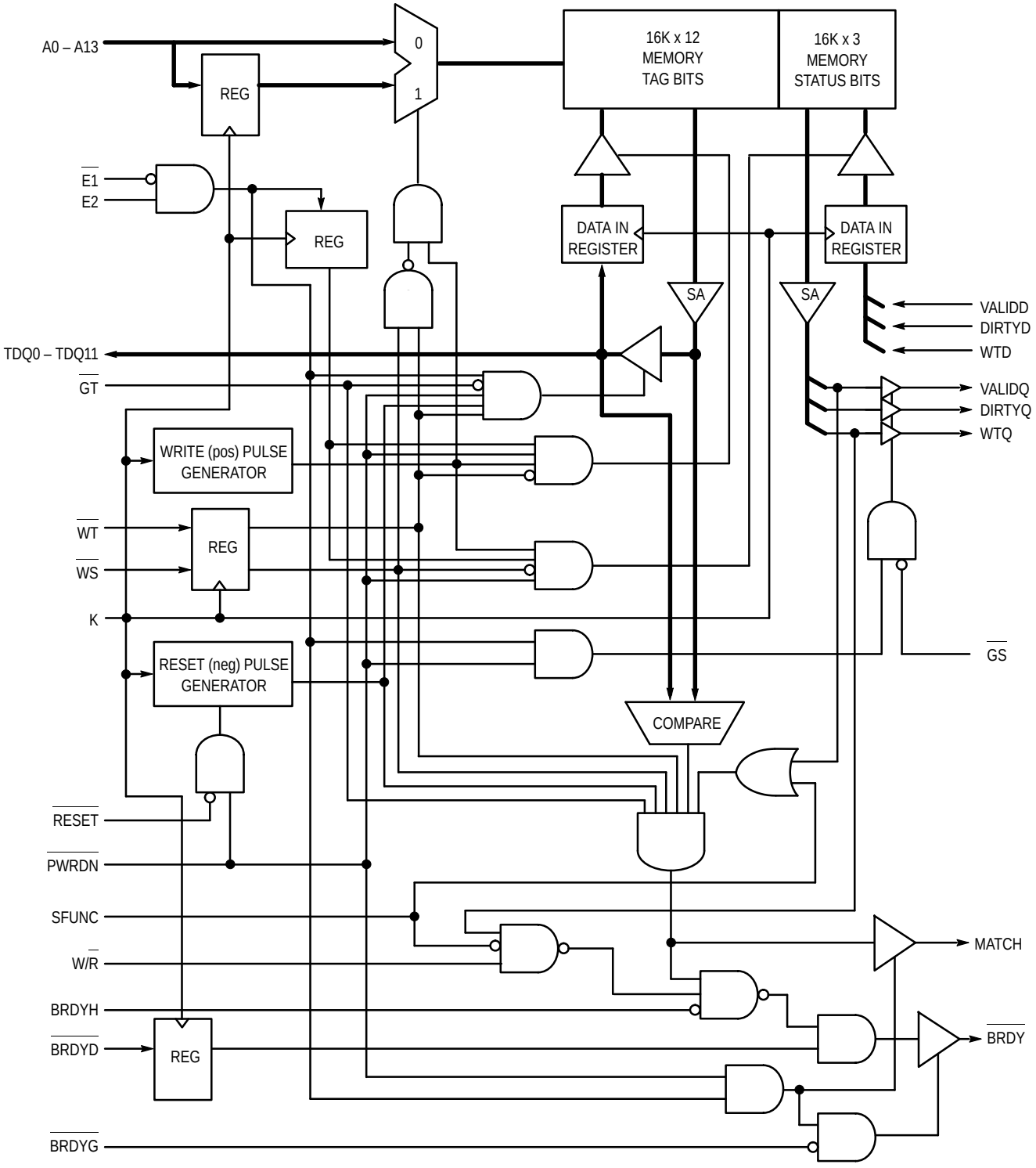
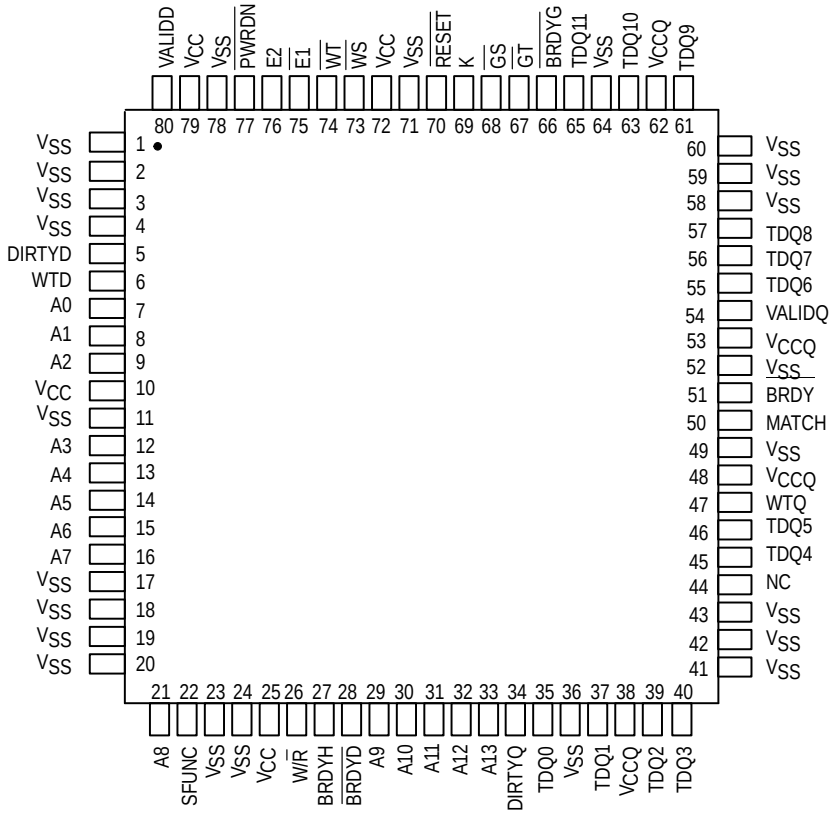
FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENTS



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