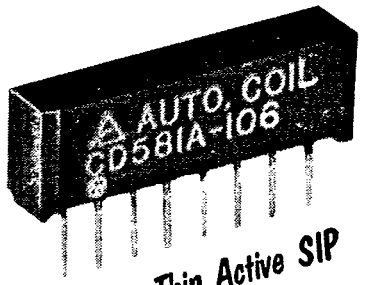
T-47-13

CD581 Series
TTL Digital Delay Module, 8 PIN, 5 TAP

- Requires minimum mounting space
- TTL input and outputs
- Precise and stable delays
- Reliable hybrid construction
- No external components required
- Fan out 10TTL loads/tap, 20TTL loads/package
- Operating temperature 0° to 70°C
- Storage temperature –55° to +125°C



Ultra Thin Active SIP

8 PIN SIP

Electrical Characteristics:

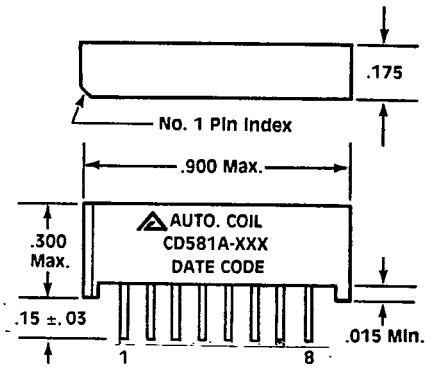
VIH	(High level input voltage)	2.0 To 5.0V
IIH	(High level input current)	50 μA Max.
VIL	(Low level input voltage)	0.8 V Max.
IIL	(Low level input current)	–2 ma Max.
VOH	(High level output voltage)	2.5 V Min.
VOL	(Low level output voltage)	0.5 V Max.
VCC	(Supply voltage)	5.0 V ±0.25 V DC
ICC	(Supply current)	75 ma Max.

Mechancial Specifications:
Case: Epoxy filled D.A.P.
Leads: Phosphor bronze or equiv. solder coated
Marking: White epoxy ink

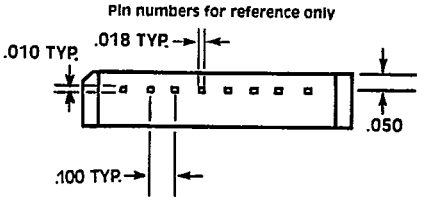
Also Available:
Intermediate delays
Non symmetrical tap delays
Tighter delay tolerances
Falling edge delay specifications
Non tapped modules

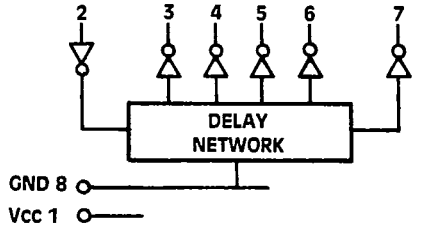
Input & test conditions are not limiting parameters.
All digital delay modules can be operated at conditions other than specified.
Since accuracies may be slightly affected, we suggest that the module be evaluated under specific operating conditions.

Specifications subject to change without notice.



Pin numbers for reference only





Nominal Delays (In NS) ±2 NS or 5% Whichever Is Greater					
Automatic Coil Part Number	PIN 3	PIN 4	PIN 5	PIN 6	PIN 7
CD581A-101	5	10	15	20	25
CD581A-102	6	12	18	24	30
CD581A-103	7	14	21	28	35
CD581A-104	8	16	24	32	40
CD581A-105	9	18	27	36	45
CD581A-106	10	20	30	40	50
CD581A-107	15	30	45	60	75
CD581A-108	20	40	60	80	100
CD581A-109	25	50	75	100	125
CD581A-110	30	60	90	120	150
CD581A-111	40	80	120	160	200
CD581A-112	50	100	150	200	250
CD581A-113	60	120	180	240	300
CD581A-114	70	140	210	280	350
CD581A-115	80	160	240	320	400
CD581A-116	90	180	270	360	450
CD581A-117	100	200	300	400	500

Output rise times (TPLH) 4.0 NS max. (0.75 to 2.4 V level).

Test Conditions:
1) All measurements are made @ 25°C
2) VCC is maintained @ 5.0 VDC
3) All measurements are made with no loads on outputs
4) Delays are measured @ 1.5V level
5) Delays & tolerances for leading edges only (TPLH) – falling edges (TPHL) closely matched to TPLH

Input Conditions:
1) Pulse amplitude: 3.20V
2) Input rise time 3.0 NS (10 to 90%)
3) Pulse width 2 × total delay
4) Duty cycle < 25%

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