TLC320AD91C
Data Manual

Stereo Audio Codec

SLAS185A
October 1998

TEXAS INSTRUMENTS

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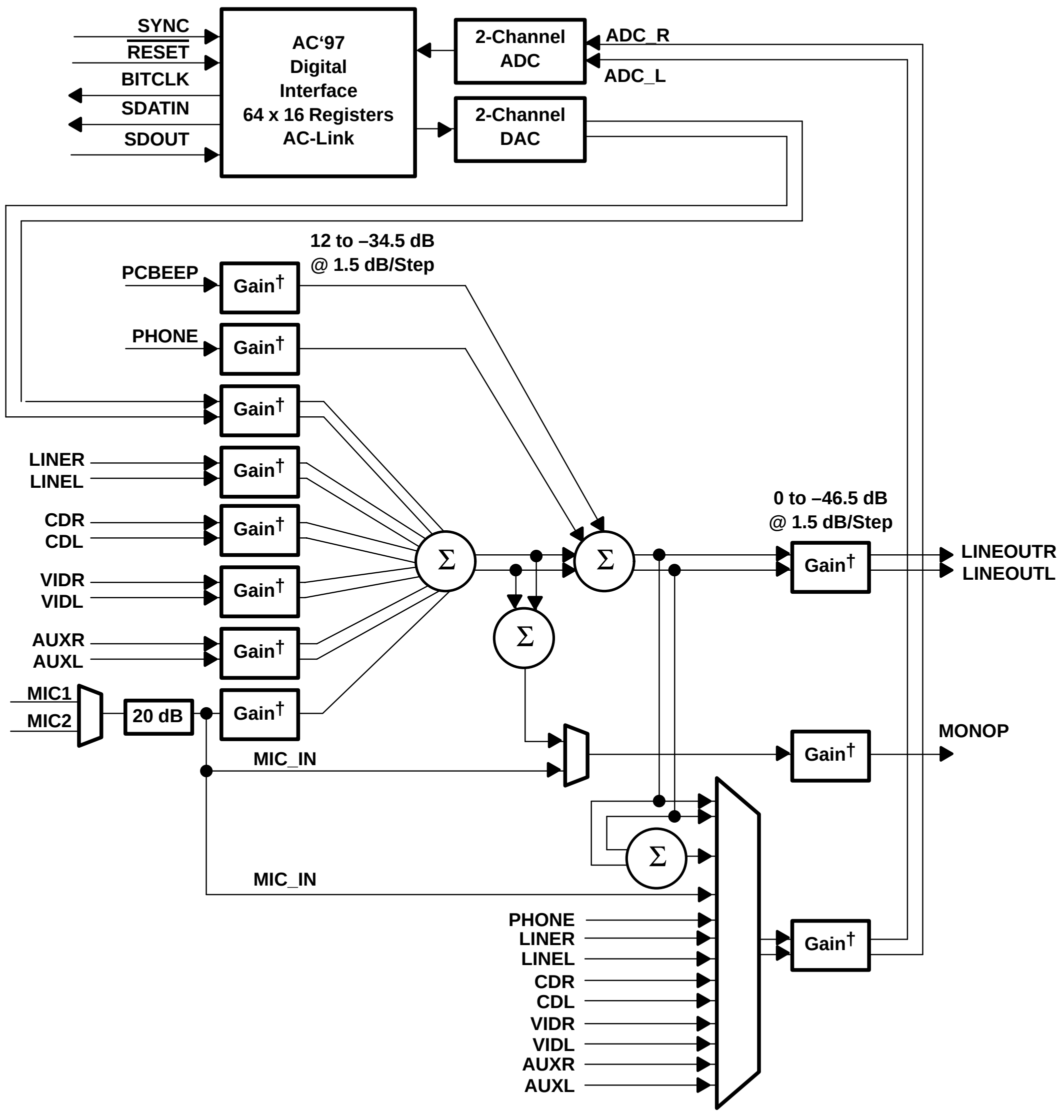
1 Introduction

The TLC320AD91C is designed to be 100% compliant with the audio codec ‘97 (AC‘97) standard specification. The codec is designed to be controlled by a digital controller. The two fixed 48-kHz sample rate DACs support a stereo PCM output channel that contains a mix, determined by the codec controller, of all digital audio sources, including an internal synthesizer, and any other digital sources. The output of these DACs is mixed with additional analog sources and sent to the independently-controlled LINOP output. For a speakerphone, the MONOP output delivers either mic only or a mono mix of sources to a telephony subsystem. The ADC path supports two channels of fixed 48-kHz sample rate inputs. The standard stereo PCM input channel supports the record of any mono or stereo source, or a mix of sources.

1.1 Features

- Compliant with Audio Codec (AC) ’97 Specification
- Serial (AC-Link) Interface Port
- Full-Duplex Codec with 18-Bit Resolution ADC and DAC
- 48-kHz Sample Rate
- Multiple Stereo Input Mixer: LINE, CD, VID, and AUX
- Line Level Mono Inputs for Speakerphone and BEEP
- Mono Mic Input Switchable From Two Different Sources
- Very Low Interchannel Crosstalk Preserves Stereo Fidelity
- ADC and DAC Total Harmonic Distortion Met for Full-Scale (0.9 V_{rms}) Levels
- Stereo Line Level Output Plus Mono Output For Speakerphone
- Mono and Stereo Volume Control
- Power Management Support (Power Down Mode)
- Interfaces to 5-V or 3.3-V Digital Controller
- Operates From 3.3-V or 5.5-V Power Supply
- Standard 48-Pin TQFP Package
- Tone Free ADC and DAC in PC Environment

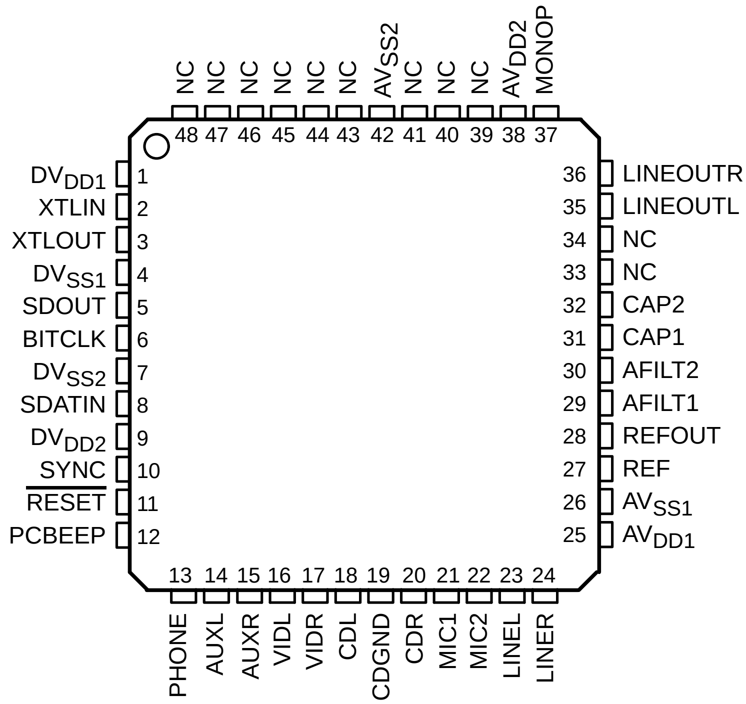
1.2 Functional Block Diagram



† Gain = Gain, Attenuate, Mute

1.3 Terminal Assignments

PT PACKAGE
(TOP VIEW)



NC – No internal connection

1.4 Ordering Information

T_A	PACKAGE CHIP CARRIER (PT)
0°C to 70°C	TLC320AD91CPT

1.5 Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AFILT1	29	I	Reference input/output. Pulls to midrail if not driven.
AFILT2	30	O	On-chip generated supply independent reference output
AUXL	14	I	Auxiliary input left channel from internal connector. AUXL is used for upgrade synthesizer or other source.
AUXR	15	I	Auxiliary input right channel from internal connector. AUXR is used for upgrade synthesizer or other source.
AV_{DD1}	25	I	Analog 5-V supply voltage
AV_{DD2}	38	I	Analog 5-V supply voltage
AV_{SS1}	26	I	Analog ground
AV_{SS2}	42	I	Analog ground
BITCLK	6	O	12.288-MHz serial data clock
CDGND	19	I	CD audio analog ground (for pseudo-differential inputs) from CDROM.
CAP1	31	O	Buffered AFILT1. Used as ADC reference.
CAP2	32	O	Buffered AFILT1. Used as DAC reference.
CDL	18	I	CD audio left channel from CDROM – pseudo-differential input
CDR	20	I	CD audio right channel from CDROM – pseudo-differential input
DV_{DD1}	1	I	Digital 5-V supply voltage
DV_{DD2}	9	I	Digital 5-V or 3.3-V supply voltage
DV_{SS1}	4	I	Digital ground
DV_{SS2}	7	I	Digital ground
LINEL	23	I	Line in left channel. LINEL connects to line-in jack. Will drive 600-Ω load.
LINER	24	I	Line in right channel. LINER connects to line-in jack. Will drive 600-Ω load.
LINEOUTL	35	O	Line output left channel to output jack.
LINEOUTR	36	O	Line output right channel to output jack.
MIC1	21	I	Desktop (primary) microphone input. MIC1 connects to the microphone jack.
MIC2	22	I	Second microphone input. MIC2 connects to the headset microphone jack.
MONOP	37	O	Mono output. MONOP is generally used to drive a telephony subsystem (and/or speakerphone card). Will drive 600-Ω load.
PCBEEP	12	I	PC speaker beep pass through. PCBEEP connects to the output of the PC speaker.
PHONE	13	I	Telephony subsystem speakerphone input (DLP – down line phone)
REF	27	O	Reference voltage
REFOUT	28	O	Reference voltage. Provides a 5-mA drive to bias microphones.
NC	33,34, 39–41, 43–48		No connect
$\overline{\text{RESET}}$	11	I	Master hardware reset
SDATIN	8	O	Serial time-division-multiplexed TLC320AD91C output stream
SDOUT	5	I	Serial time-division-multiplexed TLC320AD91C input stream
SYNC	10	I	48-kHz fixed sample sync signal

1.5 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
VIDL	16	I	Video audio left channel. VIDL connects to a TV tuner or video camera (typically an internal connector).
VIDR	17	I	Video audio right channel. VIDR connects to a TV tuner or video camera (typically an internal connector).
XTLIN	2	I	24.576-MHz crystal
XTLOUT	3	O	24.576-MHz crystal

2 Functional Description

2.1 Analog Input/Output Ports

2.1.1 Analog Outputs

The TLC320AD91C mixer generates the following two distinct audio outputs:

- A stereo mix of all sources for output to the speakers, headset, and LINOP output
- A mono, mic only, or mix of all sources (except PHONE and PCBEEP) for speakerphone output (MONOP)

2.1.2 Analog Inputs

The TLC320AD91C supports all analog audio inputs required by the audio codec ‘97 (AC‘97) specification. Specifically, the device supports the playback and record of all digital and analog sources likely to be present in PCs. These sources include the following:

- System audio: digital PCM input and output for business, games, and multimedia
- CD: analog CD-ROM redbook audio with internal connections to codec mixer
- Mono microphone: choice of desktop or headset mic with programmable boost and gain
- Speakerphone: use of system mic and speakers for telephony, DSVD, and video conferencing
- Stereo line in: analog external line level source from consumer audio, video camera, etc
- Video: TV tuner or video capture card with internal connections to codec mixer
- Aux/synth: analog FM or wavetable synthesizer or other internal source

The analog inputs connect to a stereo analog mixer as well as a stereo multiplexer. The mixer is used for playback or analog pass-through. The multiplexer is used during record.

The multiplexer offers the capability to record any of the audio sources or the outgoing mix of all sources. The multiplexer implementation is more efficient than an independent mix and offers simple monitoring when a mix is recorded: what you hear is what you get. The mono and stereo mix also provides excellent echo cancellation reference signals.

The TLC320AD91C supports the following full range of input options (the audio driver may maintain a consistent record input level for each multiplexer option):

- Any mono or stereo source
- Mono or stereo mix of all sources
- Two-channel input with mono output reference (mic and stereo mix for stereo echo cancellation)

2.2 Digital Interface

The TLC320AD91C, per the AC‘97 specification, incorporates a 5-wire serial digital interface to a digital controller. The AC-Link specifies a bidirectional, fixed rate, serial PCM digital stream. The interface handles multiple input and output audio streams, as well as control register accesses by employing a time division multiplexed (TDM) protocol.

The AC-Link architecture divides each audio frame into 12 outgoing and 12 incoming data streams, each with 20-bit sample resolution.

The TLC320AD91C data streams, per the AC‘97 specification, are the following:

- PCM playback has two output slots with a two-channel composite PCM output stream
- PCM record has two input slots with a two-channel composite PCM input stream
- Control has two output slots with a Control register write port
- Status has two input slots with a Control register read port
- Additional data streams are defined in the AC‘97 specification but their functionality is not implemented in the TLC320AD91C

The AC‘97 audio frame is shown in Figure 2–1.

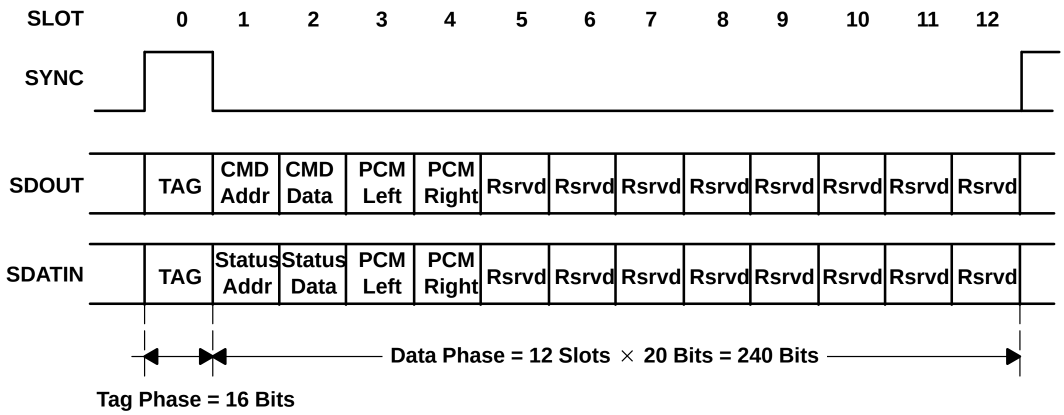


Figure 2–1. AC-Link Bidirectional Audio Frame (As Implemented)

2.2.1 AC-Link Signal Definitions

The AC-Link signals are shown in Figure 2–2.

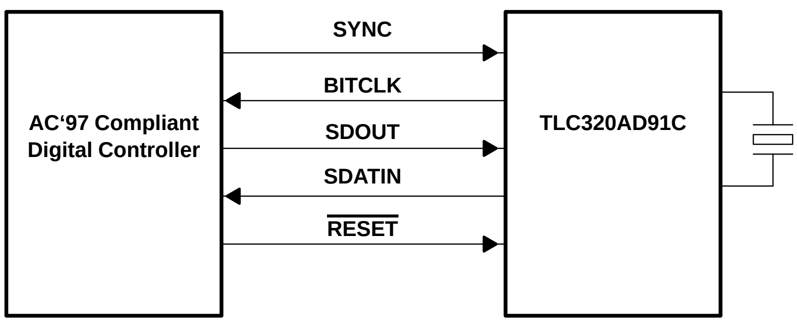


Figure 2–2. AC-Link Signals

The AC-Link signal definitions are listed in Table 2–1.

Table 2–1. AC-Link Signal Definitions

SIGNAL	SOURCE	DESCRIPTION
SYNC	Controller	Marks the beginning of each frame. Sourced by the controller. Occurs at a fixed rate of 48 kHz unless in power-down mode. Synchronous to BITCLK. Width of 18 bits. Defines the TAG phase.
BITCLK	Codec	Sourced by TLC320AD91C. Fixed rate of 12.288 MHz. One bit is transmitted on every rising edge. One bit is captured on every falling edge.
SDOUT	Controller	Serial bit stream sent from the controller to the codec. Data and control are transmitted by the controller.
SDATIN	Codec	Serial bit stream sent from the codec to the controller. Data and control are transmitted by the TLC320AD91C.
$\overline{\text{RESET}}$	Controller	Reset signal used to bring the TLC320AD91C out of power-down mode. Defines the cold TLC320AD91C reset.

2.2.2 Protocol

The TLC320AD91C protocol includes the following:

- The AC-Link is a TDM serial interface consisting of 256 bits/frame.
- Each frame is divided into two sections: A TAG phase of 18 bits, and a DATA phase of 240 bits.
- The DATA phase is divided into 12 time slots with each time slot consisting of 20 bits.
- Data is bidirectional with SDOUT transmitted by the controller, and SDATIN transmitted by the codec.

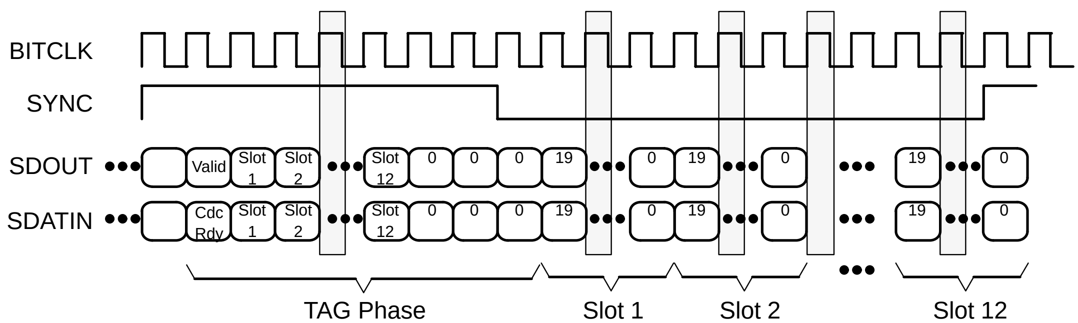


Figure 2–3. AC-Link Protocol

2.2.2.1 Zero-Padding

The TLC320AD91C uses zero-padding which is defined as the following:

- Reserved time-slots are filled with zeroes.
- Unused bits within a time-slot must be filled with zeroes (e.g., 18-bit converter in a 20-bit time slot). This operation must be performed by the source (i.e., the controller for SDOUT, the TLC320AD91C for SDATIN).
- Time slots tagged as invalid must be filled with zeroes.

2.2.2.2 SYNC

The TLC320AD91C SYNC signal includes the following characteristics:

- SYNC is driven by the controller.
- SYNC is derived by dividing down the BITCLK signal (BITCLK is an input to the controller).
- SYNC is high for 18 BITCLKs at the beginning of each frame. These 18 BITCLKs (bits) define the TAG phase. The TAG phase defines the beginning of a frame.
- The TLC320AD91C synchronizes data conversion with the rising edge of SYNC.
- SYNC remains low for the next 240 BITCLKs. These 240 BITCLKs (bits) define the DATA phase.
- SYNC is sampled by TLC320AD91C at the falling edge of BITCLK.
- SYNC transition edges are on the rising edge of BITCLK.
- The controller must hold SYNC low during a TLC320AD91C power-down halted state.

2.2.2.3 BITCLK

The TLC320AD91C BITCLK signal includes the following characteristics:

- BITCLK is fixed at 12.288 MHz (256 $\times$ sampling rate). The sampling rate is fixed at 48 kHz.
- BITCLK is sourced by the TLC320AD91C.
- BITCLK goes low and remains low when a write to register 26h with PR4 is detected (power-down state).
- BITCLK becomes active from a power-down state in response to a cold or warm TLC320AD91C reset condition.

2.2.2.4 SDOUT

The TLC320AD91C SDOUT signal includes the following characteristics:

- SDOUT is driven by the controller.
- SDOUT transitions on the rising edge of BITCLK.
- SDOUT is captured by the TLC320AD91C on the falling edge of BITCLK.
- The controller must hold SDOUT low during an TLC320AD91C power-down halted state.

2.2.2.5 SDATIN

The TLC320AD91C SDATIN signal includes the following characteristics:

- SDATIN is driven by the TLC320AD91C.
- SDATIN transitions on the rising edge of BITCLK.
- SDATIN is captured by the controller on the falling edge of BITCLK.
- SDATIN goes low and remains low when a write to register 26h with PR4 is detected (power-down state).
- SDATIN becomes active from a power-down state in response to a cold or warm TLC320AD91C reset condition.

2.2.3 Frame Contents

The SDOUT frame contents are listed in Table 2–2.

Table 2–2. SDOUT Frame Contents (Driven by Audio Controller)

SLOT	SLOT NAME	BIT POSITION	NAME	DESCRIPTION
0	TAG	15	Valid Frame	0: Indicates no valid data is in this frame 1: There is at least one TDM slot containing valid data in the frame.
		14	Slot 1 Valid	0: Indicates no data is available in the first time slot of the data phase. Slot one must be zero-padded. 1: Valid data is available in the first time slot.
		13–3	Slot x Valid	0: No valid data is in slot x of the data phase. The corresponding slot must be zero-padded. 1: Valid data is in slot x
		2–0	Zero Pad	Reserved. Must be zeroes.
1	Command Address	19	Read/Write	0: Write to the addressed register 1: Read from the addressed register
		18–12	Register Index	These seven bits are used to access the control registers. Only the even numbers are used. A total of 64 registers are defined. Odd numbered register accesses map to the preceding even boundary.
		11–0	Zero Pad	Reserved. Must be zeroes.
2	Command Data	19–4	Register Data	If the current command operation is a write (see bit 19 of slot one) then these bits contain the data to be written. These bits must be zero-padded if the current operation is a read.
		3–0	Zero Pad	Reserved. Must be zeroes.
3	PCM Left Playback	19–4	PCM Data	18-bit audio data. If the resolution is less than 18 bits, then the data must be right-justified and the LSBs must be zero-padded.
		3–0	Zero Pad	These bits must be zeroes.
4	PCM Right Playback	19–4	PCM Data	18-bit audio data. If the resolution is less than 18 bits, then the data must be right-justified and the LSBs must be zero-padded.
		3–0	Zero Pad	These bits must be zeroes.
5–12	Reserved		Zero Pad	Reserved. These bits must be zeroes. Note that slot five is the optional modem line codec.

The SDATIN frame contents are listed in Table 2–3.

Table 2–3. SDATIN Frame Contents

SLOT	SLOT NAME	BIT POSITION	NAME	DESCRIPTION
0	TAG	15	Codec Ready	0: Indicates the TLC320AD91C codec is not ready. 1: Indicates the TLC320AD91C control and status registers are available and the AC-Link is operational. The audio controller can then probe further to determine when other sections become available.
		14	Slot 1 Valid	0: Indicates no data is available in the first time slot of the data phase. Slot one must be zero-padded. 1: Valid data is available in the first time slot if the codec is ready.
		13–3	Slot x Valid	0: No valid data is in slot x of the data phase. The corresponding slot must be zero-padded. 1: Valid data is in slot x if the codec is ready.
		2–0	Zero Pad	Reserved. Must be zeroes.
1	Status Address	19	Zero Pad	Reserved. Must be zero.
		18–12	Register Index	These seven bits are used to echo the control register address. The data appears in the next slot (slot two). These bits must be zero-padded if this slot is flagged invalid during the TAG phase.
		11–0	Zero Pad	Reserved. Must be zeroes.
2	Status Data	19–4	Register Data	Contents of the register addressed by slot one (status address). These bits must be zero-padded if this slot is flagged invalid during the TAG phase.
		3–0	Zero Pad	These bits are zeroes.
3	PCM Left Record	19–4	PCM Data	18-bit audio data.
		3–0	Zero Pad	These bits must be zeroes.
4	PCM Right Record	19–4	PCM Data	18-bit audio data.
		3–0	Zero Pad	These bits are zeroes.
5–12	Reserved		Zero Pad	Reserved. These bits must be zeroes. Note that slot five is the optional modem line codec, and slot six is the optional microphone ADC record data.

2.2.4 AC-Link Low-Power Mode

The TLC320AD91C implementation of the AC-Link can be placed in a low-power mode (see Section 2.7, *Power-Down Management*). When the TLC320AD91C Power Down register (26h) is programmed to the appropriate value, both BITCLK and SDATIN are brought to and held at low-voltage logic levels.

As shown in Figure 2–4, BITCLK and SDATIN are transmitted low immediately following the decode of the write to the Power Down Register (26h) with PR4. When the digital controller driver is at the point where it is ready to program the TLC320AD91C into its low-power mode, slots one and two are assumed to be the only valid stream in the audio output frame. (At this point, all sources of audio input are assumed to have also been neutralized.)

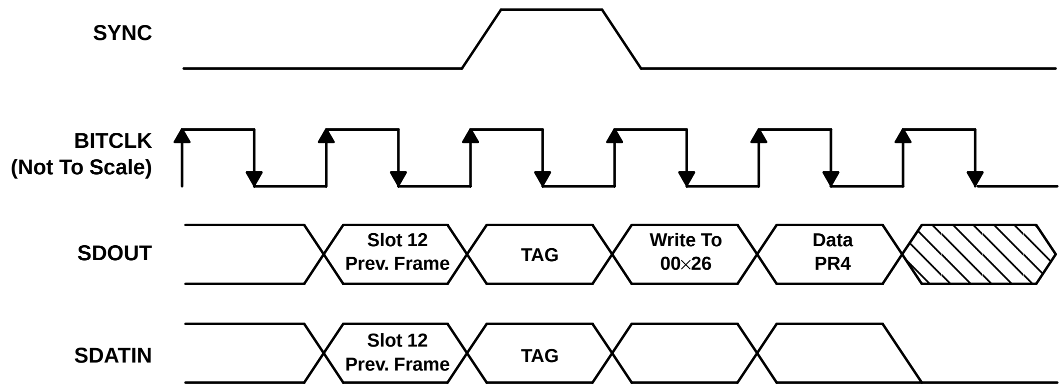


Figure 2–4. TLC320AD91C Power-Down Mode Timing

The digital controller must also drive SYNC and SDOUT low after programming the TLC320AD91C to this low-power halted mode.

Once the TLC320AD91C has been instructed to halt BITCLK, a special wake-up protocol must be used to bring the AC-Link to the active mode since normal audio output and input frames cannot be communicated in the absence of BITCLK.

The AC-Link can be made active again by means of a warm reset or a cold reset. See Section 2.5, *Resetting the TLC320AD91C* for details on the procedure. In summary, a warm reset is accomplished by asserting SYNC in the absence of BITCLK. The TLC320AD91C responds according to the protocol. A warm reset retains the values programmed into the registers. A cold reset is accomplished by asserting $\overline{\text{RESET}}$. Again, the TLC320AD91C responds according to the protocol. A cold reset sets all register values to their default values. Note that for both cases of a reset, the signals $\overline{\text{RESET}}$ and SYNC are treated as asynchronous inputs.

2.3 Software Interface

The register indexes and usage are shown in Table 2–4. All registers not shown are assumed to be reserved.

Table 2–4. TLC320AD91C Register Definitions

INDEX	NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
00h	Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h
02h	Play Master Volume Stereo	Mute	0	ML5‡	ML4	ML3	ML2	ML1	ML0	0	0	MR5‡	MR4	MR3	MR2	MR1	MR0	8000h
04h†	Headphone Volume	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h
06h	Play Master Volume Mono	Mute	0	0	0	0	0	0	0	0	0	MM5‡	MM4	MM3	MM2	MM1	MM0	8000h
08h†	Master Tone (not used)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h
0Ah	PCBEEP Volume	Mute	0	0	0	0	0	0	0	0	0	0	PV3	PV2	PV1	PV0	0	8000h
0Ch	Phone Volume	Mute	0	0	0	0	0	0	0	0	0	GN5‡	GN4	GN3	GN2	GN1	GN0	8008h
0Eh	Mic Volume	Mute	0	0	0	0	0	0	0	0	20dB	GN5‡	GN4	GN3	GN2	GN1	GN0	8008h
10h	Line In Volume	Mute	0	0	GL4	GL3	GL2	GL1	GL0	0	0	0	GR4	GR3	GR2	GR1	GR0	8808h
12h	CD Volume	Mute	0	0	GL4	GL3	GL2	GL1	GL0	0	0	0	GR4	GR3	GR2	GR1	GR0	8808h
14h	Video Volume	Mute	0	0	GL4	GL3	GL2	GL1	GL0	0	0	0	GR4	GR3	GR2	GR1	GR0	8808h
16h	Aux Volume	Mute	0	0	GL4	GL3	GL2	GL1	GL0	0	0	0	GR4	GR3	GR2	GR1	GR0	8808h
18h	PCM Out Volume	Mute	0	0	GL4	GL3	GL2	GL1	GL0	0	0	0	GR4	GR3	GR2	GR1	GR0	8808h

† Optional AC'97 registers whose functionality are not implemented on the TLC320AD91C. These registers can be written to, but reads always return zeroes.
‡ Special function volume settings. If bit is set, then the 5 volume bits implemented are set to all ones.
NOTE: All registers and all bits in all registers must have read back capabilities (be readable) to facilitate testing.

Table 2–4. TLC320AD91C Register Definitions (Continued)

INDEX	NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
1Ah	Record Select Control	0	0	0	0	0	SL2	SL1	SL0	0	0	0	0	0	SR2	SR1	SR0	0000h
1Ch	Record Gain	Mute	0	0	0	GL3	GL2	GL1	GL0	0	0	0	0	GR3	GR2	GR1	GR0	8000h
1Eh†	Record Gain Mic	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h
20h	General Purpose	0	ST	3D	1D	0	0	MIX	MS	LPBK	0	0	0	0	0	0	0	0000h
22h†	3D Control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h
24h†	Modem Rate (Not Used)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h
26h	Power-Down Control/ Status	PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0	0	0	0	MDM	REF	ANL	DAC	ADC	na
28h–59h	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5Ah–7Ah	Vendor Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	5458h
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	0000h

† Optional AC‘97 registers whose functionality are not implemented on the TLC320AD91C. These registers can be written to, but reads always return zeroes.
‡ Special function volume settings. If bit is set, then the 5 volume bits implemented are set to all ones.
NOTE: All registers and all bits in all registers must have read back capabilities (be readable) to facilitate testing.

2.3.1 Reset Register (Index 00h)

A write of any value to the Reset register performs a register reset, which causes all of the registers to revert to their default values. A read of this register returns the ID code of the TLC320AD91C and the type of 3D enhancement, if installed.

Both DACs operate at 18-bit resolution, and both ADCs operate at 18-bit resolution.

The ID decodes the capabilities of the TLC320AD91C based on the definitions listed in Table 2–5.

Table 2–5. Reset Register ID Bit Definitions

ALL BITS = 0	FUNCTION
ID0	Dedicated mic PCM channel
ID1	Modem line codec support
ID2	Bass and treble control
ID3	Simulated stereo (mono to stereo)
ID4	Headphone out support
ID5	Loudness (bass boost) support
ID6	18-bit DAC resolution
ID7	20-bit DAC resolution
ID8	18-bit ADC resolution
ID9	20-bit ADC resolution

2.3.2 Play Master Volume Stereo and Mono Registers (Index 02h and 06h)

The Play Master Volume registers manage output signal volumes. Register 02h controls the stereo master volume (both right and left channels). Register 06h controls the mono volume output. Each step corresponds to 1.5 dB. ML5 through ML0 is for the left channel level. MR5 through MR0 is for the right channel level. MM5 through MM0 is for the mono out channel.

The MSB is the mute bit and is supported in the TLC320AD91C. When this bit is set to 1, the level for that channel is set at maximum attenuation.

The default value of these registers is 8000h (1000 0000 0000 0000) which corresponds to 0-dB attenuation with mute on. The Play Master Volume register definitions are listed in Table 2–6.

Table 2–6. Play Master Volume Register Definitions

MUTE	Mx5 – Mx0	FUNCTION
0	00 0000	0-dB Attenuation
	...	...
	01 1111	46.5-dB Attenuation
1	xx xxxx	Maximum attenuation (mute)

2.3.3 PCBEEP Volume Register (Index 0Ah)

The PCBEEP Volume register controls the level of the PCBEEP input. Each step corresponds to 3 dB of attenuation. The MSB of the register is the mute bit. When this bit is set to 1, the level for the channel is set at maximum attenuation.

NOTE:

Power-on self-test (POST) codes need to be heard by the user when a hardware problem with the PC exists, even when the TLC320AD91C is in a reset state. Therefore, PCBEEP is routed to the left and right line outputs (a high-impedance path to the outputs is used with no attenuation).

The default value of this register is 8000h which corresponds to maximum attenuation with mute on. The PCBEEP register definitions are listed in Table 2–7.

Table 2–7. PCBEEP Register Definitions

MUTE	PV3 – PV0	FUNCTION
0	0000	0-dB Attenuation
	...	...
	1111	45-dB Attenuation
1	xxxx	Maximum attenuation (mute)

2.3.4 Analog Mixer Input Gain Registers (Index 0Ch – 18h)

The Analog Mixer Input Gain registers (Phone Volume, Mic Volume, Line In Volume, CD Volume, Video Volume, Aux Volume, PCM Out Volume) control the gain and attenuation for each of the analog inputs except PCBEEP. Each step corresponds to approximately 1.5 dB. The MSB of each register is the mute bit. When this bit is set to 1, the level for that channel is set at maximum attenuation.

Register 0Eh (Mic Volume register) has an extra bit for a 20-dB boost. When bit D6 is set to 1, the 20-dB boost is on. The default value of this register is 8008h which corresponds to 0-dB gain with mute on.

The default value for the mono (Phone Volume, Mic Volume) registers is 8008h which corresponds to 0-dB gain with mute on. The default value for the stereo registers is 8808h which corresponds to 0-dB gain with mute on. The Analog Mixer Input Gain register definitions are listed in Table 2–8.

Table 2–8. Analog Mixer Input Gain Register Definitions

MUTE	Gx4 – Gx0	FUNCTION
0	0 0000	12-dB Gain
	...	...
	0 1000	0-dB Gain
	...	...
	1 1111	–34.5-dB Gain
1	x xxxx	Maximum attenuation (mute)

2.3.5 Record Select Control Register (Index 1Ah)

The Record Select Control registers are used to select the record source, independently, for the right and left channels. See Tables 2–9 and 2–10 for the legend.

The default value of this register is 0000h which corresponds to MIC_IN. The Record Select Control register definitions are listed in Tables 2–9 and 2–10.

Table 2–9. Right Record Select Control Register Definitions

SR2 – SR0	RIGHT RECORD SOURCE
000	MIC_IN
001	CDR
010	VIDEO_R
011	AUXR
100	LINER
101	Stereo Mix (R)
110	Mono Mix (R)
111	PHONE

Table 2–10. Left Record Select Control Register Definitions

SL2 – SL0	LEFT RECORD SOURCE
000	MIC_IN
001	CDL
010	VIDEO_IN_L
011	AUXL
100	LINEL
101	Stereo Mix (L)
110	Mono Mix (L)
111	PHONE

2.3.6 Record Gain Register (Index 1Ch)

The Record Gain register is for the stereo input. Each step corresponds to 1.5 dB with 22.5 dB corresponding to 0F0Fh. The MSB of the register is the mute bit. When this bit is set to 1, the level for that channel is set to maximum attenuation.

The default value of this register is 8000h which represents 0-dB gain with mute on. The Record Gain register definitions are listed in Tables 2–11.

Table 2–11. Record Gain Register Definitions

MUTE	Gx3 – Gx0	FUNCTION
0	1111	22.5-dB Gain
	...	...
	0000	0-dB Gain
1	xxxx	Maximum attenuation (mute)

2.3.7 General-Purpose Register (Index 20h)

The General-Purpose register is used to control several miscellaneous functions of the TLC320AD91C: microphone output select, microphone select, and loopback.

This register should be read before writing to generate a mask for only the bit(s) that need to be changed.

The default value of this register is 0000h. The General-Purpose register definitions are listed in Table 2–12.

Table 2–12. General-Purpose Register Definitions

BIT	FUNCTION
MIX	Mono select. 0 = Mix, 1 = Mic
MS	Mic select. 0 = MIC1, 1 = MIC2
LPBK	ADC/DAC loopback mode. 0: Off 1: Enables loopback of the ADC output to the DAC input without involving the AC-Link thus allowing for full system performance measurements.

2.3.8 Power-Down Control/Status Register (Index 26h)

The Power-Down Control/Status register is a read/write register used to program power-down states and monitor subsystem readiness. The lower half of this register is read-only status with a one indicating that the subsection is ready. Ready is defined as the subsection that is able to perform in its nominal state. When this register is written, the bit values received on the AC-link have no effect on read-only bits 0–7.

When the AC-Link Codec Ready indicator bit (SDATIN, slot 0, bit 15) is a one, the AC-link and TLC320AD91C control and status registers are in a fully operational state. The digital controller must further probe this Power-Down Control/Status register to determine which subsections, if any, are ready. The Power-Down Control/Status register bits D0–D3 definitions are listed in Table 2–13.

Table 2–13. Power-Down Control/Status Register Bits D0–D3 Definitions

BIT	FUNCTION
REF	V_{ref} is up to nominal level
ANL	Analog mixers, etc. ready
DAC	DAC section ready
ADC	ADC section ready

The power-down modes include the following:

- The first three bits (PR0–PR2) are to be used individually rather than in combination with each other.
- The last bit, PR3 can be used with PR2 or by itself.
- PR0 and PR1 control the PCM ADCs and DACs only.

The Power-Down Control/Status register bits D8–D13 definitions are listed in Table 2–14.

Table 2–14. Power-Down Control/Status Register Bits D8–D13 Definitions

BIT	FUNCTION (SEE NOTE 1)
PR0	PCM in ADCs and input mux power down
PR1	PCM out DACs power down
PR2	Analog mixer power down (V_{ref} on)
PR3	Analog mixer power down (V_{ref} off)
PR4	Digital interface (AC-Link) power down (external clock off)
PR5	Internal clock disabled

NOTE 1: PR6 and PR7 are specified in the AC‘97 specification, but are not implemented in TLC320AD91C. These bits are read back as zeros.

2.3.9 Reserved Registers (Index 28h – 59h)

These registers are reserved. Write operations should not be performed to these registers.

2.3.10 Vendor Reserved Registers (Index 5Ah – 7Ah)

The Vendor Reserved registers are reserved for future use and are vendor specific. The TLC320AD91C register positions are allocated in the architecture but all bits are permanently set to zero.

A write operation to any of the Vendor Reserved registers has no effect. A read operation of any of these registers, except for index 5Ah, produces all zero values.

2.3.11 Vendor ID Registers (Index 7Ch – 7Eh)

The Vendor ID registers are for specific vendor identification, if so desired. The ID method is the Microsoft Plug and Play™ vendor ID code with F7 – F0 containing the first character of that ID, S7 – S0 containing the second ID character, and T7 – T0 containing the third ID character. These three characters are ASCII encoded. The REV7 – REV0 field is for the vendor revision number.

Register 7Ch is hard coded with 5458h and register 7Eh is hard coded with 4E20h. Only these values are read from these registers.

2.4 Clocking

The TLC320AD91C codec derives its clock from an external 24.576-MHz crystal. The codec drives a buffered and divided down (1/2) clock to the digital controller over the AC-Link on BIT_CLK. The frequency of this clock is 12.288 Mhz. (An external oscillator can be used; however, a crystal may yield more stable operation.) See Figure 2–5 and Figure 2–6 for the clock connection options.

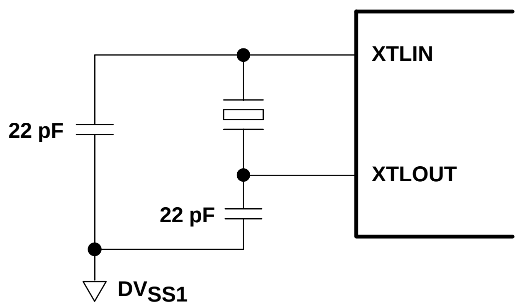


Figure 2–5. Crystal Configuration

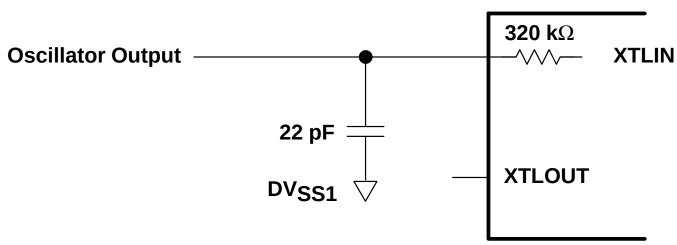


Figure 2–6. External Oscillator Configuration

If an external oscillator is used, it must be filtered with a 22-pF capacitor.

Clock jitter at the data converters (DACs and ADCs) is a fundamental impediment to high-quality performance. The internally generated clock provides the TLC320AD91C with a clean clock that is independent of the physical proximity of the digital controller.

The beginning of all audio sample packets or audio frames transferred over the AC-link are synchronized to the rising edge of the SYNC signal. SYNC is driven by the controller. The controller receives the BITCLK input and generates SYNC by dividing BITCLK by 256 and applying conditioning to tailor the duty cycle. The result is a 48-kHz sample rate SYNC signal whose period defines an audio frame. Data is transferred out on every rising edge of BITCLK and subsequently sampled on the receiving side of the AC-Link on each immediately falling edge of BITCLK.

The audio data stream cannot be paused in record or playback since the codec does not contain data buffering capabilities.

2.5 Resetting the TLC320AD91C

The three types of TLC320AD91C resets include the following:

- A cold reset where all TLC320AD91C logic (registers included) is initialized to the default state. This reset is accomplished by asserting $\overline{\text{RESET}}$.
- A warm reset where the contents of the TLC320AD91C register set are left unaltered. This reset is accomplished by asserting SYNC during an AC-link power-down state.
- A register reset which only initializes the TLC320AD91C registers to their default states. See Section 2.3, *Software Interface*, register 0h.

After signaling a reset to the TLC320AD91C, the digital controller should not attempt to play or capture audio data until it has sampled a codec ready indication from the TLC320AD91C.

2.5.1 Cold Reset

A cold reset is achieved by asserting $\overline{\text{RESET}}$ for 1 µs. By driving $\overline{\text{RESET}}$ low, BIT_CLK and SDATA_OUT are activated, or reactivated, and all TLC320AD91C control registers are initialized to default power-on reset values.

$\overline{\text{RESET}}$ is an asynchronous input.

2.5.2 Warm Reset

The AC-link can be put in a low-power consumption state (see Section 2.3, *Software Interface*). In this state, all signals become inactive including BITCLK, and SYNC. A warm TLC320AD91C reset reactivates the AC-link without altering the current TLC320AD91C register values. A warm reset is signaled by driving SYNC high for a minimum of 1 µs in the absence of BITCLK.

Within normal audio frames, SYNC is a synchronous TLC320AD91C input. However, in the absence of BITCLK, SYNC is treated as an asynchronous input used in the generation of a warm reset to the TLC320AD91C.

The TLC320AD91C does not respond with the activation of BITCLK until SYNC has been sampled low again by the TLC320AD91C. This precludes the false detection of a new audio frame.

2.5.3 Reset From Test Mode

Once either of the two test modes have been entered, the TLC320AD91C must be issued another reset with all AC-link signals low to return to the normal operating mode.

2.6 Microphone Input Programmable Gain Amplifier

The TLC320AD91C is designed to allow most common microphones to be connected to it without the use of external preamplifiers. As shown in Figure 2–7, the microphone input multiplexer is followed by a buffer amplifier with 100-kΩ input impedance. This configuration allows the value of the input coupling capacitors to be kept small while maintaining acceptable low frequency response characteristics.

As shown in Figure 2–7, the reference output is designed to provide bias current for two microphones.

Figure 2–7 shows the connection of two electret microphones to the TLC320AD91C codec.

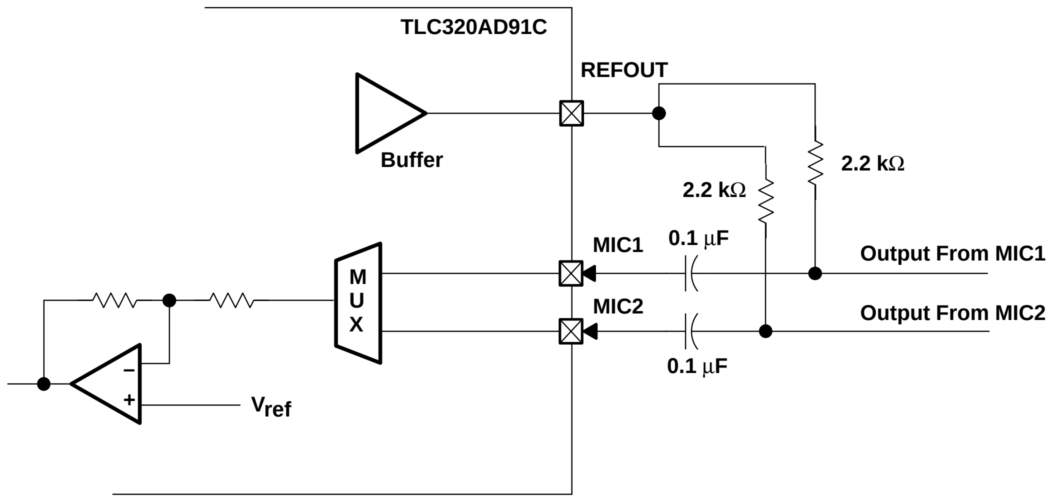


Figure 2–7. Microphone Programmable Gain Amplifier With Two Electret Microphones

2.7 Power-Down Management

The TLC320AD91C is capable of operating at reduced power when no activity is required. The state of power down is controlled by the Power Down register (Index 26h). There are seven commands of separate power down with the addition of modem codec. The TLC320AD91C is fully static and if the clock is stopped, the register values are not lost. Table 2–15 lists the different power-down modes.

Table 2–15. Power-Down Modes

BITS	FUNCTION
PR0	PCM in ADCs and input MUX power down
PR1	PCM out DACs power down
PR2	Analog mixer power down (V_{ref} on)
PR3	Analog mixer power down (V_{ref} off)
PR4	Digital interface (AC‘97) power down (external clock off)
PR5	Internal clock disabled

Figure 2–8 illustrates one example procedure for a complete power down of the TLC320AD91C. From normal operation, sequential writes to the General-Purpose register are performed to power down the TLC320AD91C one section at a time. After all of the other sections have been shut down, a final write (of PR4) can be executed to shut down the TLC320AD91C digital interface (AC-link). The device remains in sleep mode with all registers holding their static values. To wake up the TLC320AD91C, the digital controller sends a pulse on SYNC which issues a warm reset. This operation restarts the TLC320AD91C digital interface (resets PR4 to zero). The TLC320AD91C can also be awakened with a cold reset. A cold reset causes a loss of the register values since a cold reset sets the registers back to their default states. When a section is powered back on, the Power Down register (index 26h) should be read to verify that the section is ready (i.e., stable) before any operation that requires the section is attempted.

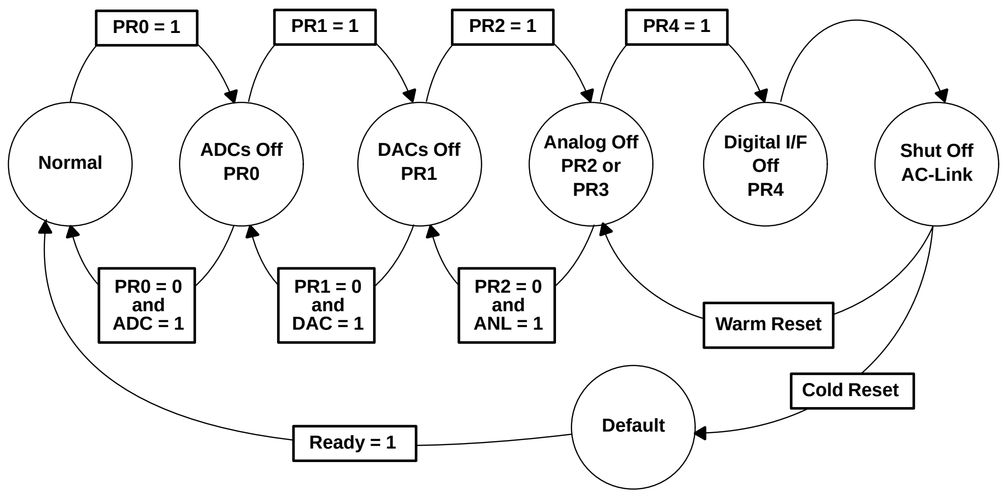


Figure 2–8. TLC320AD91C Power-Down/ Power-Up Flow Example

Figure 2–9 illustrates an example procedure where all of the mixers are operational with the static volume settings contained in their associated registers. This procedure is used when a CD is played (or external LINE source) through the TLC320AD91C to the speakers but most of the system is in low-power mode. This procedure follows the previous procedure, except that the analog mixer is never shut down.

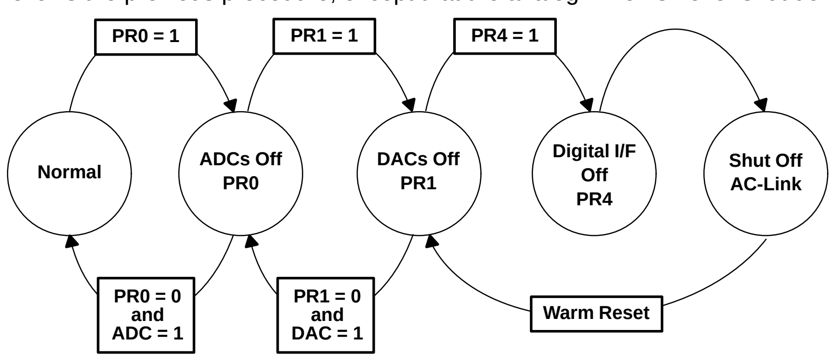


Figure 2–9. TLC320AD91C Power-Down/Power-Up Flow Example With Analog Still Alive

2.8 Mixer Functions

The TLC320AD91C mixer functions are listed in Table 2–16.

Table 2–16. TLC320AD91C Mixer Functions

SOURCE	SOURCE	CONNECTION
PCBEEP	PCBEEP pass through	From PC beeper output
PHONE	Speakerphone	From telephony subsystem
MIC1	Desktop microphone	From microphone jack
MIC2	Headset microphone	From headset microphone jack
LINE	External audio source	From line-in jack
CD	Audio from CD-ROM drive	CD audio left channel
VID	Audio from TV tuner or video camera	Cable from TV or video capture card
AUX	Upgrade synth or other source	Internal connector
SDOUT	Digital audio output from digital controller	AC-link
Mix out	Mix of all sources	TLC320AD91C internal connection
LINOP	Stereo mix of all sources	To output jack
MONOP	Mic or mix for speakerphone	To telephony subsystem
SDATIN	Digital audio input to digital controller	AC-link

3 Specifications

3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)†

Supply voltage range, AV_{DD} (see Note 1) . . . . –0.3 V to 7 V
Supply voltage range, DV_{DD} (see Note 2) . . . . –0.3 V to 7 V
Analog input voltage range (see Note 1) . . . . AV_{SS} –0.3 V to AV_{DD} + 0.3 V
Digital Input voltage range (see Note 2) . . . . DV_{SS} –0.3 V to DV_{DD} + 0.3 V
Operating free-air temperature range, T_A . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature from case for 10 seconds . . . . 240°C
Lead temperature from case for 2 minutes . . . . 183°C
ESD tolerance (see Note 3) . . . . 2000 V

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values for maximum ratings are with respect to AGND.
2. Voltage values for maximum ratings are with respect to DGND.
3. Human Body Model per Method 3015.2 of MIL–STD–883B.

3.2 Recommended Operating Conditions

	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Analog supply voltage, AV_{DD1}, AV_{DD2} (see Note 4)	3.3-V interface	3	3.3	3.6	V
	5-V interface	4.5	5	5.5	
Digital supply voltage, DV_{DD1}, DV_{DD2}	3.3-V interface	3	3.3	3.6	V
	5-V interface	4.5	5	5.5	V
Power supply offset voltage, DV_{SS} – AV_{SS} (see Note 4)		–0.3	0	0.3	V
Analog supply current			28		mA
Digital supply current			10		mA
Power supply rejection	20 Hz, 20 kHz		46		dB
Operating free-air temperature, T_A		0	25	70	°C

NOTE 4: Voltages at analog inputs and outputs and V_{SS} are with respect to the AGND terminal.

3.2.1 Static Digital Specifications, T_A = 25°C, $AV_{DD1} = AV_{DD2} = DV_{DD1}$ = 5 V ± 0.5 V, DV_{DD2} = 3.3 V ± 0.3 V

PARAMETER		MIN	MAX	UNIT
V_{IH}	High-level input voltage	2	DV_{DD}+0.3	V
V_{IL}	Low-level input voltage	–0.3	0.8	V
V_{OH}	High-level output voltage (I_O = –2 mA)	2.4	DV_{DD}	V
V_{OL}	Low-level output voltage (I_O = 2 mA)	DV_{SS}	0.4	V
	Input leakage current	–10	10	µA
	Output leakage current	–10	10	µA

3.3 Electrical Characteristics

3.3.1 Analog-to-Digital Converter, T_A = 25°C, $AV_{DD1} = AV_{DD2} = DV_{DD1} = DV_{DD2}$ = 5 V ± 0.5 V, f_s = 48 kHz, Gain Settings at 0 dB, Input = 1 V_{rms} Sine Wave at 1 kHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-noise ratio, A-weighted 1	Input = 0.9 V_{rms}	75	80		dB
Full-scale input voltage	0 dB, V_{ref} = 2.5 V		1		V_{rms}
Total harmonic distortion	–3-dB input		0.02		%
Frequency response		20		19 200	Hz
Transition band		19 200		28 800	Hz
Stop band		28 800			Hz
Stop band rejection		–74			dB
Power supply rejection ratio	20 Hz – 20 kHz		46		dB

3.3.2 Digital-to-Analog Converter, T_A = 25°C, $AV_{DD1} = AV_{DD2} = DV_{DD1} = DV_{DD2}$ = 5 V ± 0.5 V, f_s = 48 kHz, Gain Settings at 0 dB

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-noise ratio, A-weighted 1	Input = 0.9 V_{rms}	85	90		dB
Full-scale output voltage	0 dB, V_{ref} = 2.5 V		1		V_{rms}
Total harmonic distortion	–6-dB input		0.01		%
Frequency response		20		19 200	Hz
Transition band		19 200		28 800	Hz
Stop band		28 800			Hz
Out-of-band rejection			–40		dB
Spurious tone reduction			–100		dB
Power supply rejection ratio	20 Hz – 20 kHz		46		dB

3.3.3 Reference Specifications, $T_A = 25°C$, $AV_{DD1} = AV_{DD2} = DV_{DD1} = DV_{DD2} = 5\ V \pm 0.5\ V$, $f_S = 48\ kHz$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reference voltage, input/output	AFILT1		$2/5AV_{DD}$	$AV_{DD}/2$	$3/5AV_{DD}$	V
Reference voltage, output	AFILT2		$AV_{DD}/2–$ 100 mV	$AV_{DD}/2$	$AV_{DD}/2+$ 100 mV	V
	REFOUT			buffered VAFILT1		V
Reference voltage, mixer	REF			buffered VAFILT1		V
Reference voltage, ADC	CAP1			buffered VAFILT1		V
Reference voltage, DAC	CAP2			buffered VAFILT1		V
Current, sink	CAP1, CAP2, AFILT2, REF, and REFOUT			–5		mA
Current, source	CAP1, CAP2, REF, and REFOUT			5		mA
Voltage	AFILT1	V_{DD} = 4 V – 5.5 V nom		2.5		V
	AFILT2			1.5		V
Voltage, switch threshold	AFILT2		3.6	3.8		V
Impedance	AFILT1		75			kΩ

3.3.4 Circuit Specifications, T_A = 25°C, $AV_{DD1} = AV_{DD2} = DV_{DD1} = DV_{DD2}$ = 5 V ± 0.5 V, f_S = 48 kHz, For Gain Settings at 0 dB, Input = 1 V_{rms} Sine Wave at 1 kHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Mixer Circuit		V_{DD} = 5 V				
Signal-to-noise ratio	CD path A-weighted 1		90	95		dB
	Other paths A-weighted 1		85	95		
Maximum input voltage			AV_{SS}	1	AV_{DD}	Vrms
Maximum output voltage	LINOP			1		Vrms
Total harmonic distortion				0.02		%
Frequency response (±1 dB)			20		20 000	Hz
Input impedance	CD inputs	At any gain	10	20	30	kΩ
	Other mixer inputs	At maximum gain	10	20	30	
		At 0-dB gain	50	100	150	
	MIC inputs	At maximum gain	10	20	30	
		At 0-dB gain	55	110	165	
Power supply rejection ratio		20 Hz – 20 kHz		46		dB
Power Supply Monitor and Power On Reset (POR)						
POR threshold voltage			1.5	2.4	2.7	V

3.4 Timing Requirements

3.4.1 Device Timing Requirements, T_A = 25°C, $AV_{DD1} = AV_{DD2} = DV_{DD1} = DV_{DD2}$ = 5 V ± 0.5 V, f_S = 48 kHz, For Gain Settings at 0 dB, Input = 1 V_{rms} Sine Wave at 1 kHz

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
Clock Frequencies						
	Crystal clock frequency			24.576		MHz
	BITCLK frequency			12.288		MHz
	SYNC frequency			48		kHz
AC-Link Power Down Timing						
t_{d1}	Delay time, end of slot 2, SDATIN low, to BITCLK low				1	µs
Cold Reset Timing						
$t_{wL(RST)}$	Pulse duration, $\overline{\text{RESET}}$ active low		1			µs
$t_{d(RST\_CLK)}$	Delay time, startup, $\overline{\text{RESET}}$ inactive to BITCLK		162.8			ns
Warm Reset Timing						
$t_{wH(SYNC)}$	Pulse duration, SYNC active high			1.3		µs
$t_{d(SYNC\_CLK)}$	Delay time, SYNC inactive to BITCLK startup		162.8			ns
Clock Timing						
$t_{cyc(CLK)}$	Cycle time BITCLK			81.4		ns
	Output jitter, BITCLK			600		ps
$t_{wH(CLK)}$	Pulse duration, BITCLK high		32.56	40.7	48.84	ns
$t_{wL(CLK)}$	Pulse duration, BITCLK low		32.56	40.7	48.84	ns
$t_{cyc(SYNC)}$	Cycle time, SYNC			20.8		µs
$t_{wH(SYNC)}$	Pulse duration, SYNC high			1.3		µs
$t_{wL(SYNC)}$	Pulse duration, SYNC low			19.5		µs
Data Setup and Hold Timing						
t_{su1}	Setup time, falling edge of BITCLK		15			ns
t_{h1}	Hold time, falling edge of BITCLK		5			ns
Signal Rise and Fall Timing						
$t_{r(CLK)}$	Rise time, BITCLK		2		6	ns
$t_{f(CLK)}$	Fall time, BITCLK		2		6	ns
$t_{r(SYNC)}$	Rise time, SYNC		2		6	ns
$t_{f(SYNC)}$	Fall time, SYNC		2		6	ns
$t_{r(DIN)}$	Rise time, SDATIN		2		6	ns
$t_{f(DIN)}$	Fall time, SDATIN		2		6	ns
$t_{r(DOUT)}$	Rise time, SDOUT		2		6	ns
$t_{f(DOUT)}$	Fall time, SDOUT		2		6	ns

3.4.2 ATE Test Mode Timing Requirements, $T_A = 25°C$, $AV_{DD} = DV_{DD} = 5$ V dc, $AV_{SS} = DV_{SS} = 0$ V, 50-pF External Load

PARAMETER		MIN	TYP	MAX	UNIT
t_{su3}	Setup time, SDOUT↑, SYNC to $\overline{\text{RESET}}$↑ (see Notes 5 and 6)	15			ns
$t_{d(off)}$	Delay time, $\overline{\text{RESET}}$↑ to SDATIN, BITCLK Hi-Z (see Notes 5 and 6)			25	ns

NOTES: 5. All AC-link signals are normally low though $\overline{\text{RESET}}$↑. SDOUT should be high prior to $\overline{\text{RESET}}$↑ which causes the TLC320AD91C AC-link outputs to go high impedance which is suitable for ATE in circuit testing.

6. The Texas Instruments internal test mode is entered by bringing SYNC high prior to $\overline{\text{RESET}}$↑. This mode has no effect on the TLC320AD91C AC-link output signal levels.

4 Parameter Measurement Information

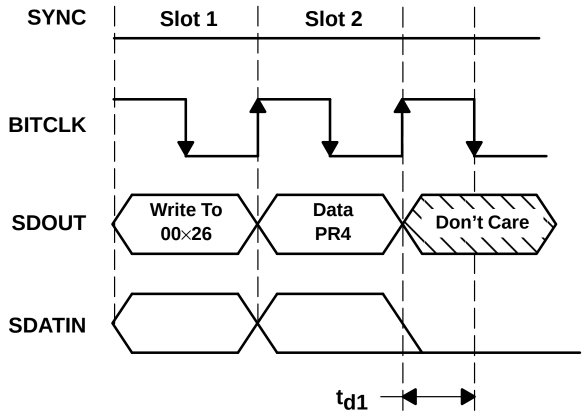


Figure 4–1. AC-Link Low-Power Mode Timing

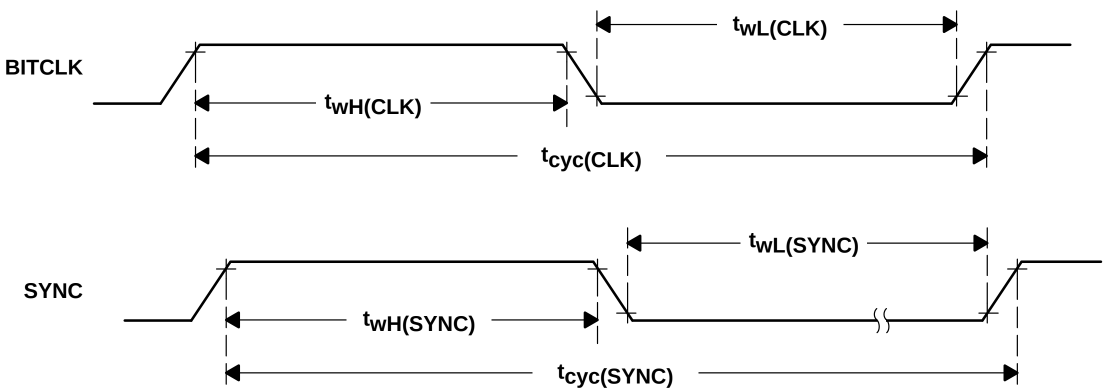


Figure 4–2. Clock Timing

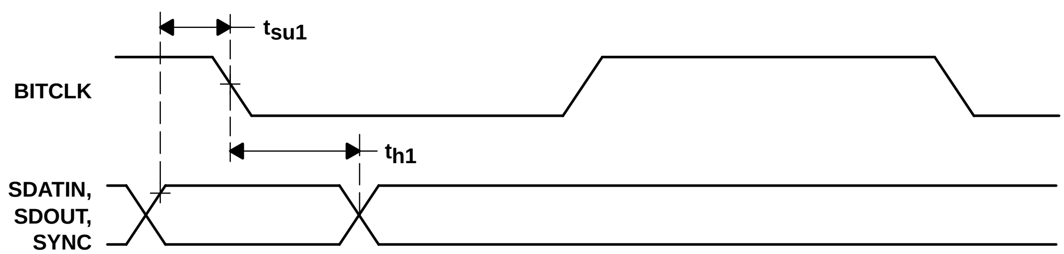


Figure 4–3. Data Setup and Hold Timing

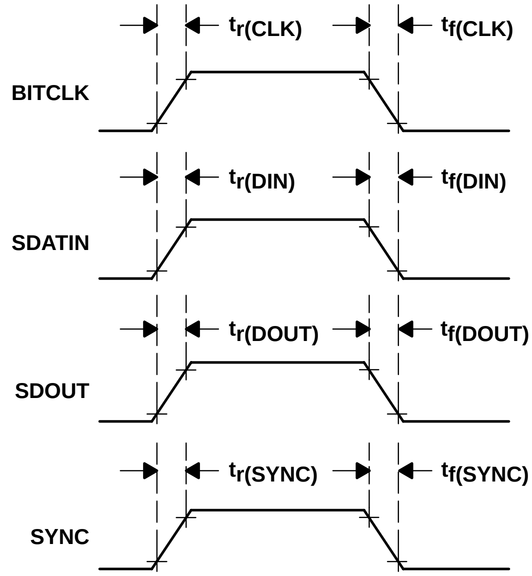


Figure 4–4. Signal Rise and Fall Timing

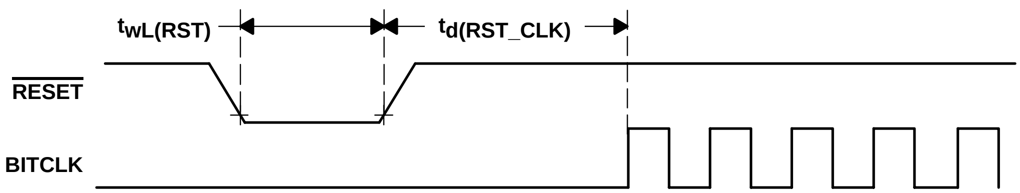


Figure 4–5. Cold Reset Timing

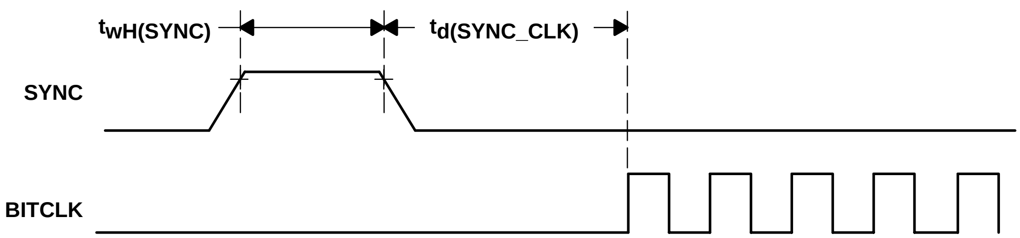


Figure 4–6. Warm Reset Timing

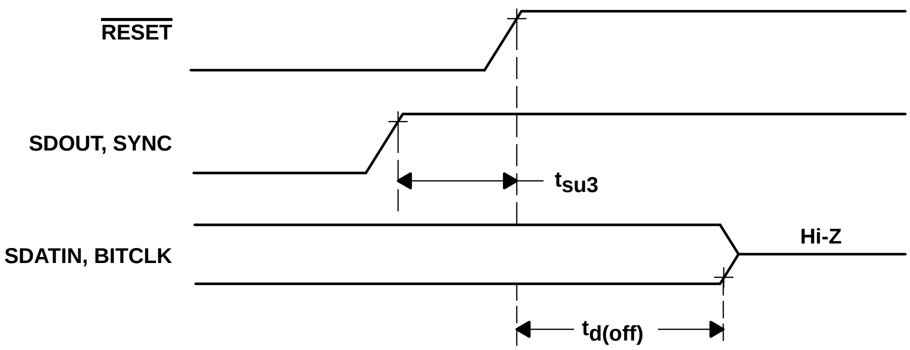


Figure 4–7. ATE Test Mode Timing

5 Application Information/System Usage

The system diagram in Figure 5–1 shows the essential components, including the TLC320AD91C, used in the design of a system. In this scenario, the TLC320AD91C operates at the fixed sample rate of 48 kHz and performs digital-to-analog conversion, analog-to-digital conversion, analog input, mixing, and allows for the insertion of analog and digital signal processing (3D sound, stereo enhancement, etc).

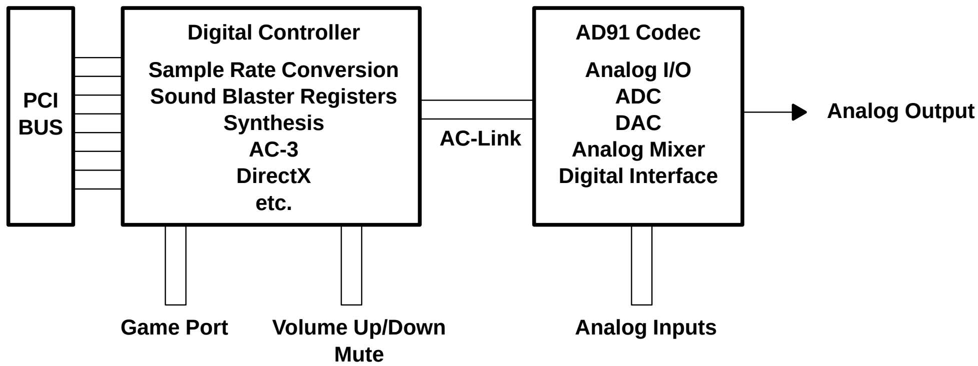


Figure 5–1. System Diagram

The digital controller, generally connected to the PCI bus, performs the following functions:

- Sample rate conversion to and from 48 kHz
- Sound Blaster compatibility
- FM synthesis
- Wave table synthesis
- Direct Sound acceleration (optional)
- AC-3 decode

The digital link is an AC‘97 compatible bidirectional, 5-wire, serial TDM format interface designed for a dedicated point-to-point interconnect on a circuit board.

5.1 Software Driver Support for the Texas Instruments TLC320AD91C Stereo Codec

The TLC320AD91C codec is compatible with software drivers developed to conform to the AC‘97 audio codec specification.

With the use of an AC‘97 compliant digital controller, the TLC320AD91C can perform high quality (90-dB SNR) sample rate conversions on a minimum of four simultaneous channels (stereo in and stereo out) and between a variety of sample rates. With the input sample rate at 48 kHz, data conversion to 8, 11.025, 16, 22.05, 32, and 44.1 kHz are possible.

Mono PCM always translates to two mono channels (L and R) on the AC‘97 AC-Link.

5.2 The Texas Instruments TLC320AD91C Connected to an AC‘97 Compliant Digital Controller

The TLC320AD91C communicates with an AC‘97 compliant digital controller through the digital serial link or AC-link. In addition to all digital audio streams, command and status information is also communicated over this point-to-point serial connection. This connection is shown in Figure 5–2.

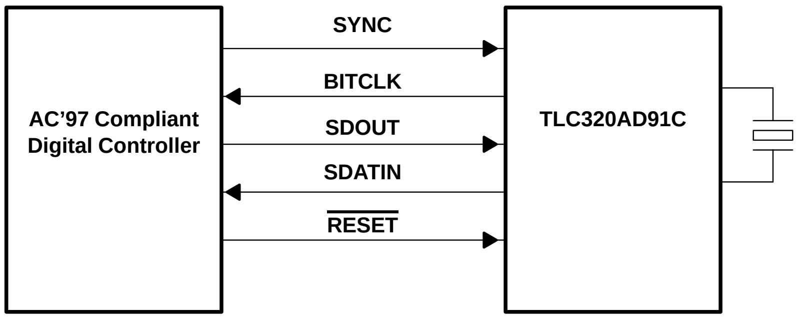


Figure 5–2. Connection to an AC‘97 Digital Controller

5.3 Testability

5.3.1 Activating the Test Modes

The TLC320AD91C has two test modes. One mode is for ATE in circuit test and the other mode is for Texas Instruments specific tests. The two test modes are activated according to the following:

- The TLC320AD91C enters the ATE in circuit test mode if SDATA_OUT is sampled high at the trailing edge of $\overline{\text{RESET}}$.
- The TLC320AD91C enters the Texas Instruments test mode when coming out of reset if SYNC is high.
- The TLC320AD91C enters Texas Instruments Scan Test mode when coming out of $\overline{\text{RESET}}$ when both SYNC and SDOUT are held high.

These cases should never occur during standard operating conditions.

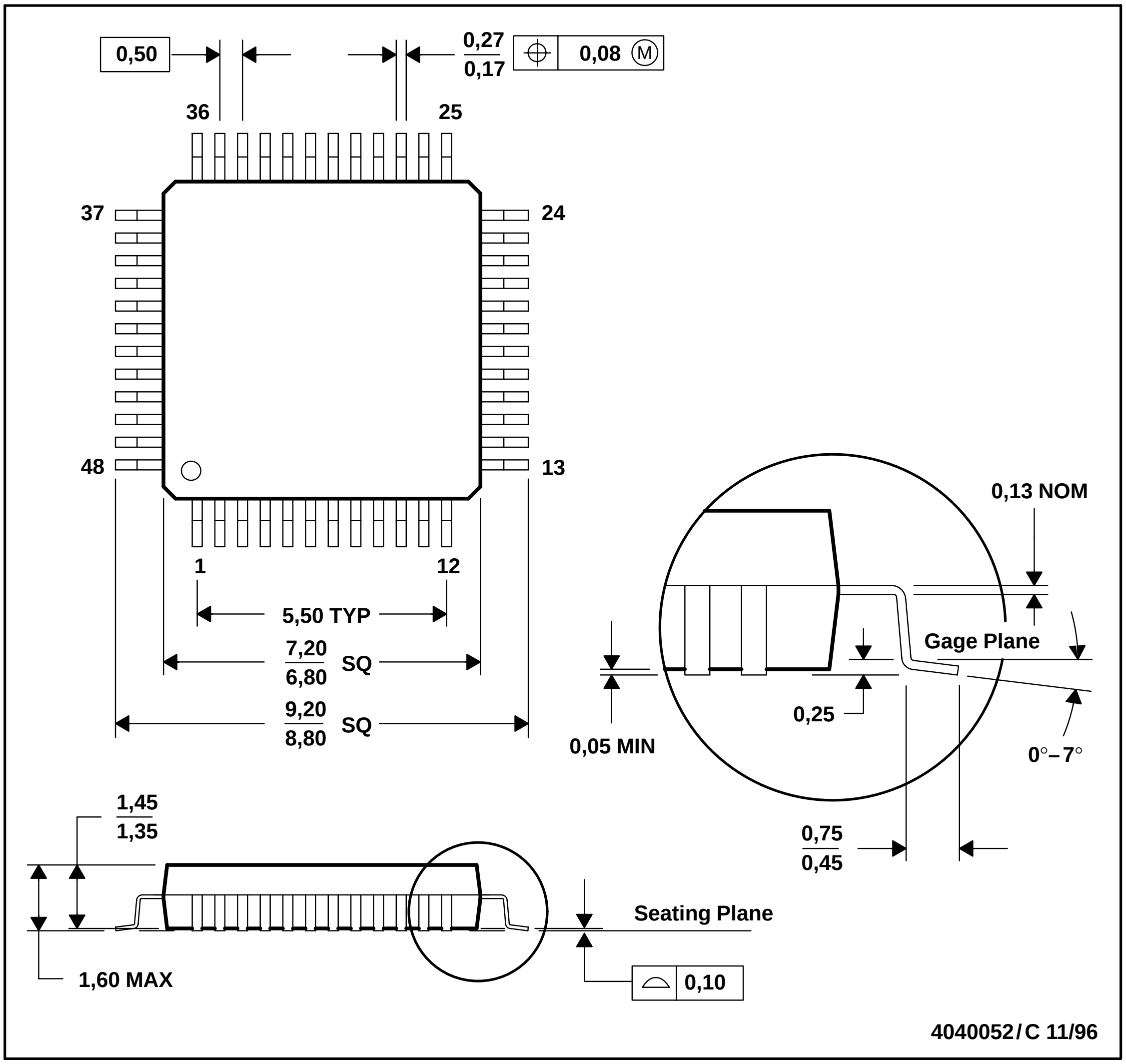
Regardless of the test mode, the digital controller must issue a cold reset to resume normal operation of the TLC320AD91C.

5.3.2 Test Mode Functions – ATE in Circuit Test Mode

When the TLC320AD91C is placed in the ATE test mode, the TLC32AD91C digital AC-Link outputs (i.e., BITCLK and SDATIN) are driven to a high-impedance state. This condition allows ATE in circuit testing of the digital controller.

Appendix A
Mechanical Data

PT (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. This may also be a thermally enhanced plastic package with leads conected to the die pads.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TLC320AD91CPT	OBSOLETE	LQFP	PT	48		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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