

**2592-pixel CCD Linear Image Sensor (B/W)**

**Description**

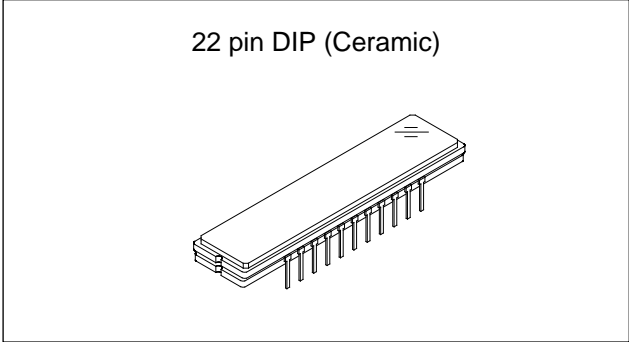
The ILX505A is a reduction type CCD linear sensor designed for facsimile, image scanner and OCR use. This sensor reads A3 size documents at a density of 200 DPI (Dot Per Inch). A built-in timing generator and clock-drivers ensure direct drive at 5V logic for easy use.

**Features**

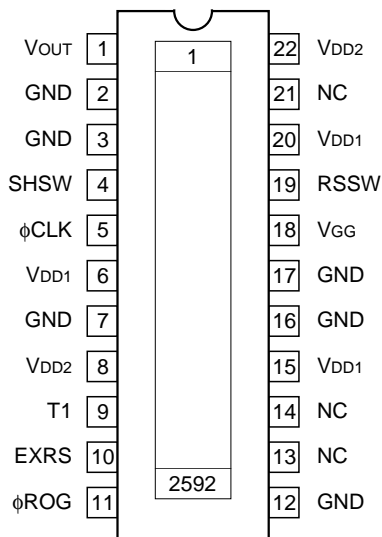
- Number of effective pixels: 2592 pixels
- Pixel size: 11µm × 11µm (11µm pitch)
- Built-in timing generator and clock-drivers
- Ultra low lag
- High sensitivity
- Maximum clock frequency: 5MHz

**Absolute Maximum Ratings**

- Supply voltage  $V_{DD1}$  11 V  
 $V_{DD2}$  6 V
- Operating temperature -10 to +55 °C
- Storage temperature -30 to +80 °C

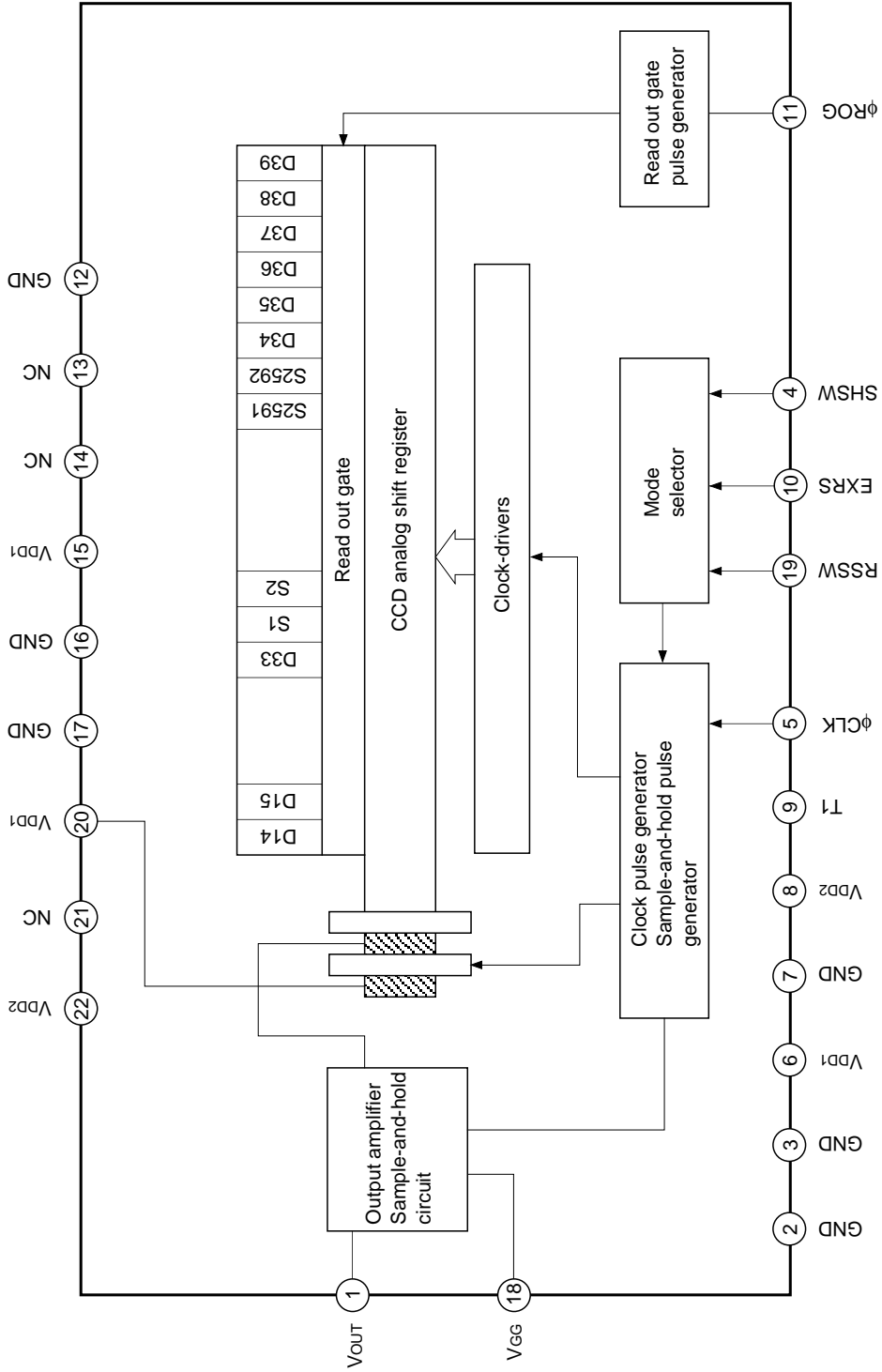


**Pin Configuration (Top View)**



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Block Diagram



## Pin Description

Pin No.	Symbol	Description
1	V <sub>OUT</sub>	Signal output
2	GND	GND
3	GND	GND
4	SHSW	Switch { with S/H → GND without S/H → V <sub>DD2</sub>
5	φCLK	Clock pulse
6	V <sub>DD1</sub>	9V power supply
7	GND	GND
8	V <sub>DD2</sub>	5V power supply
9	T1	Test pin (V <sub>DD2</sub> )
10	EXRS	External RS pulse input. Must be connected to V <sub>DD2</sub> when the internal RS pulse is used.
11	φROG	Clock pulse
12	GND	GND
13	NC	NC
14	NC	NC
15	V <sub>DD1</sub>	9V power supply
16	GND	GND
17	GND	GND
18	V <sub>GG</sub>	Output circuit gate bias
19	RSSW	Reset pulse switchover pin
20	V <sub>DD1</sub>	9V power supply
21	NC	NC
22	V <sub>DD2</sub>	5V power supply

**Mode Description**

Mode in Use	19 pin RSSW	10 pin EXRS
Internal RS	GND	V <sub>DD2</sub>
External RS	V <sub>DD2</sub>	φRS

**Note)** When the external RS mode is in use, operation of use internal S/H is not guaranteed. Pin 4 must be connected to 5V DC power supply.

**Recommended Voltage**

Item	Min.	Typ.	Max.	Unit
V <sub>DD1</sub>	8.5	9.0	9.5	V
V <sub>DD2</sub>	4.75	5.0	5.25	V

**Note)** Rules for raising and lowering power supply voltage

To raise power supply voltage, first raise V<sub>DD1</sub> (9V) and then V<sub>DD2</sub> (5V).

To lower voltage, first lower V<sub>DD2</sub> (5V) and then V<sub>DD1</sub> (9V).

**Electro-optical Characteristics**

(Ta = 25°C, VDD1 = 9V, VDD2 = 5V, Clock frequency: 1MHz,  
Light source = 3200K, IR cut filter: CM-500S (t = 1.0mm)),  
When Internal RS (Pin 19 = GND, Pin 10 = VDD2)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Sensitivity 1	R1	16.8	21	25.2	V/(lx · s)	Note 1
Sensitivity 2	R2	—	53	—	V/(lx · s)	Note 2
Sensitivity nonuniformity	PRNU	—	2.0	8.0	%	Note 3
Saturation output voltage	VSAT	1.5	1.8	—	V	—
Dark voltage average	VDRK	—	0.3	2.0	mV	Note 4
Dark signal nonuniformity	DSNU	—	0.5	3.0	mV	Note 4
Image lag	IL	—	0.02	—	%	Note 5
Dynamic range	DR	—	6000	—	—	Note 6
Saturation exposure	SE	—	0.085	—	lx · s	Note 7
9V supply current	IvDD1	—	14.0	20.0	mA	—
5V supply current	IvDD2	—	5.0	10.0	mA	—
Total transfer efficiency	TTE	92.0	97.0	—	%	—
Output impedance	Zo	—	600	—	Ω	—
Offset level	Vos	—	4.5	—	V	Note 8

**Notes)**

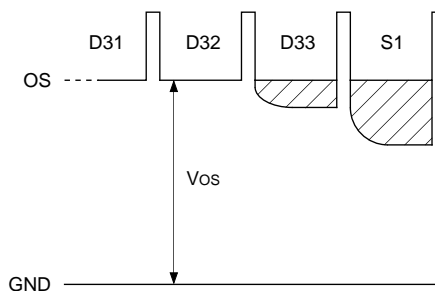
- 1) For the sensitivity test light is applied with a uniform intensity of illumination.
- 2) W lamp (2854K)
- 3) PRNU is defined as indicated below. Ray incidence conditions are the same as for Note 1.

$$PRNU = \frac{(V_{MAX} - V_{MIN})/2}{V_{AVE}} \times 100 [\%]$$

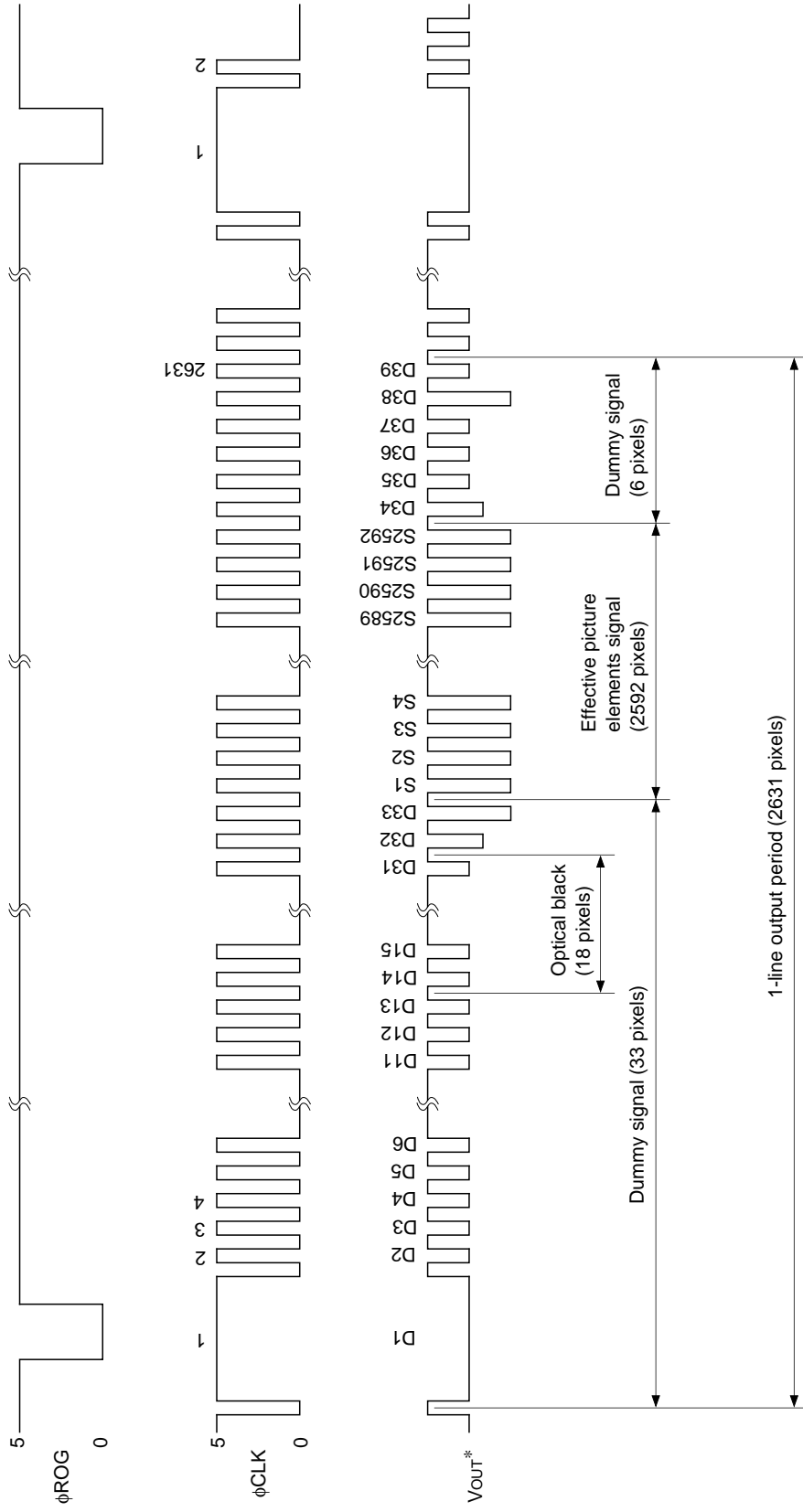
The maximum output of all the valid pixels is set to VMAX, the minimum output to VMIN and the average output to VAVE.

- 4) Integration time is 10ms.
- 5) VOUT = 500mV
- 6) DR = VSAT/VDRK
- 7) SE = VSAT/R1
- 8) Vos is defined as indicated below.

Signal is observed at PNP-type emitter follower out.

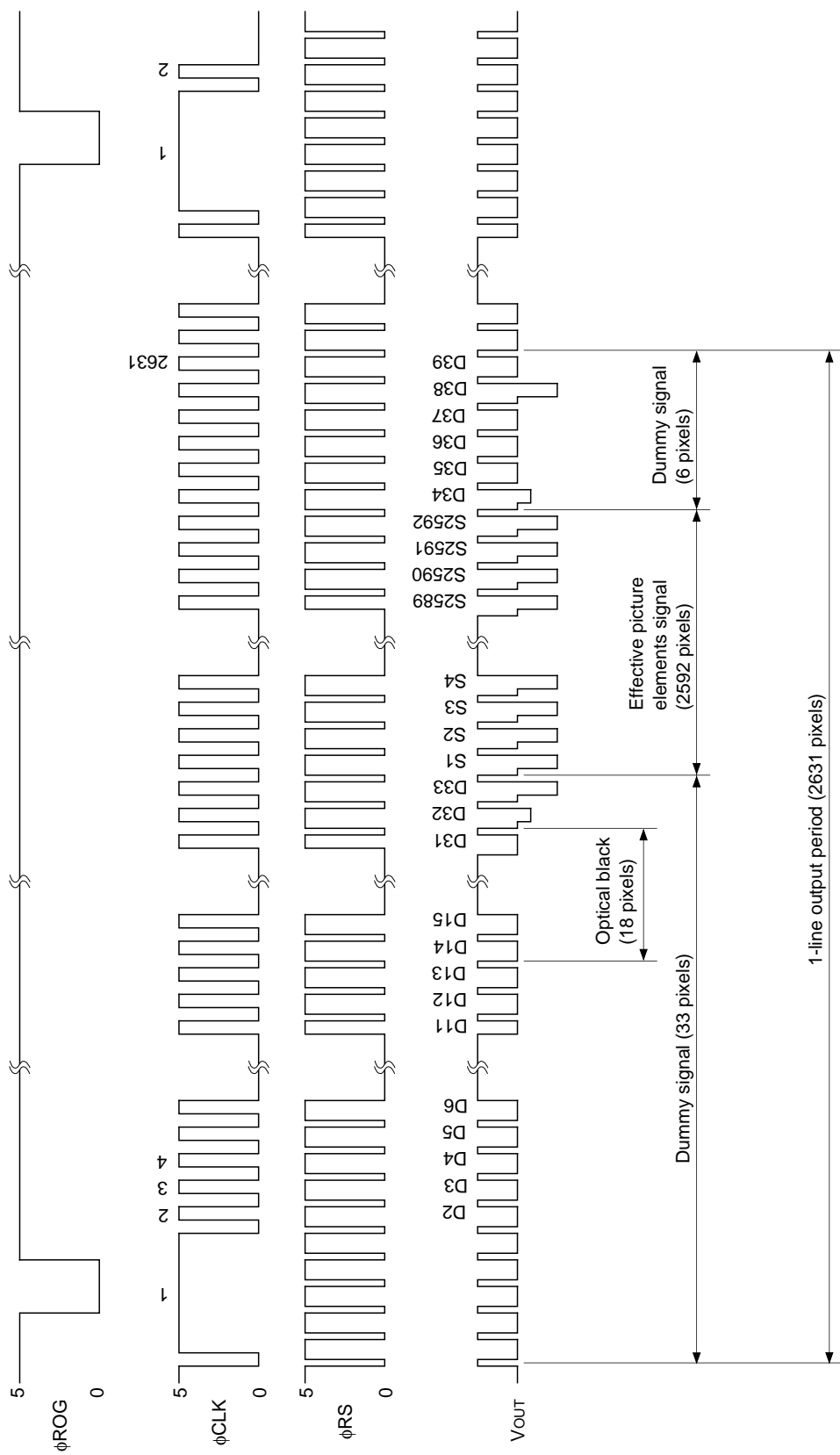


Clock Timing Diagram (For internal RS mode)

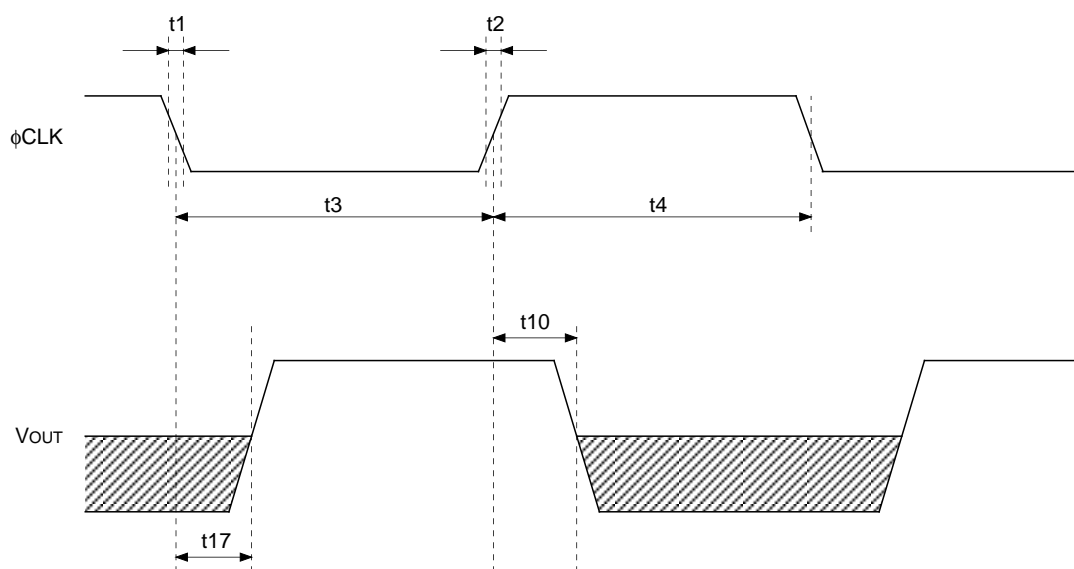


\* Internal S/H is not in use

Clock Timing Diagram (For external RS mode)



$\phi$ CLK, Vout Timing (For internal RS mode)

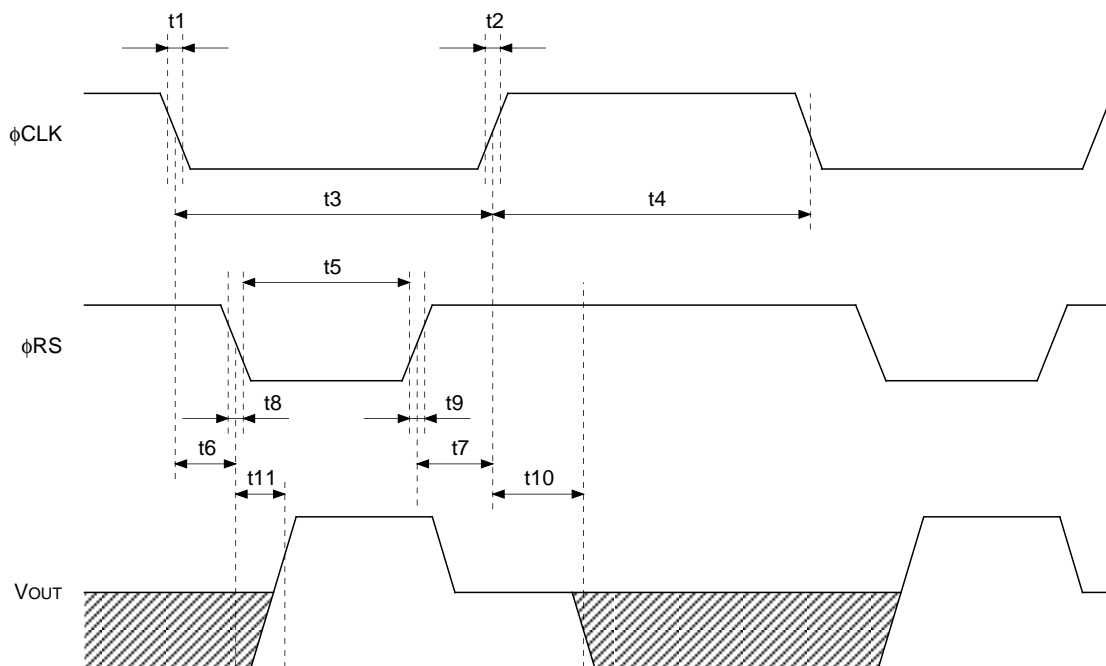


Item	Symbol	Min.	Typ.	Max.	Unit
$\phi$ CLK pulse rise/fall time	$t_1, t_2$	0	10	—	ns
$\phi$ CLK pulse duty*1	—	40	50	60	%
$\phi$ CLK – $V_{OUT}$ 1	$t_{10}$	50	80	110	ns
$\phi$ CLK – $V_{OUT}$ 2	$t_{17}$	30	75	120	ns

\*1  $100 \times t_3 / (t_3 + t_4)$



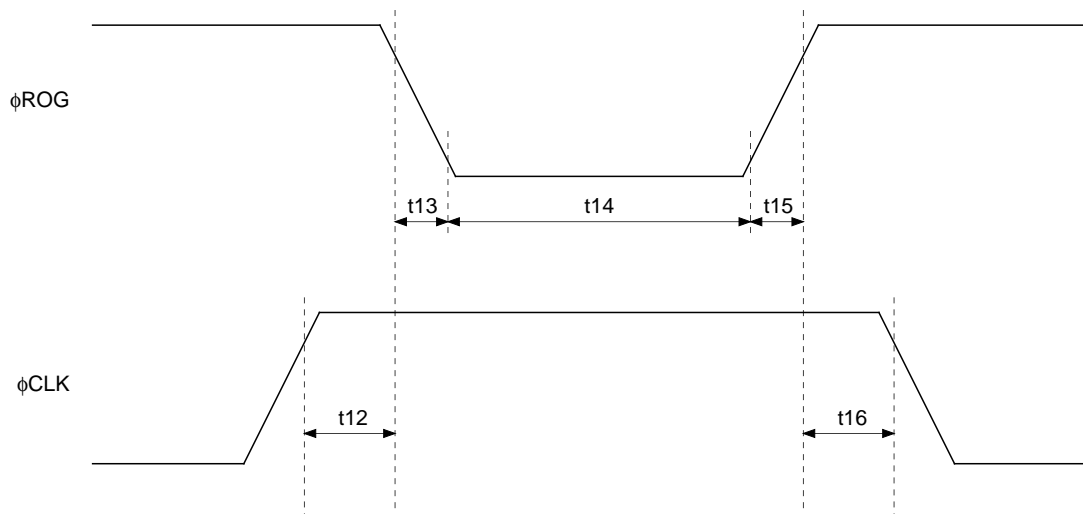
$\phi$ CLK,  $\phi$ RS,  $V_{out}$  Timing (For external RS mode)



Item	Symbol	Min.	Typ.	Max.	Unit
$\phi$ CLK, $\phi$ RS pulse rise/fall time	t1, t2, t8, t9	0	10	—	ns
$\phi$ CLK pulse duty*1	—	40	50	60	%
$\phi$ CLK – $\phi$ RS pulse timing	t6	0	100	—	ns
$\phi$ CLK – $\phi$ RS pulse timing	t7	50	100	—	ns
$\phi$ RS pulse period	t5	50	100	—	ns
$\phi$ CLK – $V_{out}$	t10	50	80	110	ns
$\phi$ RS – $V_{out}$	t11	30	50	70	ns

\*1  $100 \times t3 / (t3 + t4)$

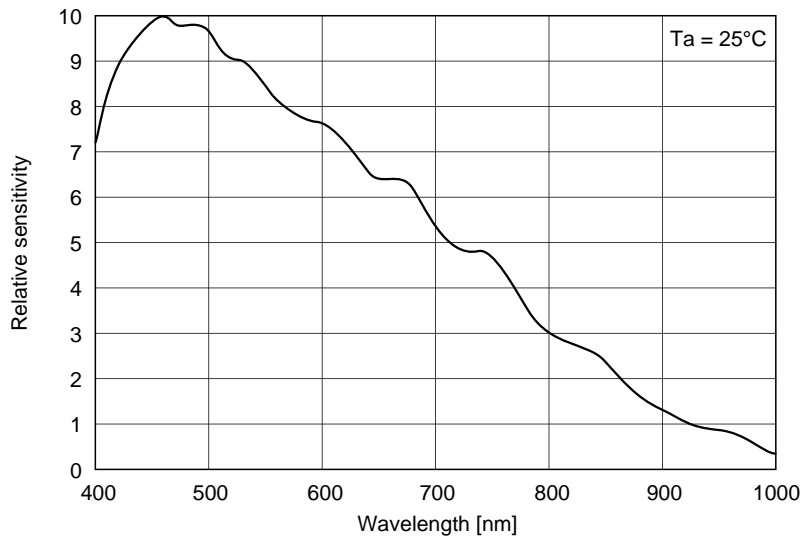
$\phi$ ROG,  $\phi$ CLK Timing



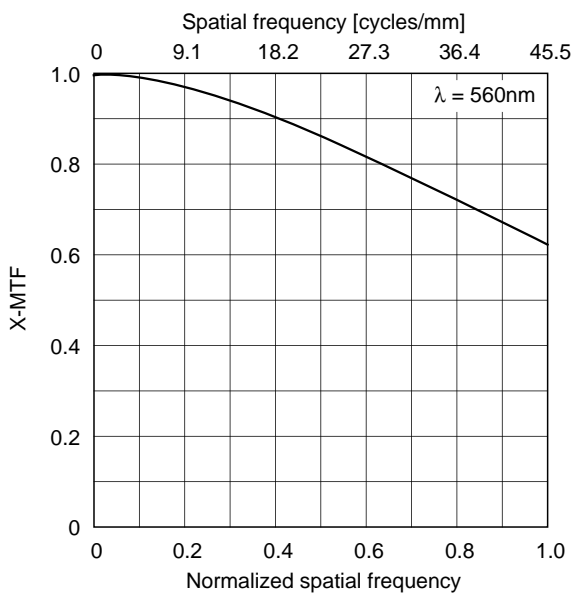
Item	Symbol	Min.	Typ.	Max.	Unit
$\phi$ ROG, $\phi$ CLK pulse timing	t12, t16	500	1000	—	ns
$\phi$ ROG pulse rise/fall time	t13, t15	0	10	—	ns
$\phi$ ROG pulse period	t14	500	1000	—	ns

Example of Representative Characteristics

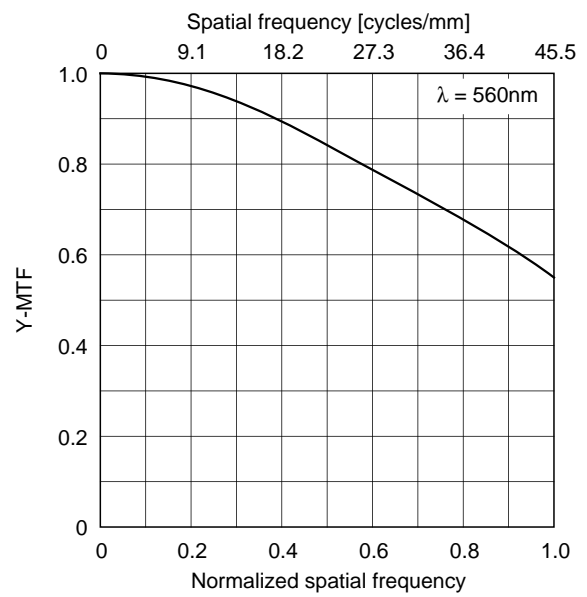
Spectral sensitivity characteristics  
(Standard characteristics)



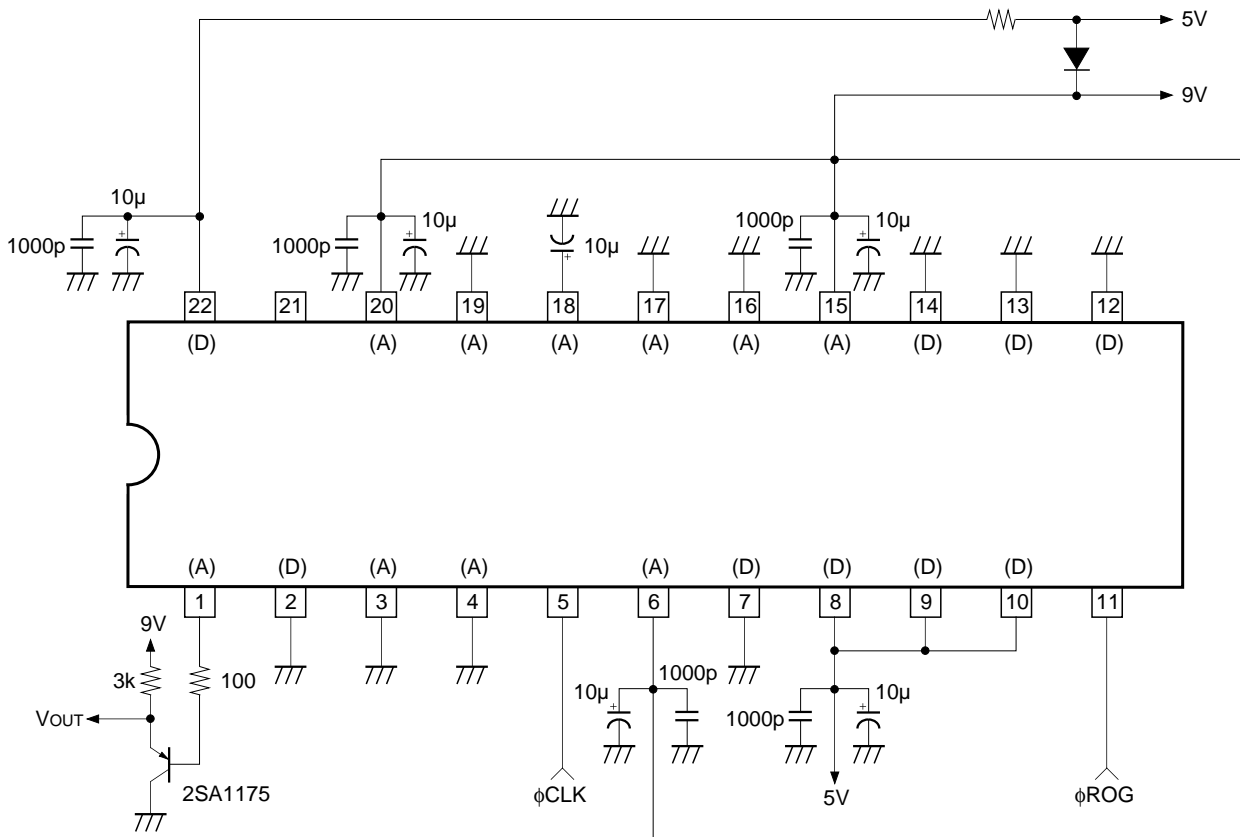
MTF of main scanning direction  
(Standard characteristics)



MTF of sub scanning direction  
(Standard characteristics)



Application Circuit



- Internal S/H is in use. Pin 4 must be connected to 5V DC power supply when S/H is not used.
- Internal RS mode is used. For the external RS mode, connect Pin 19 and Pin 4 to 5V DC power supply and input a proper clock pulse into Pin 10.
- When noise influence into output signal is large, connect pins indicated by (A) to the analog power supply and pins indicated by (D) to the digital power supply, and also use a decoupling capacitor of large capacitance.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

## Notes on Handling

### 1) Static charge prevention

CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

- a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
- b) When handling directly use an earth band.
- c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
- d) Ionized air is recommended for discharge when handling CCD image sensor.
- e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

### 2) Regulation for raising and lowering the power supply voltage

When raising the supply voltage, first raise  $V_{DD1}$  (9V) and then  $V_{DD2}$  (5V). Similarly, lower  $V_{DD2}$  (5V) first and then  $V_{DD1}$  (9V).

### 3) Soldering

- a) Make sure the package temperature does not exceed 80°C.
- b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
- c) To dismount an image sensor, do not use a solder suction equipment. When using an electric desoldering tool, ground the controller. For the control system, use a zero cross type.

### 4) Dust and dirt protection

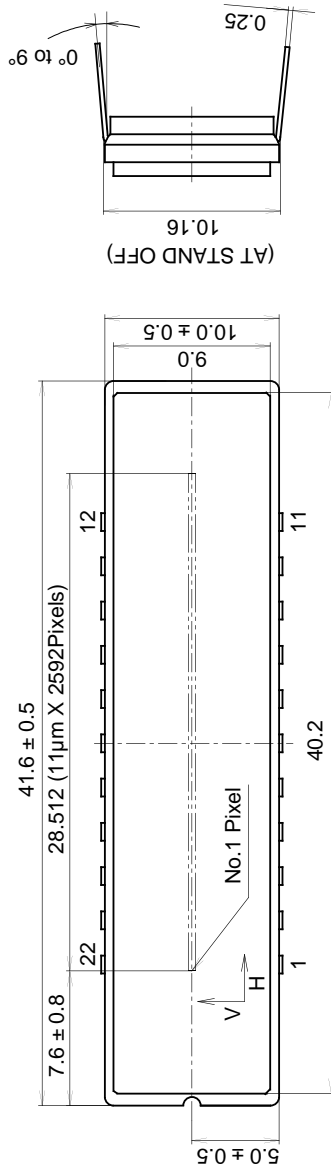
- a) Operate in clean environments.
- b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
- c) Clean with a cotton bud and ethyl alcohol if the grease stained. Be careful not to scratch the glass.
- d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

### 5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

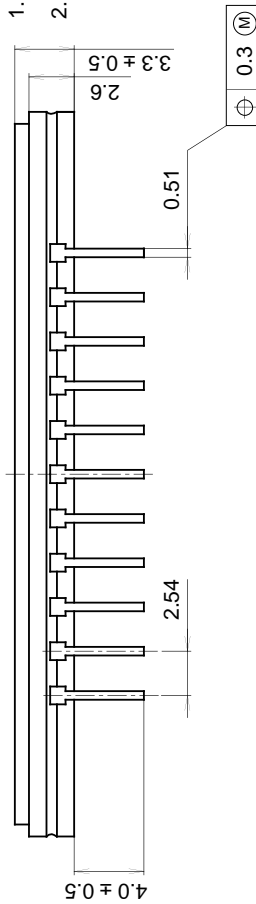
### 6) CCD image sensors are precise optical equipment that should not be subject to mechanical shocks.

Package Outline Unit: mm

22pin DIP (400mil)



1. The height from the bottom to the sensor surface is  $1.61 \pm 0.3\text{mm}$ .
2. The thickness of the cover glass is  $0.7\text{mm}$ , and the refractive index is 1.5.



PACKAGE STRUCTURE

PACKAGE MATERIAL	Cer-DIP
LEAD TREATMENT	TIN PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	3.9g