

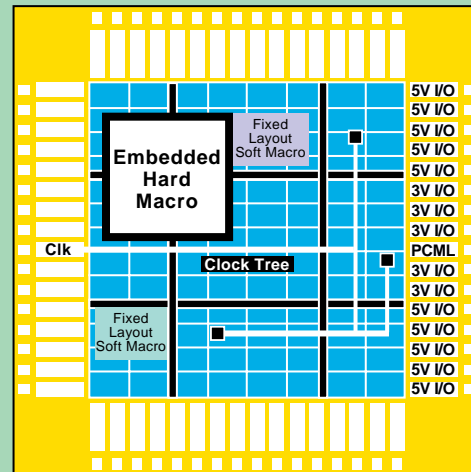
CE61 Series Embedded Array



0.28 μ m L_{eff}

Features

- 0.28 μ m L_{eff} (0.35 μ m drawn)
- Propagation delay of 85 ps
- Mixed-signal macros—A/D and D/A converters
- High density diffused RAMs and ROMs
- Separate core and I/O supply voltages
- I/Os—5V, 3.3V and 5V tolerant
- 70 μ m staggered pad pitch for pad-limited designs
- High performance and special I/Os—311 PCML, 250 MHz LVDS, PCI, SSTL
- Analog and digital PLLs
- Packaging options—QFP, HQFP, BGA
- Support for major third-party EDA tools



Description

Fujitsu's CE61 is a series of high-performance, CMOS embedded arrays featuring full support of mixed-signal macros, as well as diffused high-speed RAMs, ROMs and a variety of other embedded functions. The CE61 series offers density and performance approaching standard cells, yet provides the time-to-market advantage of gate arrays. The E-series is optimized for pad-limited designs, and the F-series offers a cost-effective solution for core-limited designs. A fifth metal layer option is also available for area bump designs, providing over 1,000 I/O pads.

Featuring true 3.3V internal operation, with 3.3V, 5V and 5V tolerant I/Os, the CE61 series features a very low-power consumption of 0.32 μ W/gate/MHz. Potential applications for the CE61 series include computing, graphics, communications, networking, wireless, and consumer designs.

E-series, 70 μ m Staggered Pad Pitch Optimized for Pad-Limited Designs

Frame	Total Gates	Total Pads
CE61E71	1,584K	672
CE61E59	1,149K	576
CE61E45	784K	480
CE61E35	602K	424
CE61E25	403K	352
CE61E19	280K	304
CE61E15	193K	256
CE61E09	120K	208
CE61E08	80K	176
CE61E07	64K	160

F-series, Optimized for Core-Limited Designs

Frame	Total Gates	Total Pads
CE61F80	2,026K	456
CE61F70	1,508K	400
CE61F60	1,182K	400
CE61F50	913K	352
CE61F40	664K	304
CE61F30	476K	256
CE61F20	303K	208
CE61F10	132K	144

CE61 Series (0.28 μ m Leff) Embedded Array

Mixed-Signal Macros

D/A Converters

- 8-bit, 30 MHz (video)
- 8-bit, 50 MHz (video)
- 8-bit, 220 MHz (video)
- 10-bit, 1.5 MHz (general purpose)
- 8-bit, 200 kHz (general purpose)

A/D Converters

- 8-bit, 50 MHz (video)
- 6-bit, 300 MHz (disk drive)
- 10-bit, 20 MHz (digital communications)
- 8-bit, 400 kHz (general purpose)
- 10-bit, 1 MHz (general purpose)

Multiplier Compiler

- Multiplicand (m): $4 \leq m \leq 32$
- Multiplier (n): $4 \leq n \leq 32$ (even numbers only)

Memory Macros

- SRAM Compiler: single and dual port (1 R/W, 1R), up to 72K bits per block
- ROM Compiler: up to 512K bits per block

Phase Locked Loops

- Digital: 180 to 360 MHz
- Analog: 50 to 200 MHz

I/Os

- 5V, 3.3V and 5V tolerant
- Slew-rate controlled
- CMOS, TTL, PCML/PECL, LVDS, PCI, SSTL, 1284, GTL+

IPs and Mega Macros

To achieve the highest level of integration for our customers, Fujitsu offers a rich set of intellectual properties (IPs), developed either internally or acquired through strategic relationships with IP providers.

Interface Functions

- ARC: 32-bit embedded core
- OakDSPCore[®]: 16-bit fixed point DSP core
- PCI core
- 10/100 Ethernet MAC
- P1394
- USB

High-Performance Functions

- MPEG2 (Q1 '99)
- 16/64/256 QAM (Q1 '99)
- QPSK (Q1 '99)

ASIC Design Kit and EDA Support

Verifire (VCS, Cadence Tools, Synopsys, Synthesis)	VCS, Verilog-XL, Sign-off Simulation, Veritime, Verifault, Design Compiler (Synopsys)
Vhdlfire	All Vital compliance tools, Sign-off Simulation, Design Time, Design Compiler
Other EDA Tools	Motive, Sunrise, HLD, DesignPower

PACKAGE AVAILABILITY

No. of Pins	Frame Size
QFP Package (1.0, 0.8, 0.65 mm pitch)	
64	F10
80	F10
100	F10
120	F10, E7/8/9/15/19/25/35/45
160	E7/8/9/15/19/25/35/45/59, F20/30/40/50/60/70/80
Shrink QFP Package (0.5 mm pitch)	
64	E7/8/9, F10
80	E7/8/9, F10
100	E9/15, F10
120	E7/8/9/15/19/25/35/45, F10
144	E7/8/9/15/19/25/35/45, F20/30/40/50
176	E8/9/15/19/25/35/45, F20/30/40/50
208	E9/15/19/25/35/45/59, F20/30/40/50/60/70/80
240	E15/19/25/35/45/59, F30/40/50/60/70
256	F40/50/60/70/80
304	F50/60/70/80
256 (0.4 mm)	E19/25/35/45/59
Heatspreader QFP Package (0.5 mm pitch)	
208	E9/15/19/25/35/45/59/71, F20/30/40/50/60/70/80
240	E15/19/25/35/45/58/71, F30/40/50/60/70/80
256	F40/50/60/70/80
304	E35/45/59/71, F50/60/70/80
256 (0.4 mm)	E19/25/35/45/59/71
Ball Grid Array (1.27 mm pitch)	
256	E15/19, F40/50
352	E25/35, F60/70
420	E35/45, F60/70
576	E45/59
672	E71

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Printed in the U.S.A. ASIC-FS-20505-7/98