

# BIPOLAR ANALOG INTEGRATED CIRCUIT

# $\mu$ PC8129GR

### UP CONVERTER WITH AGC FUNCTION + QUADRATURE MODULATOR IC FOR DIGITAL MOBILE COMMUNICATION SYSTEMS

#### DESCRIPTION

The  $\mu$ PC8129GR is a silicon monolithic integrated circuit designed as indirect quadrature modulator for digital mobile communication systems. This modulator consists of 0.8 GHz to 1.9 GHz up-converter and 100 MHz to 400 MHz quadrature modulator which are packaged in 20 pin SSOP. The device has power save function and can operate 2.7 to 5.5 V supply voltage, therefore, it can contribute to make RF block small, high performance and low power consumption.

#### FEATURES

- High linearity up converter is incorporated;  $P_{RFout} = -5$  dBm TYP./@ $f_{RFout} = 900$  MHz
- Wide operating frequency range. Up converter;  $f_{RFout} = 800$  MHz to 1900 MHz  
Modulator ;  $f_{LO1in} = 200$  MHz to 800 MHz  
 $f_{MODout} = 100$  MHz to 400 MHz,  $f_{I/Q} = DC$  to 10 MHz
- External IF filter can be applied between modulator output and up converter input terminal.
- Low phase difference due to digital phase shifter is adopted.
- Supply voltage:  $V_{CC} = 2.7$  to 5.5 V
- Equipped with power save function.
- 20 pin SSOP suitable for high density surface mounting.

#### APPLICATIONS

- Digital cellular phones (ex. GSM etc...)
- Digital cordless phones

#### ORDERING INFORMATION

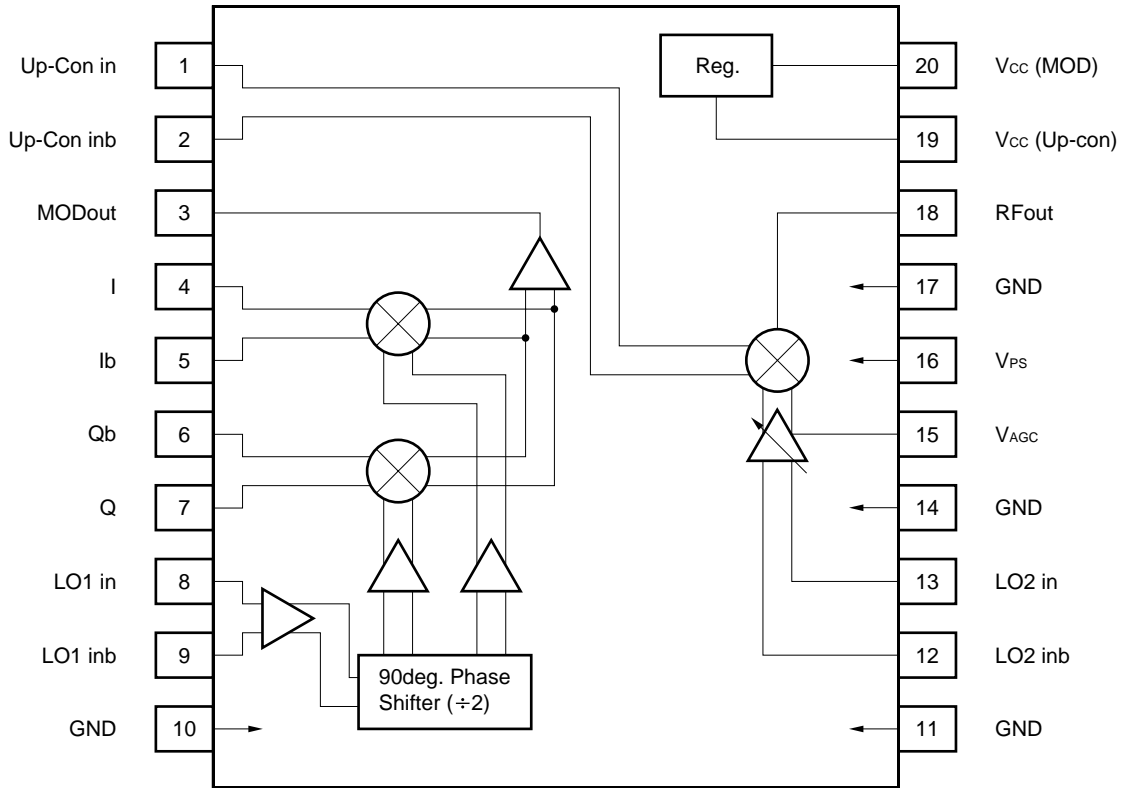
| PART NUMBER       | PACKAGE                          | SUPPLYING FORM   |
|-------------------|----------------------------------|--|
| $\mu$ PC8129GR-E1 | 20 pin plastic SSOP<br>(225 mil) | Embossed tape 12 mm wide. QTY 2.5 kp/Reel.<br>Pins 1 through 10 are in pull-out direction. |

\* To order evaluation samples, please contact your local NEC sales office. (Part number for sample order:  $\mu$ PC8129GR)

**Caution electro-static sensitive device**

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.  
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

INTERNAL BLOCK DIAGRAM AND PIN CONNECTIONS

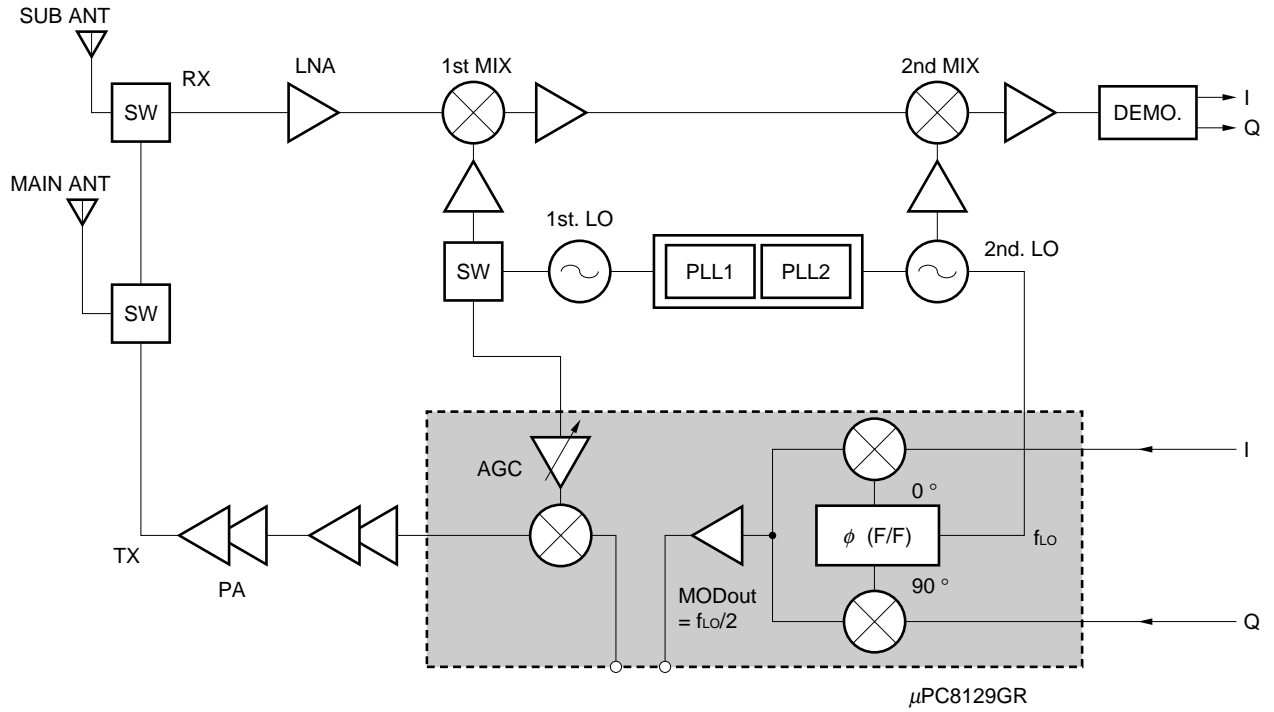


★ QUADRATURE MODULATOR SERIES PRODUCT

| Part Number   | Functions  | I <sub>cc</sub> (mA)           | f <sub>LOin</sub> (MHz) | f <sub>MODout</sub> (MHz) | RF Mixer f <sub>RFout</sub> (MHz) | Phase Shifter | Package                | Application        |
|---------------|--|--------------------------------|-------------------------|---------------------------|-----------------------------------|---------------|------------------------|--------------------|
| μPC8101GR     | 150 MHz Quad.Mod   | 15/@2.7 V                      | 100 to 300              | 50 to 150                 | External                          | F/F           | 20-pin                 | CT-2 etc.          |
| μPC8104GR     | RF Up-Converter + IF Quad.Mod                                | 28/@3.0 V                      | 100 to 400              | 900 to 1 900              | External                          | Doubler + F/F | SSOP (225 mil)         | Digital Comm.      |
| μPC8105GR     | 400 MHz Quad.Mod   | 16/@3.0 V                      | 100 to 400              | 16-pin SSOP (225 mil)     |                                   |               |                        |                    |
| μPC8110GR     | 1 GHz Direct Quad.Mod  | 24/@3.0 V                      | 800 to 1 000            | 20-pin SSOP (225 mil)     |                                   |               | PDC800 MHz, etc.       |                    |
| μPC8125GR     | RF Up-Converter + IF Quad.Mod + AGC                          | 36/@3.0 V                      | 220 to 270              | 1 800 to 2 000            |                                   |               | PHS                    |                    |
| μPC8126GR     | 900 MHz Direct Quad.Mod with Offset-Mixer                    | 35/@3.0 V                      | 915 to 960              | 915 to 960                | 889 to 960                        | 889 to 960    | 28-pin QFN             | PDC800 MHz         |
| μPC8126K      |  |                                |                         |                           |                                   |               |                        |                    |
| μPC8129GR     | ×2LO IF Quad. Mod+RF Up-Converter                            | 28/@3.0 V                      | 200 to 800              | 100 to 400                | 800 to 1 900                      | F/F           | 20-pin SSOP (225 mil)  | GSM, DCS1800, etc. |
| μPC8139GR-7JH | Transceiver IC (1.9 GHz Indirect Quad. Mod + RX-IF + IF VCO) | TX: 32.5<br>RX: 4.8<br>/@3.0 V | 220 to 270              | 1 800 to 2 000            | 800 to 1 500                      | CR            | 30-pin TSSOP (225 mil) | PHS                |
| μPC8158K      | RF Up-Converter + IF Quad.Mod + AGC                          | 28/@3.0 V                      | 100 to 300              | 28-pin QFN                |                                   |               | PDC800 M/1.5 G         |                    |

APPLICATION EXAMPLE

[GSM]



**ABSOLUTE MAXIMUM RATINGS**

| PARAMETER                     | SYMBOL           | RATING      | UNIT | CONDITION                               |
|-------------------------------|------------------|-------------|------|---|
| Supply Voltage                | V <sub>CC</sub>  | 6.0         | V    | T <sub>A</sub> = +25 °C                 |
| Power Save Voltage            | V <sub>PS</sub>  | 6.0         | V    |   |
| AGC Control Voltage           | V <sub>AGC</sub> | 6.0         | V    |   |
| IQ DC Offset Voltage          | IQ (DC)          | 4.0         | V    |   |
| Power Dissipation             | P <sub>D</sub>   | 430         | mW   | T <sub>A</sub> = +85 °C <sup>Note</sup> |
| Operating Ambient Temperature | T <sub>A</sub>   | -40 to +85  | °C   |   |
| Storage Temperature           | T <sub>stg</sub> | -55 to +150 | °C   |   |

**Note** Mounted on double sided copper clad 50 × 50 × 1.6 mm epoxy glass PWB.

**RECOMMENDED OPERATING CONDITIONS**

| PARAMETER                     | SYMBOL               | MIN. | TYP. | MAX. | UNIT              | CONDITIONS         |
|-------------------------------|----------------------|------|------|------|-------------------|--------------------|
| Supply Voltage                | V <sub>CC</sub>      | 2.7  | 3.0  | 5.5  | V                 |                    |
| Operating Ambient Temperature | T <sub>A</sub>       | -40  | +25  | +85  | °C                |                    |
| Up Converter RF Frequency     | f <sub>RFout</sub>   | 800  |      | 1900 | MHz               |                    |
| Up Converter Input Freq.      | f <sub>UPCONin</sub> | 100  |      | 400  | MHz               |                    |
| Modulator Output Frequency    | f <sub>MODout</sub>  |      |      |      |                   |                    |
| LO1 Input Frequency           | f <sub>LO1in</sub>   | 200  |      | 800  | MHz               |                    |
| LO1 Input Level               | P <sub>LO1in</sub>   | -15  | -10  | -5   | dBm               |                    |
| LO2 Input Frequency           | f <sub>LO2in</sub>   | 800  |      | 1800 | MHz               |                    |
| LO2 Input Level               | P <sub>LO2in</sub>   | -15  | -10  | -5   | dBm               |                    |
| I/Q Input Frequency           | f <sub>I/Qin</sub>   | DC   |      | 10   | MHz               |                    |
| I/Q Input Amplitude           | V <sub>I/Qin</sub>   |      |      | 600  | mV <sub>P-P</sub> | Single ended Input |

**ELECTRICAL CHARACTERISTICS (1)**

Conditions (unless otherwise specified):

$T_A = +25\text{ }^\circ\text{C}$ ,  $V_{CC} = 3\text{ V}$ ,  $V_{PS} = 3\text{ V}$ ,  $R_{PS} = 1\text{ k}\Omega$ ,  $V_{AGC} = 3\text{ V}$ ,  $R_{AGC} = 10\text{ k}\Omega$

$I/Q\text{ DC} = 1.5\text{ V}$  ( $V_{bias(I)} = V_{bias(Ib)} = V_{bias(Q)} = V_{bias(Qb)} = 1.5\text{ V}$ )

$f_{I/Qin} = 67.7\text{ kHz}$ ,  $V_{I/Qin} = 500\text{ mV}_{P-P}$  (single ended input,  $I_b = Q_b = 0\text{ mV}_{P-P}$ )

Modulation Pattern: <0000>

$f_{LO1in} = 500\text{ MHz}$ ,  $P_{LO1in} = -10\text{ dBm}$

$f_{LO2in} = 1150\text{ MHz}$ ,  $P_{LO2in} = -10\text{ dBm}$

$f_{UPCONin} = f_{MODout} = f_{LO1in}/2 + f_{I/Qin} = 250\text{ MHz} + f_{I/Qin}$

$f_{RFout} = 900\text{ MHz} - f_{I/Qin}$

| PARAMETER  | SYMBOL                    | MIN. | TYP. | MAX.  | UNIT | TEST CONDITIONS                        |
|--|---------------------------|------|------|-------|------|--|
| <b>UP CONVERTER + QUADRATURE MODULATOR TOTAL</b> |                           |      |      |       |      |  |
| Total Circuit Current                            | $I_{CC(TOTAL)}$           | 20   | 28   | 37    | mA   | No input signal                        |
| Total Circuit Current at Power Save Mode         | $I_{CC(PS)TOTAL1}$        |      | 0.6  | 10    | μA   | $V_{PS} \leq 0.5\text{ V}$             |
| Total Output Power                               | $P_{RFout}$               | -8   | -5   | -2    | dBm  |  |
| Local Oscillator Carrier Leakage                 | LoL                       |      | -40  | -26.5 | dBc  | $f_{LoL} = f_{LO2} - f_{LO1}/2$        |
| Image Rejection (Side Band Leak)                 | ImR                       |      | -30  | -26.5 | dBc  |  |
| AGC Gain Control Rang                            | GCR                       | 28   | 40   |       | dB   | $V_{AGC} = 2.5\text{ V to }0\text{ V}$ |
| Power Save Rise Time                             | $T_{PS(rise)}$            |      | 2.0  | 5.0   | μs   | $V_{PS(Low)} \rightarrow V_{PS(High)}$ |
| Power Save Fall Time                             | $T_{PS(fall)}$            |      | 2.0  | 5.0   | μs   | $V_{PS(High)} \rightarrow V_{PS(Low)}$ |
| <b>UP CONVERTER BLOCK</b>                        |                           |      |      |       |      |  |
| Circuit Current at Power Save Mode               | $I_{CC(PS)}$<br>(Up con.) |      |      | 5.0   | μA   | $V_{PS} \leq 0.5\text{ V}$             |
| <b>QUADRATURE MODULATOR BLOCK</b>                |                           |      |      |       |      |  |
| Circuit Current at Power Save Mode               | $I_{CC(PS)}$<br>(MOD)     |      |      | 5.0   | μA   | $V_{PS} \leq 0.5\text{ V}$             |

**STANDARD CHARACTERISTICS FOR REFERENCE (1)**

Conditions (unless otherwise specified):

$T_A = +25\text{ }^\circ\text{C}$ ,  $V_{CC} = 3\text{ V}$ ,  $V_{PS} = 3\text{ V}$ ,  $R_{PS} = 1\text{ k}\Omega$ ,  $V_{AGC} = 3\text{ V}$ ,  $R_{AGC} = 10\text{ k}\Omega$

I/Q DC = 1.5 V ( $V_{bias(I)} = V_{bias(Ib)} = V_{bias(Q)} = V_{bias(Qb)} = 1.5\text{ V}$ )

$f_{I/Qin} = 67.7\text{ kHz}$ ,  $P_{I/Qin} = 500\text{ mV}_{P-P}$  (single ended input,  $I_b = Q_b = 0\text{ mV}_{P-P}$ )

Modulation Pattern: <0000>

$f_{LO1in} = 500\text{ MHz}$ ,  $P_{LO1in} = -10\text{ dBm}$

$f_{LO2in} = 1150\text{ MHz}$ ,  $P_{LO2in} = -10\text{ dBm}$

$f_{UPCONin} = f_{MODout} = f_{LO1in}/2 + f_{I/Qin} = 250\text{ MHz} + f_{I/Qin}$

$f_{RFout} = 900\text{ MHz} - f_{I/Qin}$

| PARAMETER  | SYMBOL                | REFERENCE | UNIT       | TEST CONDITIONS                                     |
|--|-----------------------|-----------|------------|---|
| <b>UP CONVERTER + QUADRATURE MODULATOR TOTAL</b> |                       |           |            |   |
| Total Circuit Current at Power-Save Mode         | $I_{CC(PS)TOTAL2}$    | 60        | μA         | $V_{PS} \leq 0.5\text{ V}$ , $V_{AGC} = 0\text{ V}$ |
| Phase Error                                      | $\Delta\phi$          | 1.8       | deg. (rms) | MOD Pattern: PN9                                    |
| <b>UP CONVERTER BLOCK</b>                        |                       |           |            |   |
| UP Con. Circuit Current                          | $I_{CC(UPCon)}$       | 14        | mA         | No input signal                                     |
| UP Con. Circuit Current at Power-Save Mode       | $I_{CC(PS)UPCon}$     | 60        | μA         | $V_{PS} \leq 0.5\text{ V}$ , $V_{AGC} = 0\text{ V}$ |
| Conversion Gain                                  | CG                    | 12        | dB         | $P_{UPCONin} = -20\text{ dBm}$                      |
| Maximum Output Power                             | $P_{RF(sat)}$         | -1.5      | dBm        | $P_{UPCONin} = -4\text{ dBm}$                       |
| Output 3rd Order Intercept Point                 | OIP <sub>3</sub>      | +6        | dBm        | $f_{UPCONin} = 250.0\text{ MHz}/250.2\text{ MHz}$   |
| <b>QUADRATURE MODULATOR BLOCK</b>                |                       |           |            |   |
| MOD. Circuit Current                             | $I_{CC(MOD)}$         | 14        | mA         | No input signal                                     |
| Output Power                                     | $P_{MODout}$          | -16.5     | dBm        |   |
| LO1 Carrier Leakage                              | LoL                   | -40       | dBc        | $f_{LoL} = f_{LO1}/2$                               |
| Image Rejection (Side Band Leak)                 | ImR                   | -30       | dBc        |   |
| I/Q 3rd Order Intermodulation Distortion         | IM <sub>3/IQ</sub>    | -50       | dBc        |   |
| I/Q Input Impedance                              | Z <sub>I/Q</sub>      | 200       | kΩ         | I to Ib, Q to Qb                                    |
| IQ Bias Current                                  | I <sub>I/Q</sub>      | 5         | μA         | I, Ib, Q, Qb to GND (each)                          |
| LO1 Input VSWR                                   | VSWR <sub>(Lo1)</sub> | 1.2 : 1   | -          |   |
| Output Noise Floor                               |                       | -133      | dBc/Hz     | $\Delta f = \pm 20\text{ MHz}$                      |

**STANDARD CHARACTERISTICS FOR REFERENCE (2)**

Conditions (unless otherwise specified):

$T_A = +25\text{ }^\circ\text{C}$ ,  $V_{CC} = 3\text{ V}$ ,  $V_{PS} = 3\text{ V}$ ,  $R_{PS} = 1\text{ k}\Omega$ ,  $V_{AGC} = 3\text{ V}$ ,  $R_{AGC} = 10\text{ k}\Omega$

I/Q DC = 1.5 V ( $V_{bias(I)} = V_{bias(Ib)} = V_{bias(Q)} = V_{bias(Qb)} = 1.5\text{ V}$ )

$f_{I/Qin} = 67.7\text{ kHz}$ ,  $P_{I/Qin} = 500\text{ mV}_{P-P}$  (single ended input,  $I_b = Q_b = 0\text{ mV}_{P-P}$ )

Modulation Pattern: <0000>

$f_{LO1in} = 500\text{ MHz}$ ,  $P_{LO1in} = -10\text{ dBm}$

$f_{LO2in} = 1650\text{ MHz}$ ,  $P_{LO2in} = -10\text{ dBm}$

$f_{UPCONin} = f_{MODout} = f_{LO1in}/2 + f_{I/Qin} = 250\text{ MHz} + f_{I/Qin}$

$f_{RFout} = 1900\text{ MHz} + f_{I/Qin}$

| PARAMETER  | SYMBOL           | REFERENCE | UNIT       | TEST CONDITIONS                                   |
|--|------------------|-----------|------------|---|
| <b>UP CONVERTER + QUADRATURE MODULATOR TOTAL</b> |                  |           |            |   |
| Total Output Power                               | $P_{RFout}$      | -12       | dBm        |   |
| Local Oscillator Carrier Leakage                 | LoL              | -40       | dBc        | $f_{LoL} = f_{LO2} + f_{LO1}/2$                   |
| Image Rejection (Side Band Leak)                 | ImR              | -30       | dBc        |   |
| AGC Gain Control Rang                            | GCR              | 45        | dB         | $V_{AGC} = 2.5\text{ V to }0\text{ V}$            |
| Phase Error                                      | $\Delta\phi$     | 1.8       | deg. (rms) | MOD Pattern: PN9                                  |
| <b>UP CONVERTER BLOCK</b>                        |                  |           |            |   |
| Conversion Gain                                  | CG               | 5         | dB         | $P_{UPCONin} = -20\text{ dBm}$                    |
| Maximum Output Power                             | $P_{RF(sat)}$    | -7        | dBm        | $P_{UPCONin} = -4\text{ dBm}$                     |
| Output Intercept Point                           | OIP <sub>3</sub> | -1        | dBm        | $f_{UPCONin} = 250.0\text{ MHz}/250.2\text{ MHz}$ |

PIN EXPLANATION

| Pin No. | Symbol    | Supply Voltage (V) | Pin Voltage Typ. (V)<br>@V <sub>CC</sub> = 3 V | Description  | Equivalent Circuit |
|---------|-----------|--------------------|--|--|--------------------|
| 18      | RFout     | V <sub>CC</sub>    | –  | RF output from Up-Converter. This pin is open collector output.  |                    |
| 1       | UpCon in  | –                  | 2.2  | IF input for Up-converter. This pin is high impedance input.   |                    |
| 2       | UpCon inb | –                  | 2.2  | Bypass of IF input. Grounded through external capacitor.   |                    |
| 3       | MODout    | –                  | 1.9  | Output from modulator. This is emitter follower output.  |                    |
| 4       | I         | V <sub>CC</sub> /2 | –  | Input for I signal. This input impedance is about 200 kΩ. Relations between amplitude and V <sub>CC</sub> /2 bias of input signal are following. |                    |
| 5       | Ib        | V <sub>CC</sub> /2 | –  | Input for I signal. This input impedance is about 200 kΩ. V <sub>CC</sub> /2 biased DC signal should be input.                                   |                    |
| 6       | Qb        | V <sub>CC</sub> /2 | –  | Input for Q signal. This input impedance is about 200 kΩ. V <sub>CC</sub> /2 biased DC signal should be input.                                   |                    |
| 7       | Q         | V <sub>CC</sub> /2 | –  | Input for Q signal. This input impedance is about 200 kΩ. Relations between amplitude and V <sub>CC</sub> /2 bias of input signal are following. |                    |

| V <sub>CC</sub> /2 (V) | Signal Level (mV <sub>P-P</sub> ) |
|------------------------|-----------------------------------|
| ≥ 1.35                 | ≤ 400                             |
| ≥ 1.5                  | ≤ 600                             |
| ≥ 1.75                 | ≤ 1000                            |

Note

| V <sub>CC</sub> /2 (V) | Signal Level (mV <sub>P-P</sub> ) |
|------------------------|-----------------------------------|
| ≥ 1.35                 | ≤ 400                             |
| ≥ 1.5                  | ≤ 600                             |
| ≥ 1.75                 | ≤ 1000                            |

Note

**Note** In the case of that I/Q input signals are single ended.  
Of course, I/Q signal inputs can be used either single endedly or differentially with proper terminations.



PIN EXPLANATION

| Pin No.              | Symbol                           | Supply Voltage (V)   | Pin Voltage Typ. (V) @ V <sub>CC</sub> = 3 V | Description   | Equivalent Circuit  |                     |       |                      |                  |          |                  |
|----------------------|----------------------------------|----------------------|--|---|---|---------------------|-------|----------------------|------------------|----------|------------------|
| 8                    | LO1in                            | –                    | 0  | Lo1 input for phase shifter. This input impedance is 50 Ω matched internally.   |   |                     |       |                      |                  |          |                  |
| 9                    | LO1in b                          | –                    | 2.3  | Bypass of Lo1 input. This pin is grounded through internal capacitor.   |   |                     |       |                      |                  |          |                  |
| 10                   | GND for Modulator                | 0                    | –  | Connect to the ground with minimum inductance. Track length should be kept as short as possible.  |   |                     |       |                      |                  |          |                  |
| 11                   |                                  |                      |  |   |   |                     |       |                      |                  |          |                  |
| 12                   | LO2in b                          | –                    | 1.9  | Bypass of Lo2 input. Grounded through external capacitor.   |   |                     |       |                      |                  |          |                  |
| 13                   | LO2in                            | –                    | 1.9  | Lo2 input of Up-converter. This pin is high impedance input.  |   |                     |       |                      |                  |          |                  |
| 14                   | GND for Up-con.                  | 0                    | –  | Connect to the ground with minimum inductance. Track length should be kept as short as possible.  |   |                     |       |                      |                  |          |                  |
| 17                   |                                  |                      |  |   |   |                     |       |                      |                  |          |                  |
| 15                   | V <sub>AGC</sub>                 | 0 to V <sub>CC</sub> | –  | Input for AGC amplifier. Total Output Power can be controlled by changing input voltage. And as external series resistance (R <sub>AGC</sub> ) connecting, a slope of AGC curve can be changed by the resistance (R <sub>AGC</sub> ). |   |                     |       |                      |                  |          |                  |
| 16                   | Power Save                       | 0 to V <sub>CC</sub> | –  | Power save control pin can be controlled ON/OFF state with bias as follows;   | <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>V<sub>PS</sub> (V)</th> <th>STATE</th> </tr> </thead> <tbody> <tr> <td>2 to V<sub>CC</sub></td> <td>ON (Active Mode)</td> </tr> <tr> <td>0 to 0.5</td> <td>OFF (Sleep Mode)</td> </tr> </tbody> </table> | V <sub>PS</sub> (V) | STATE | 2 to V <sub>CC</sub> | ON (Active Mode) | 0 to 0.5 | OFF (Sleep Mode) |
| V <sub>PS</sub> (V)  | STATE                            |                      |  |   |   |                     |       |                      |                  |          |                  |
| 2 to V <sub>CC</sub> | ON (Active Mode)                 |                      |  |   |   |                     |       |                      |                  |          |                  |
| 0 to 0.5             | OFF (Sleep Mode)                 |                      |  |   |   |                     |       |                      |                  |          |                  |
| 19                   | V <sub>CC</sub> for Up-converter | 2.7 to 5.5           | –  | Supply voltage pin for Up-converter.  |   |                     |       |                      |                  |          |                  |
| 20                   | V <sub>CC</sub> for Modulator    | 2.7 to 5.5           | –  | Supply voltage pin for modulator. Internal regulator can be kept stable condition of supply bias against the variable temperature or V <sub>CC</sub> .  |   |                     |       |                      |                  |          |                  |

: Externally

**STANDARD TYPICAL CHARACTERISTICS <Modulator + Up-Converter Total at 900 MHz>**

Test Circuit 1,  $T_A = +25\text{ }^\circ\text{C}$ ,  $V_{CC} = 3\text{ V}$ ,  $V_{PS} = 3\text{ V}$ ,  $R_{PS} = 1\text{ k}\Omega$ ,  $V_{AGC} = 3\text{ V}$ ,  $R_{AGC} = 10\text{ k}\Omega$

I/Q DC = 1.5 V ( $V_{bias(I)} = V_{bias(Ib)} = V_{bias(Q)} = V_{bias(Qb)} = 1.5\text{ V}$ )

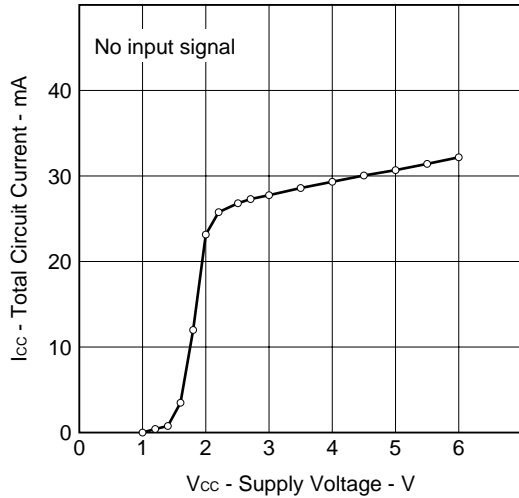
$f_{I/Qin} = 67.7\text{ kHz}$ ,  $V_{I/Qin} = 500\text{ mV}_{P-P}$  (single ended input,  $I_b = I_q = 0\text{ mV}_{P-P}$ )

Modulation Pattern: All Zero <0000>,  $f_{LO1in} = 500\text{ MHz}$ ,  $P_{LO1in} = -10\text{ dBm}$

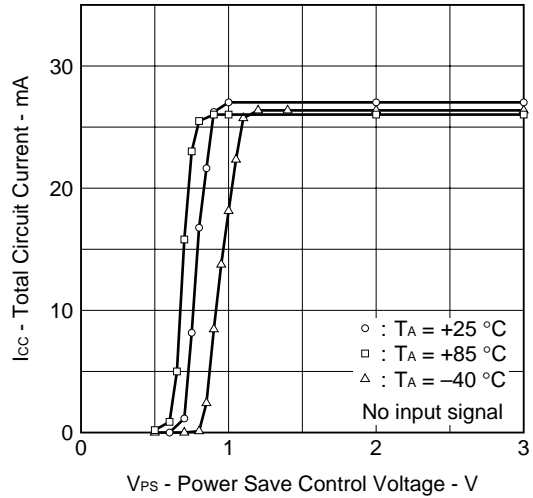
$f_{LO2in} = 1150\text{ MHz}$ ,  $P_{LO2in} = -10\text{ dBm}$ ,  $f_{UPCONin} = f_{MODout} = f_{LO1in}/2 + f_{I/Qin} = 250\text{ MHz} + f_{I/Qin}$

$f_{RFout} = 900\text{ MHz} - f_{I/Qin}$ , Unless Otherwise Specified

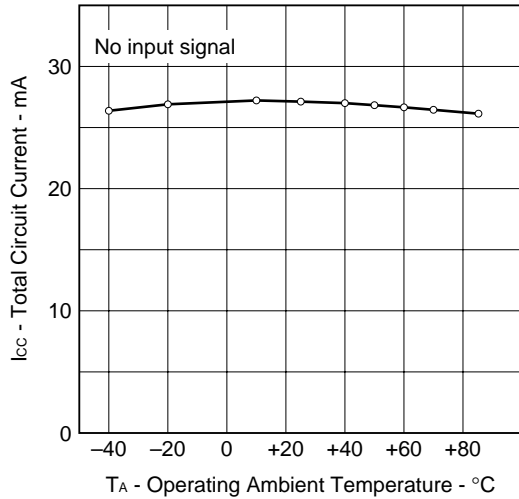
**I<sub>CC</sub> (TOTAL) vs V<sub>CC</sub>**



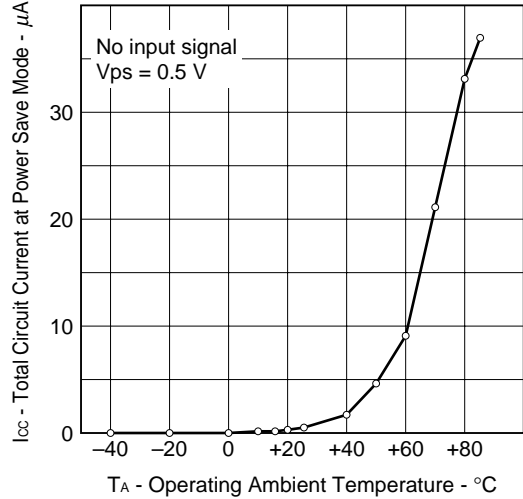
**I<sub>CC</sub> (TOTAL) vs V<sub>PS</sub>**



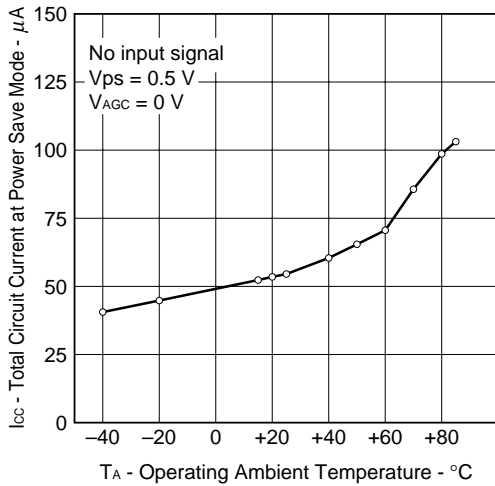
**I<sub>CC</sub> (TOTAL) vs T<sub>A</sub>**



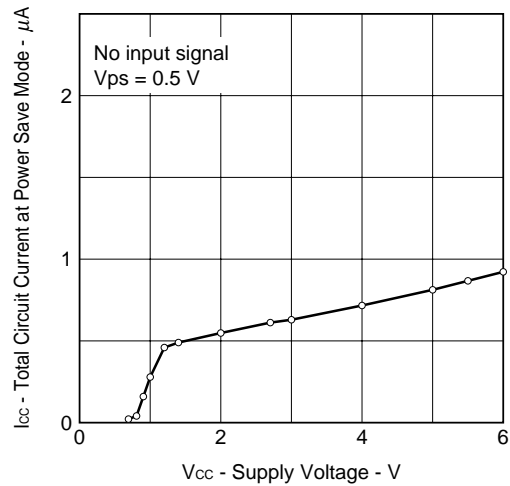
**I<sub>CC</sub> (PS) TOTAL vs T<sub>A</sub>**



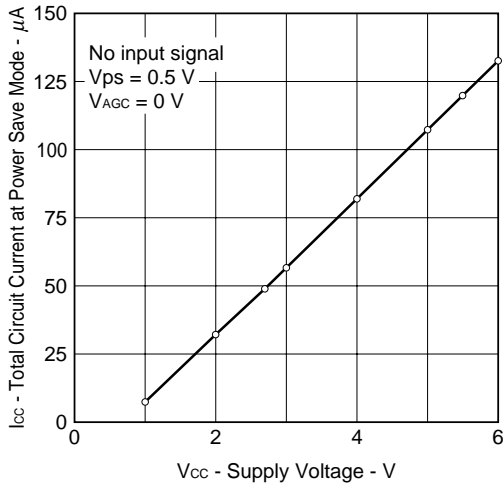
I<sub>CC</sub> (PS) TOTAL2 vs T<sub>A</sub>



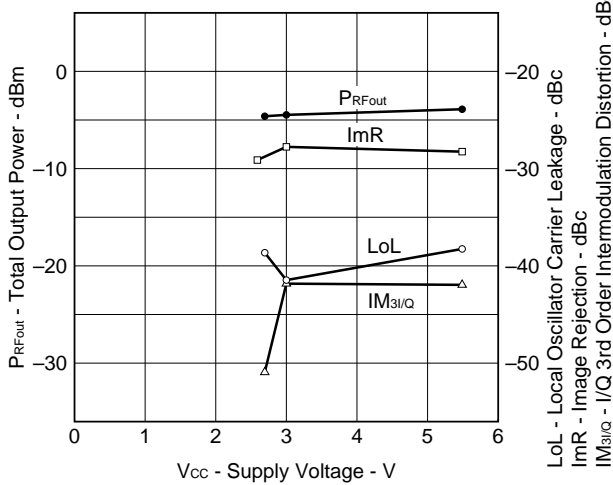
I<sub>CC</sub> (PS) TOTAL1 vs V<sub>CC</sub>



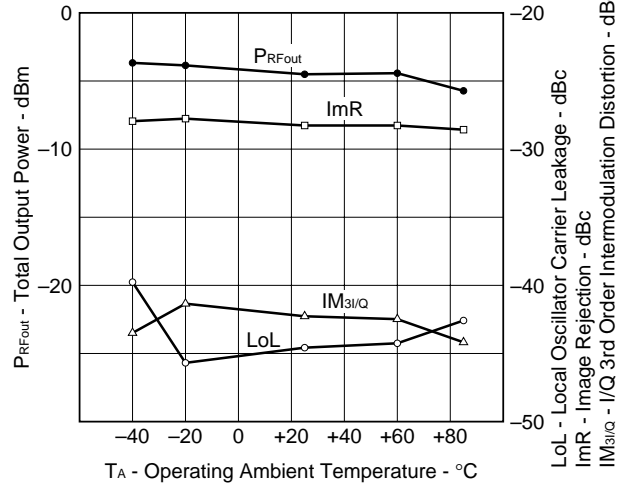
I<sub>CC</sub> (PS) TOTAL2 vs V<sub>CC</sub>



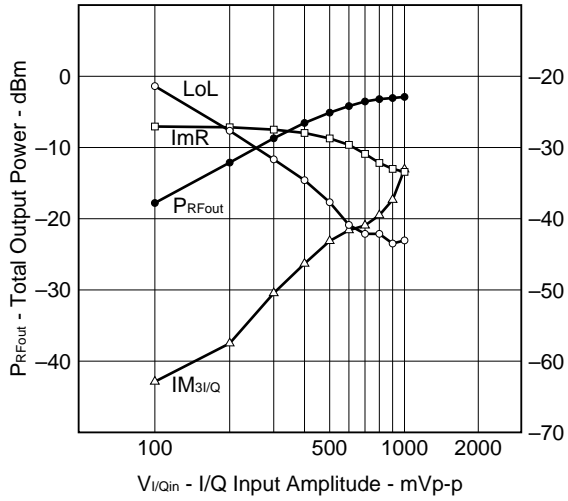
P<sub>RFout</sub>, LoL, ImR, IM<sub>3/Q</sub> vs V<sub>CC</sub>



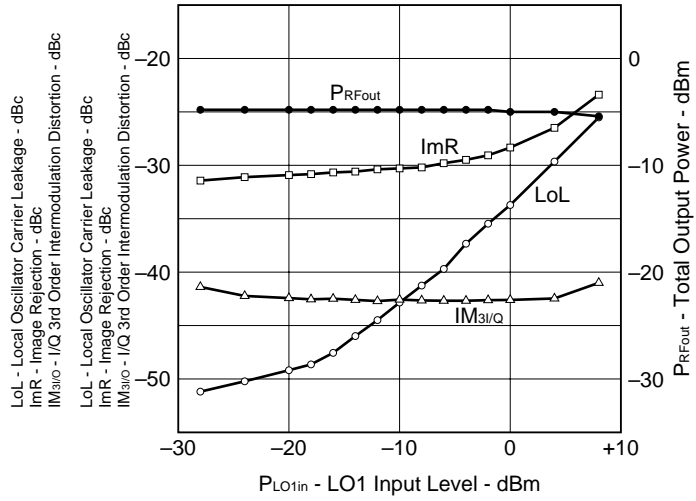
P<sub>RFout</sub>, LoL, ImR, IM<sub>3/Q</sub> vs T<sub>A</sub>



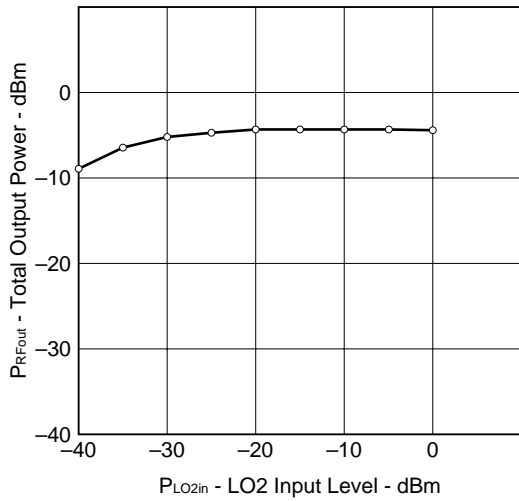
**$P_{RFout}$ , LoL, ImR,  $IM_{3/IQ}$  vs  $V_{I/Qin}$**



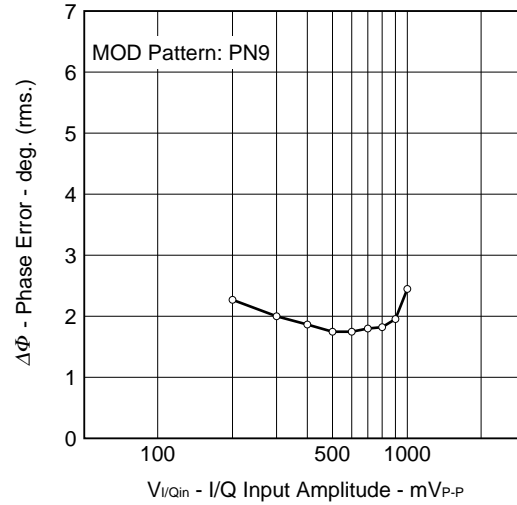
**$P_{RFout}$ , LoL, ImR,  $IM_{3/IQ}$  vs  $P_{LO1in}$**



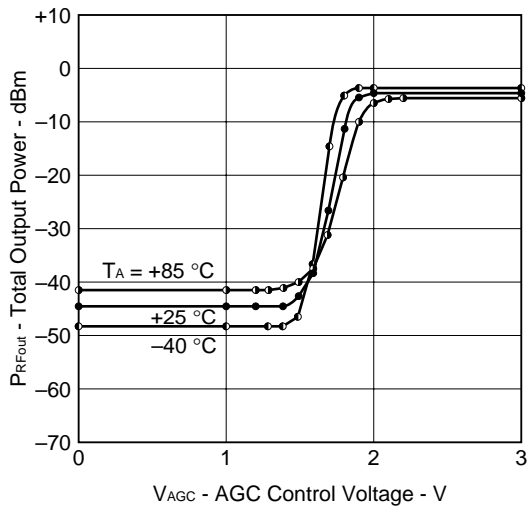
**$P_{RFout}$  vs  $P_{LO2in}$**



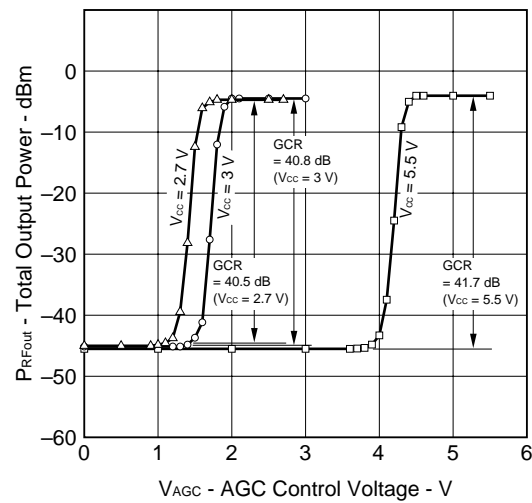
**$\Delta\phi$  vs  $V_{I/Qin}$**

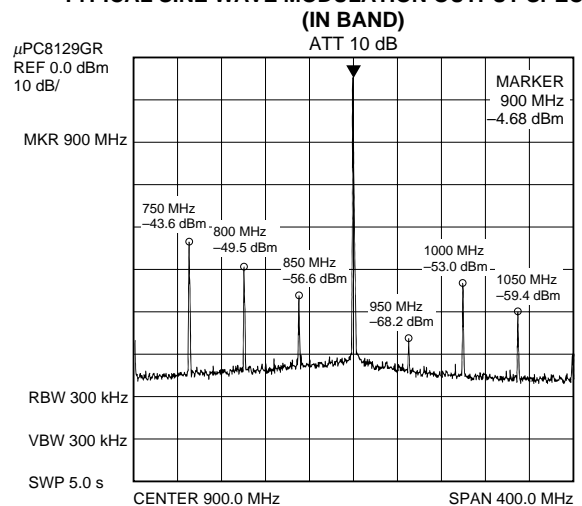
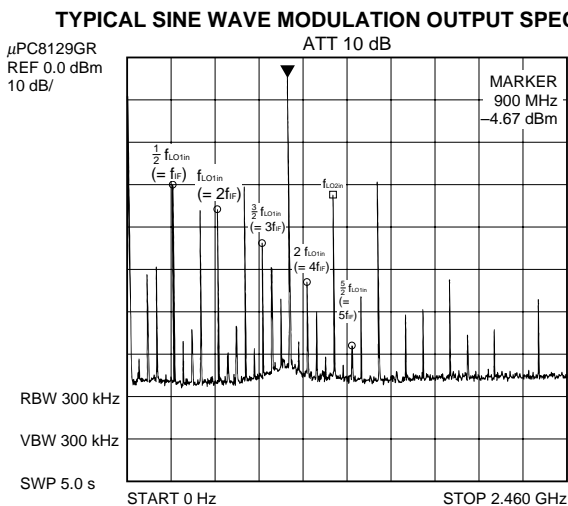
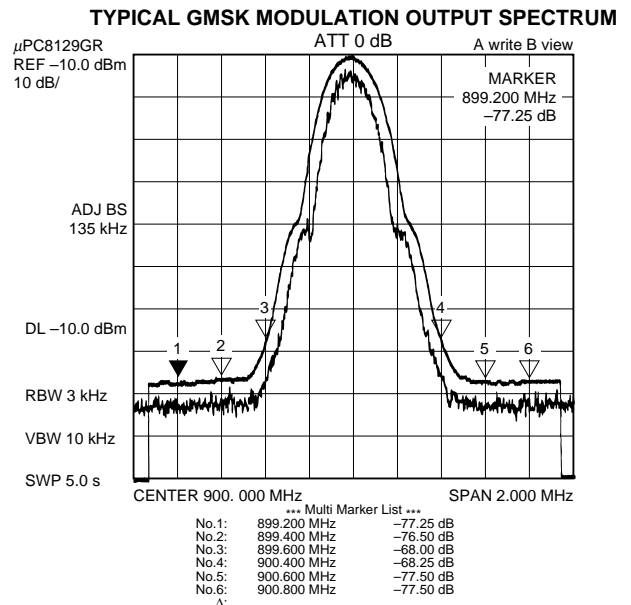
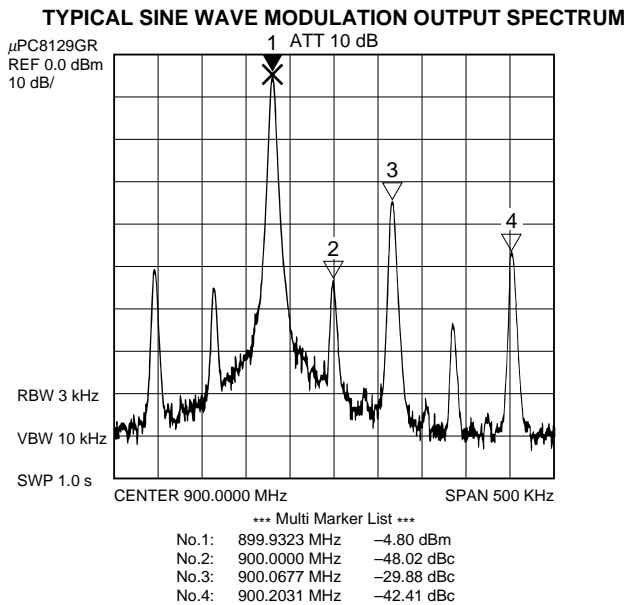
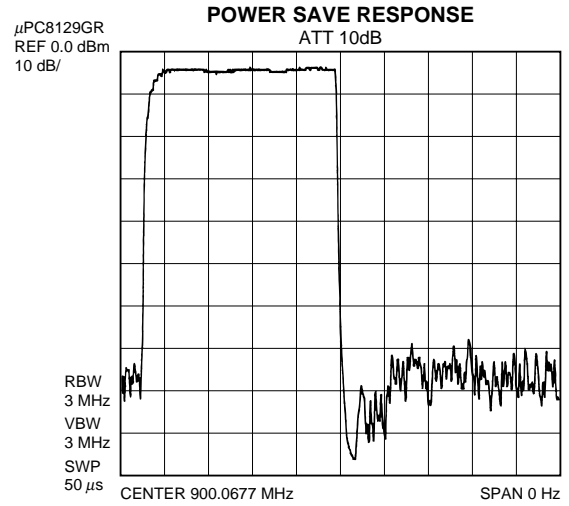
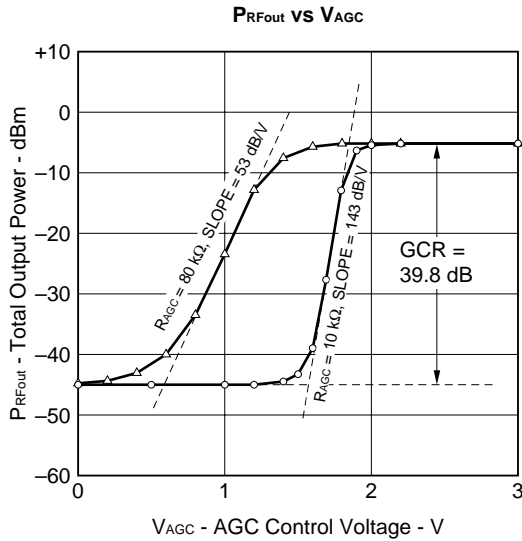


**$P_{RFout}$  vs  $V_{AGC}$**



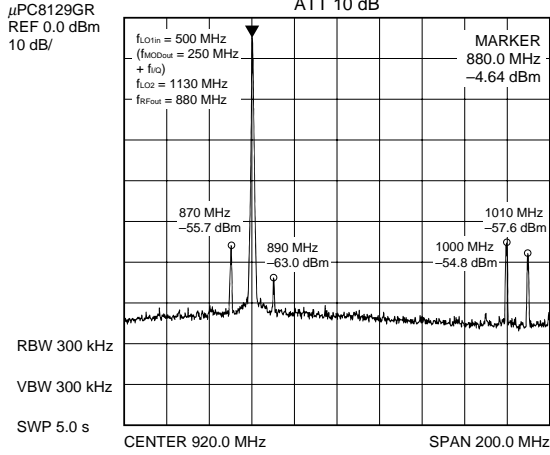
**$P_{RFout}$  vs  $V_{AGC}$**





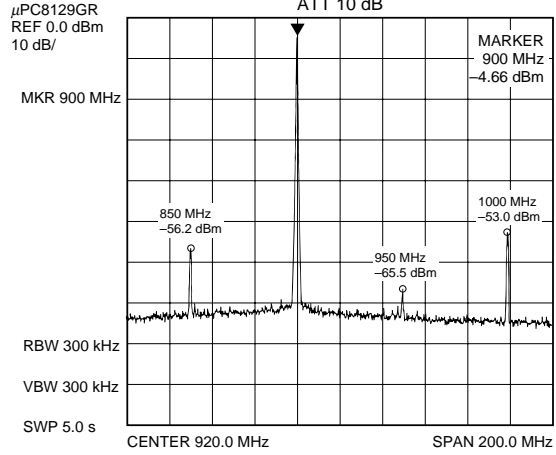
TYPICAL SINE WAVE MODULATION OUTPUT SPECTRUM

(IN BAND)  
ATT 10 dB



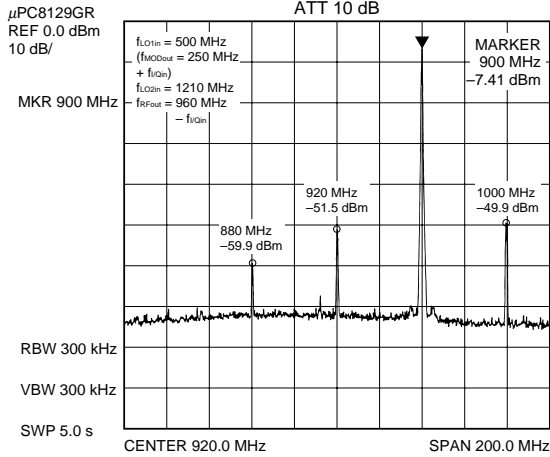
TYPICAL SINE WAVE MODULATION OUTPUT SPECTRUM

(IN BAND)  
ATT 10 dB



TYPICAL SINE WAVE MODULATION OUTPUT SPECTRUM

(IN BAND)  
ATT 10 dB



**STANDARD TYPICAL CHARACTERISTICS <Modulator + Up-Converter Total at 1900 MHz>**

Test Circuit 2,  $T_A = +25\text{ }^\circ\text{C}$ ,  $V_{CC} = 3\text{ V}$ ,  $V_{PS} = 3\text{ V}$ ,  $R_{PS} = 1\text{ k}\Omega$ ,  $V_{AGC} = 3\text{ V}$ ,  $R_{AGC} = 10\text{ k}\Omega$

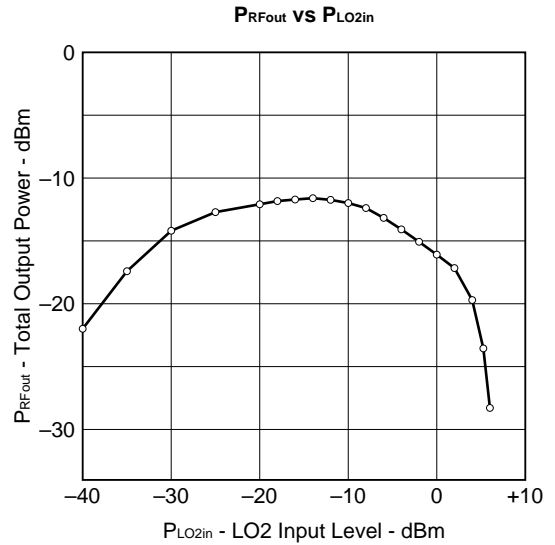
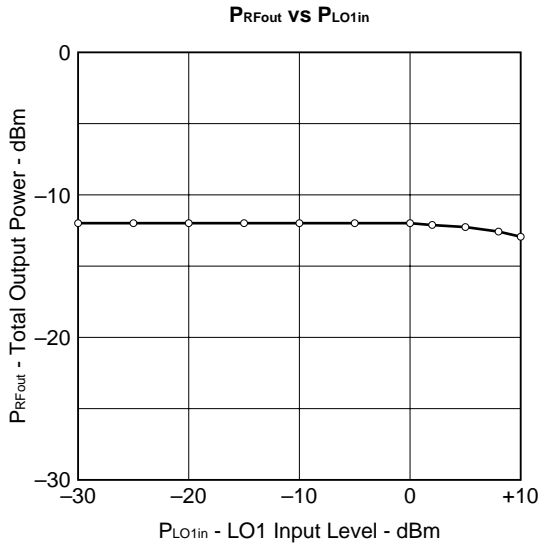
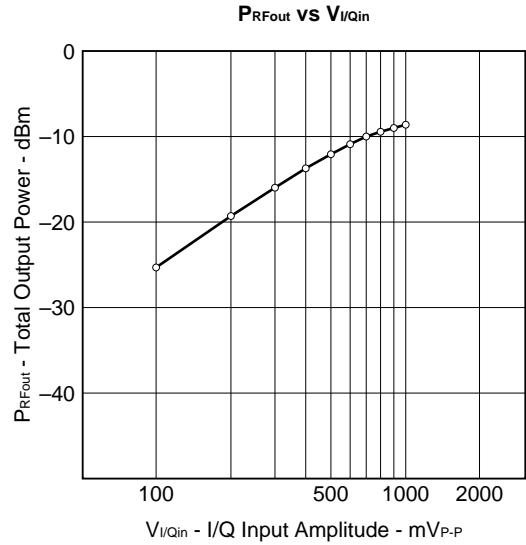
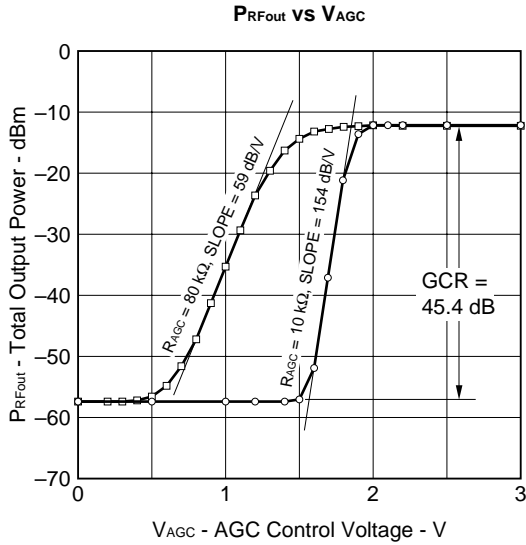
I/Q DC = 1.5 V ( $V_{bias(I)} = V_{bias(Ib)} = V_{bias(Q)} = V_{bias(Qb)} = 1.5\text{ V}$ )

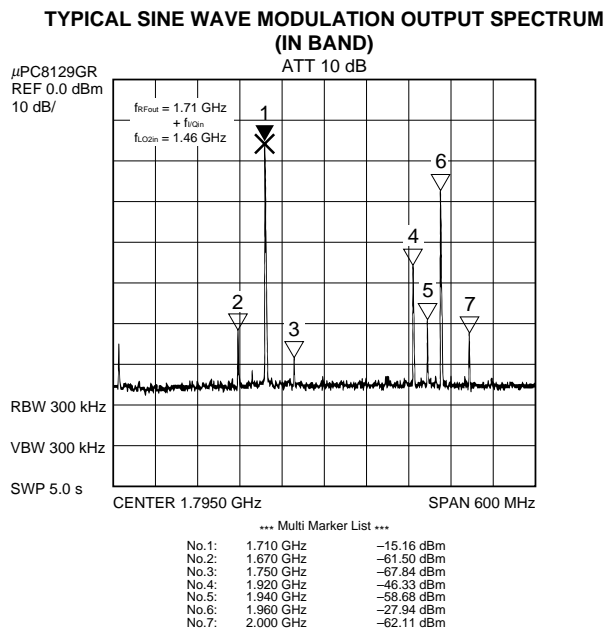
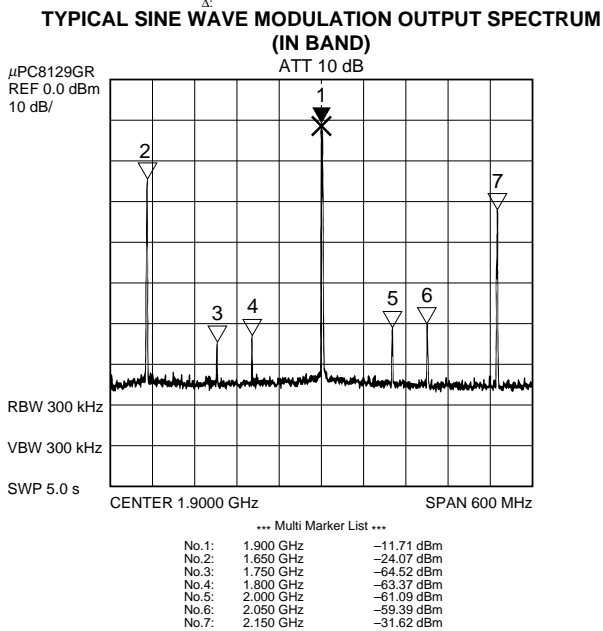
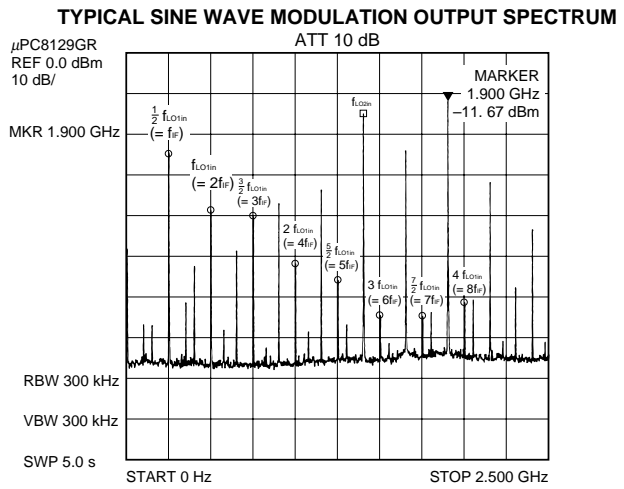
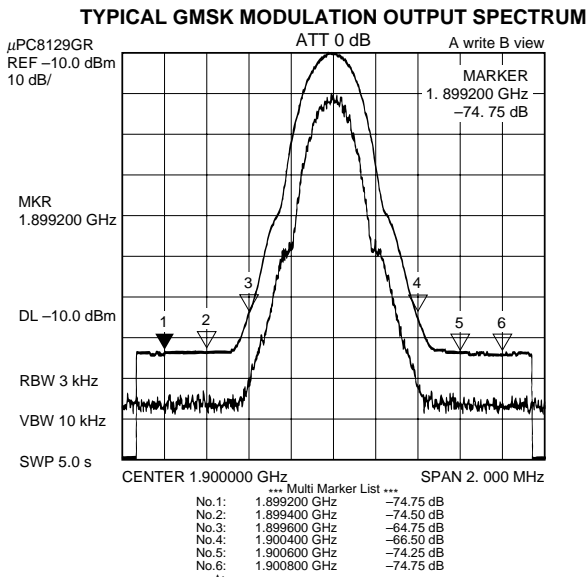
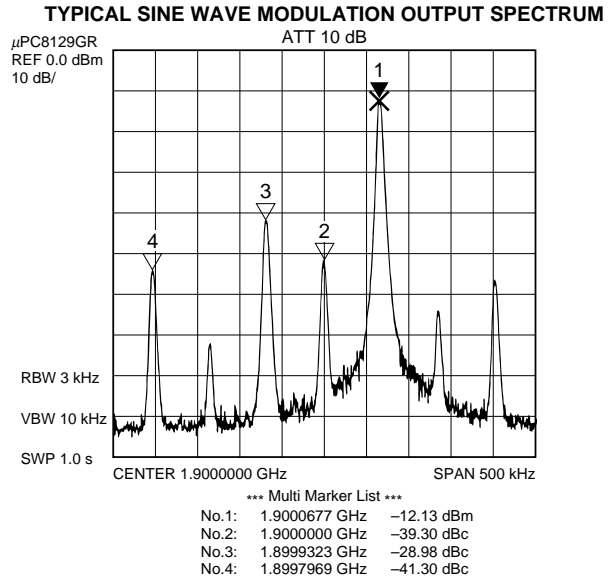
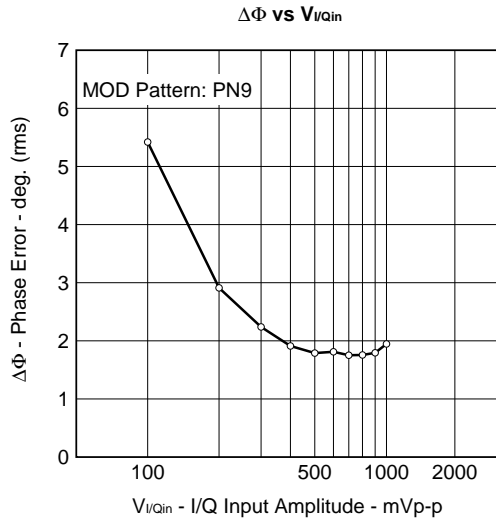
$f_{I/Qin} = 67.7\text{ kHz}$ ,  $V_{I/Qin} = 500\text{ mV}_{P-P}$  (single ended input,  $I_b = Q_b = 0\text{ mV}_{P-P}$ )

Modulation Pattern: All Zero <0000>,  $f_{LO1in} = 500\text{ MHz}$ ,  $P_{LO1in} = -10\text{ dBm}$

$f_{LO2in} = 500\text{ MHz}$ ,  $P_{LO2in} = -10\text{ dBm}$ ,  $f_{UPCONin} = f_{MODout} = f_{LO1in}/2 + f_{I/Qin} = 250\text{ MHz} + f_{I/Qin}$

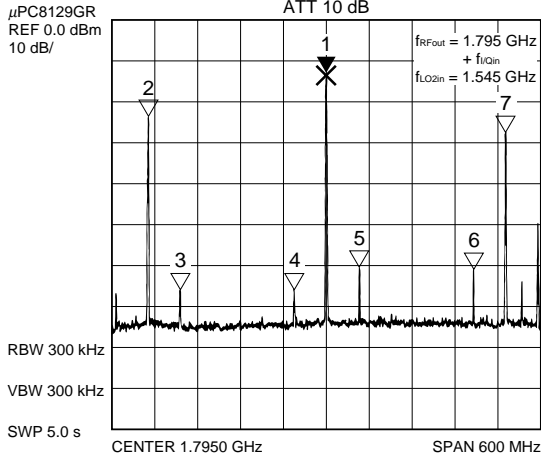
$f_{RFout} = 1900\text{ MHz} + f_{I/Qin}$ , Unless Otherwise Specified







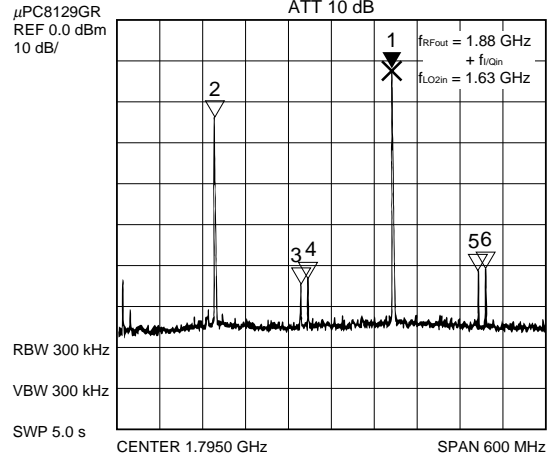
TYPICAL SINE WAVE MODULATION OUTPUT SPECTRUM  
(IN BAND)



\*\*\* Multi Marker List \*\*\*

|       |           |            |
|-------|-----------|------------|
| No.1: | 1.795 GHz | -14.21 dBm |
| No.2: | 1.545 GHz | -24.47 dBm |
| No.3: | 1.590 GHz | -65.96 dBm |
| No.4: | 1.750 GHz | -66.40 dBm |
| No.5: | 1.840 GHz | -60.91 dBm |
| No.6: | 2.000 GHz | -61.79 dBm |
| No.7: | 2.045 GHz | -28.73 dBm |

TYPICAL SINE WAVE MODULATION OUTPUT SPECTRUM  
(IN BAND)



\*\*\* Multi Marker List \*\*\*

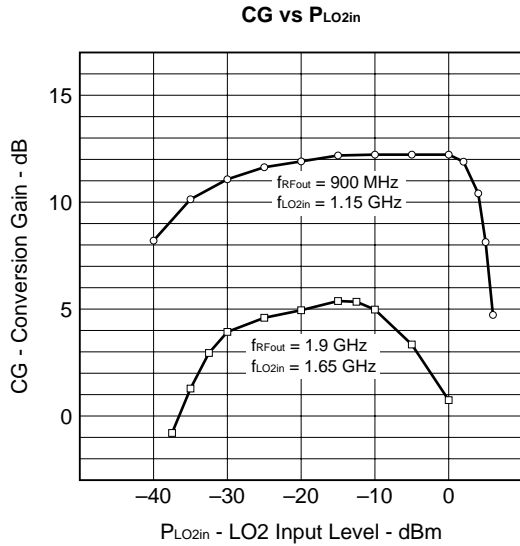
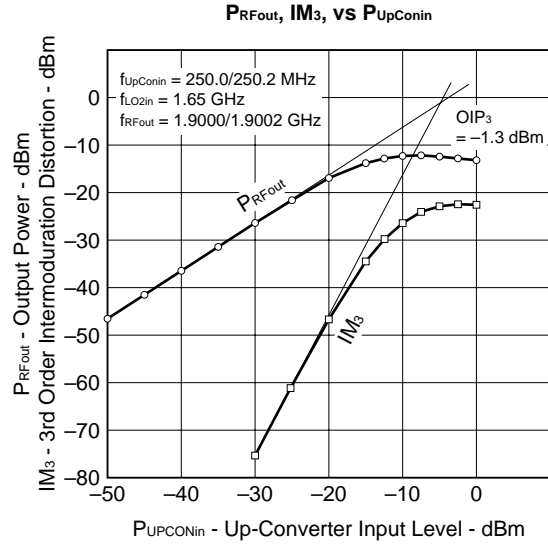
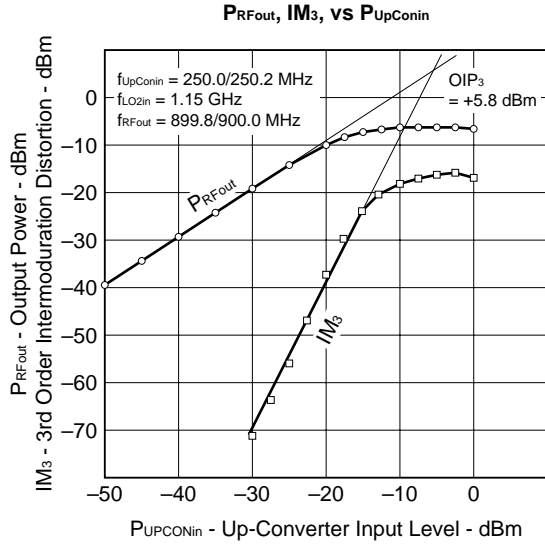
|       |           |            |
|-------|-----------|------------|
| No.1: | 1.880 GHz | -12.32 dBm |
| No.2: | 1.630 GHz | -23.47 dBm |
| No.3: | 1.750 GHz | -64.08 dBm |
| No.4: | 1.760 GHz | -63.19 dBm |
| No.5: | 2.000 GHz | -61.05 dBm |
| No.6: | 2.010 GHz | -60.25 dBm |

**STANDARD TYPICAL CHARACTERISTICS <Up-Converter Block>**

$T_A = +25\text{ }^\circ\text{C}$ ,  $V_{CC} = 3.0\text{ V}$ ,  $V_{PS} = 3.0\text{ V}$ ,  $f_{UPCONin} = 250\text{ MHz}$ ,  $P_{UPCONin} = -20\text{ dBm}$

Test Circuit 1 ( $f_{RFout} = 900\text{ MHz}$ ,  $f_{LO2in} = 1150\text{ MHz}$ ) or

Test Circuit 2 ( $f_{RFout} = 1900\text{ MHz}$ ,  $f_{LO2in} = 1650\text{ MHz}$ ), Unless Otherwise Specified



**STANDARD TYPICAL CHARACTERISTICS <Modulator Block>**

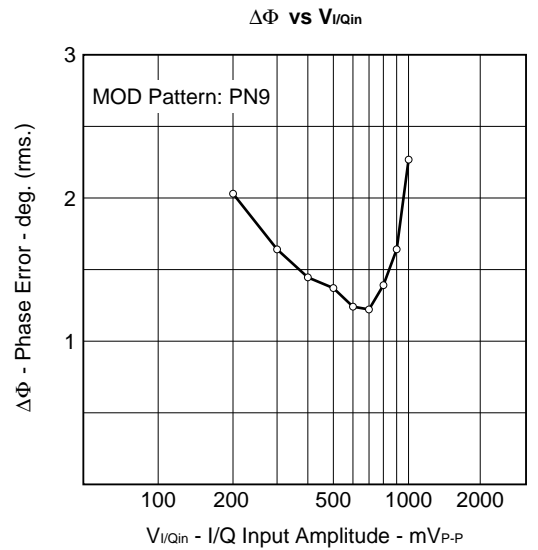
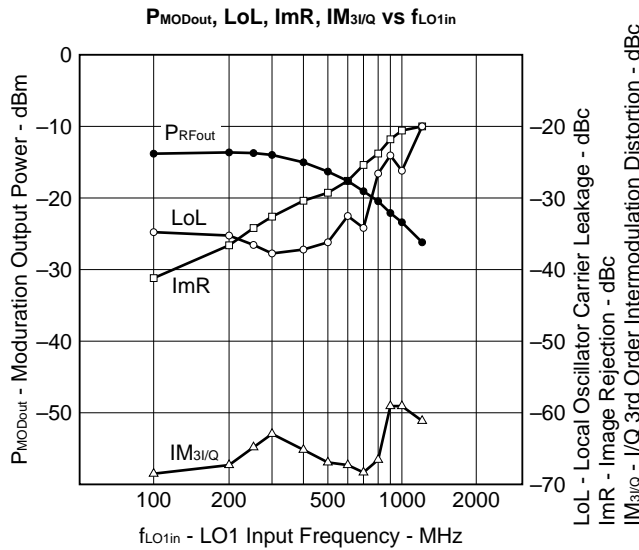
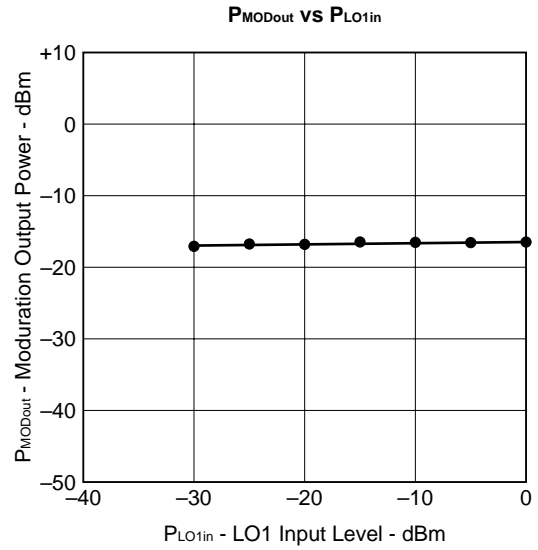
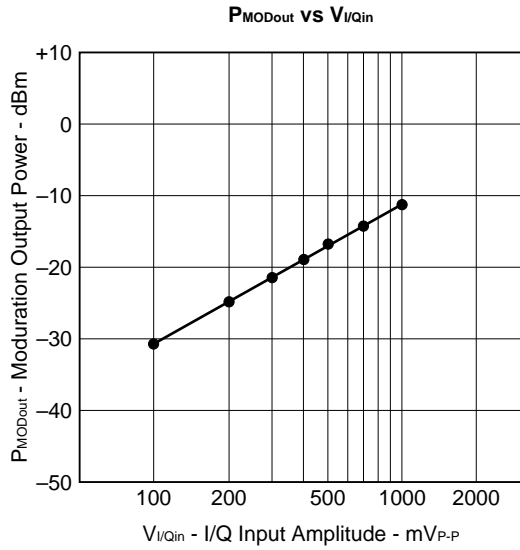
Test Circuit 1 or 2,  $T_A = +25\text{ }^\circ\text{C}$ ,  $V_{CC} = 3\text{ V}$ ,  $V_{PS} = 3\text{ V}$

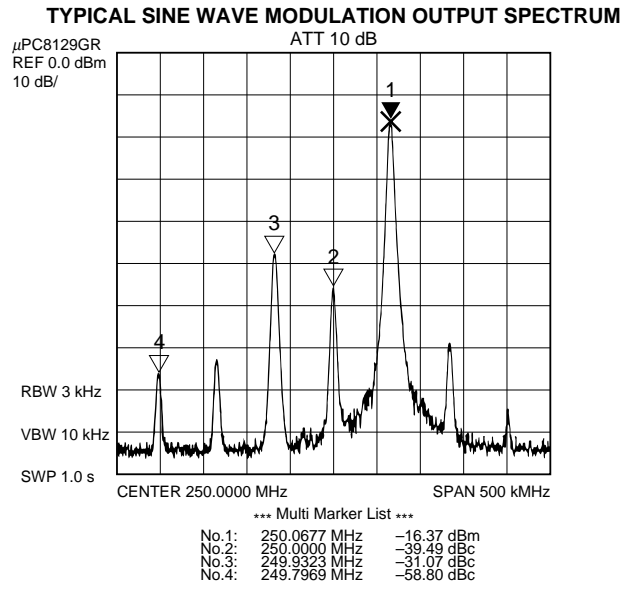
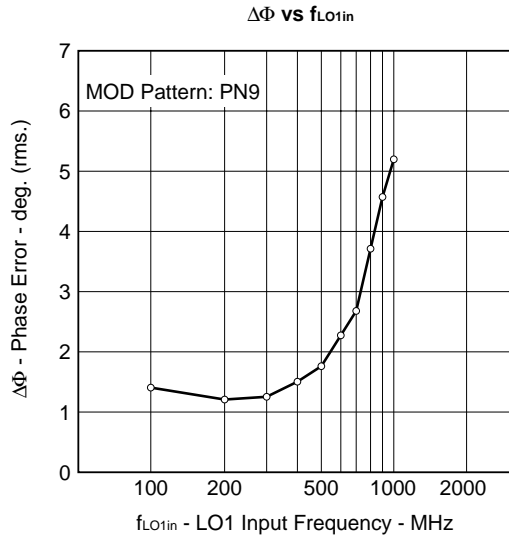
I/Q DC = 1.5 V ( $V_{bias(I)} = V_{bias(Ib)} = V_{bias(Q)} = V_{bias(Qb)} = 1.5\text{ V}$ )

$f_{I/Qin} = 67.7\text{ kHz}$ ,  $V_{I/Qin} = 500\text{ mV}_{P-P}$  (single ended input,  $I_b = Q_b = 0\text{ mV}_{P-P}$ )

Modulation Pattern: All Zero <0000>,  $f_{LO1in} = 500\text{ MHz}$ ,  $P_{LO1in} = -10\text{ dBm}$

$f_{MODout} = f_{LO1in}/2 + f_{I/Qin} = 250\text{ MHz} + f_{I/Qin}$ , Unless Otherwise Specified



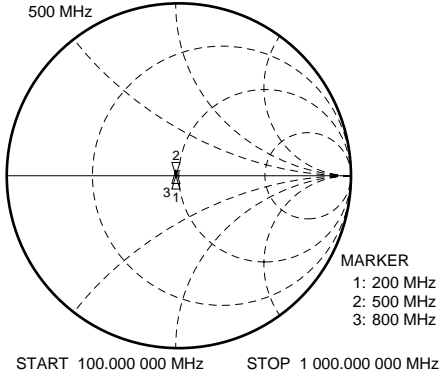


**LO1 INPUT (Pin8) IMPEDANCE**

$V_{CC} = V_{PS} = 3\text{ V}$

CH1 S<sub>11</sub> 1 U FS 2: 47.998 Ω 0.8066 Ω 256.76 pH  
500.000 000 MHz

MARKER 2  
500 MHz

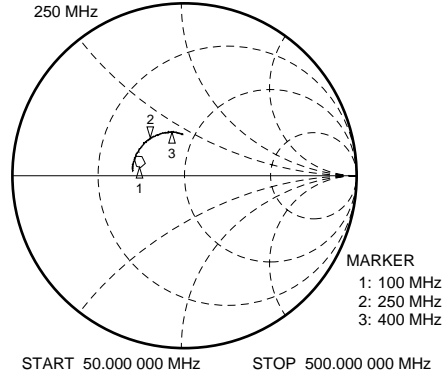


**MOD OUTPUT (Pin3) IMPEDANCE**

$V_{CC} = V_{PS} = 3\text{ V}$

CH1 S<sub>22</sub> 1 U FS 2: 31.195 Ω 14.908 Ω 9.4909 nH  
250.000 000 MHz

MARKER 2  
250 MHz

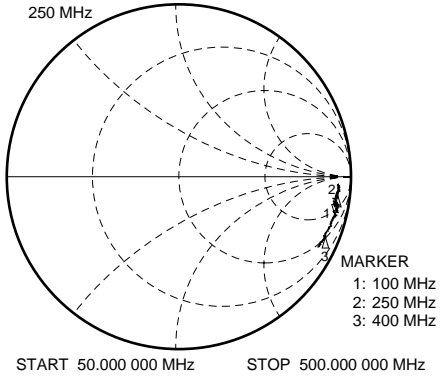


**Up-Con. INPUT (Pin1) IMPEDANCE**

$V_{CC} = V_{PS} = 3\text{ V}$

CH1 S<sub>11</sub> 1 U FS 2: 101.78 Ω -387.03 Ω 1.6449 pF  
250.000 000 MHz

MARKER 2  
250 MHz

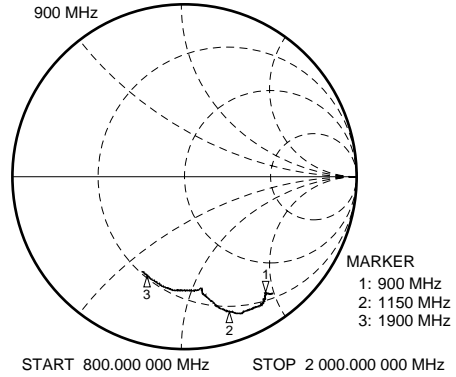


**LO2 INPUT (Pin13) IMPEDANCE**

$V_{CC} = V_{PS} = 3\text{ V}$

CH1 S<sub>11</sub> 1 U FS 1: 22.379 Ω -93.543 Ω 1.8905 pF  
900.000 000 MHz

MARKER 1  
900 MHz



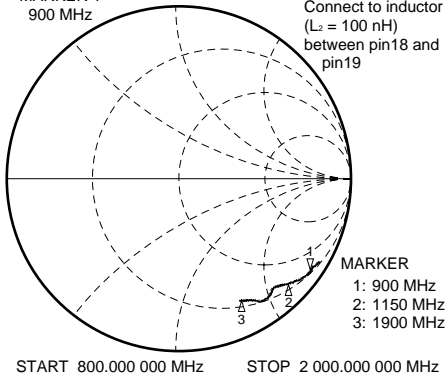
**RF OUTPUT (Pin18) IMPEDANCE**

$V_{CC} = V_{PS} = 3\text{ V}$

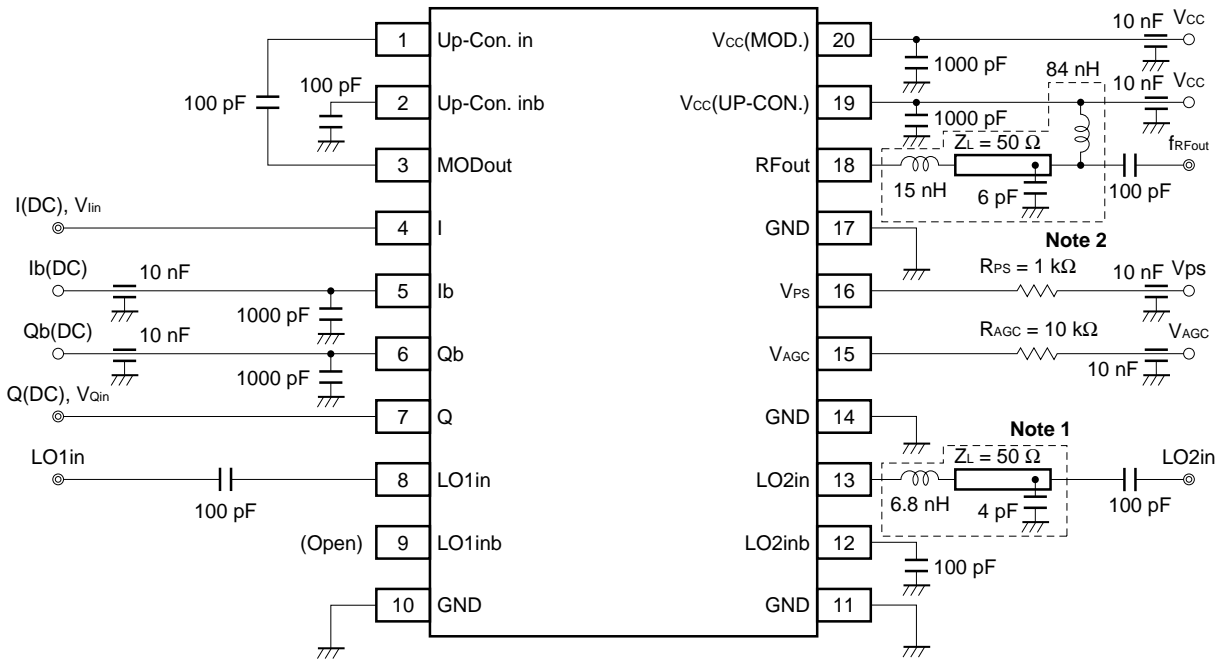
CH1 S<sub>22</sub> 1 U FS 1: 18.953 Ω -158.83 Ω 1.1134 pF  
900.000 000 MHz

MARKER 1  
900 MHz

Connect to inductor  
(L<sub>2</sub> = 100 nH)  
between pin18 and  
pin19

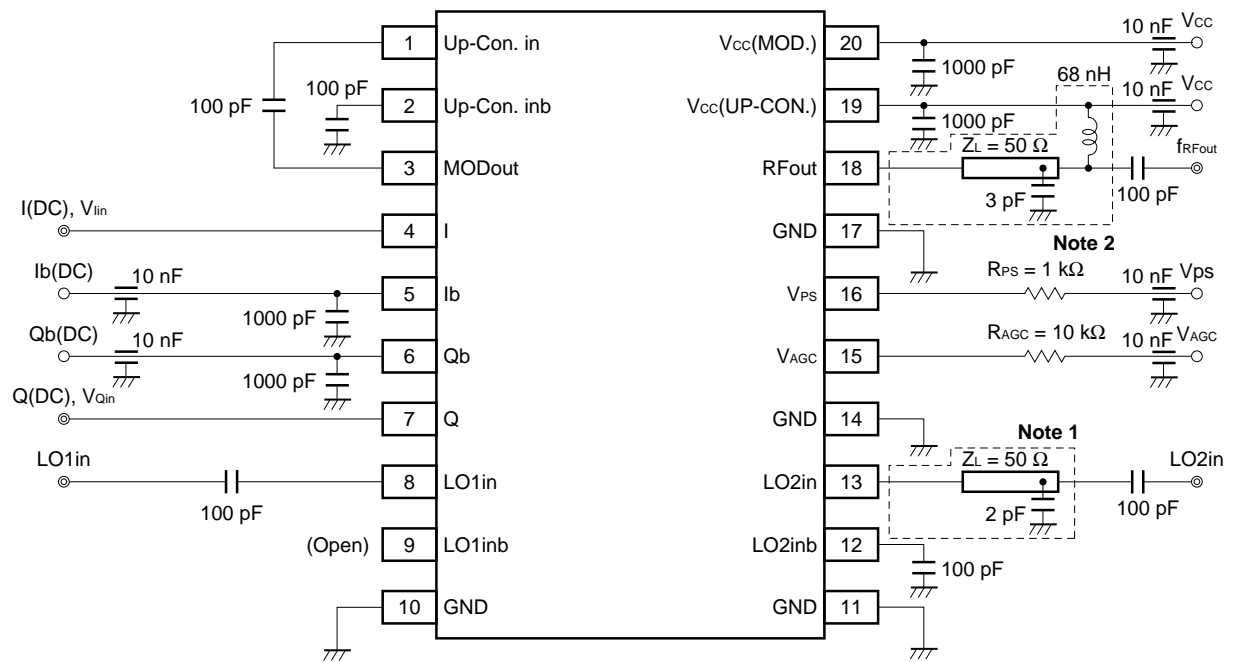


**TEST CIRCUIT 1 (In the case of  $f_{RFout} = 900$  MHz Band)**



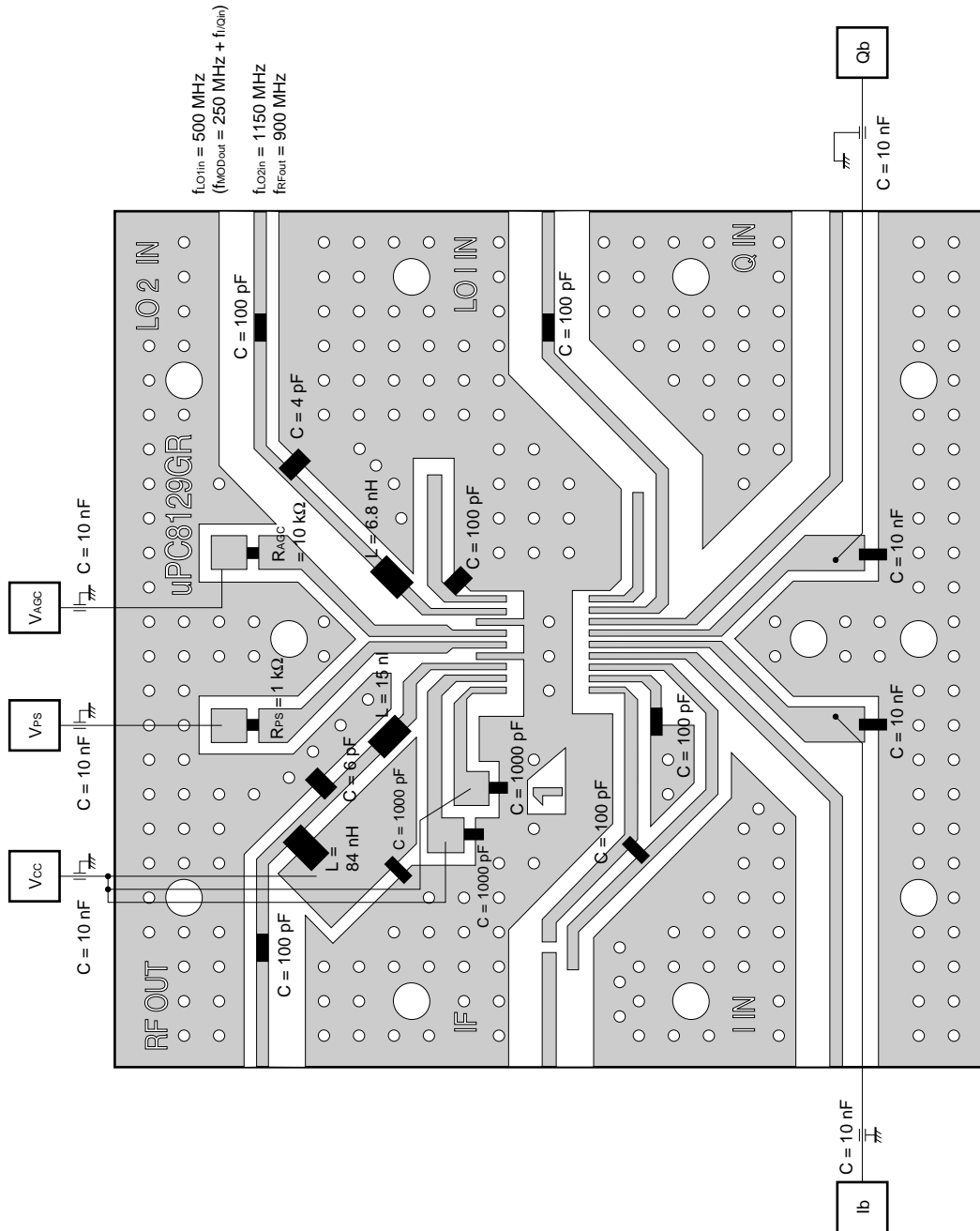
- Notes 1.** 50 Ω matching circuit at  $f_{LO2in} = 1150$  MHz.  
In the case of using NEC's evaluation board.
- 2.** 50 Ω matching circuit at  $f_{RFout} = 900$  MHz.  
In the case of using NEC's evaluation board.

**TEST CIRCUIT 2 (In the case of  $f_{RFout} = 1900$  MHz Band)**



- Notes 1.** 50  $\Omega$  matching circuit at  $f_{LO2in} = 1650$  MHz.  
 In the case of using NEC's evaluation board.
- 2.** 50  $\Omega$  matching circuit at  $f_{RFout} = 1900$  MHz.  
 In the case of using NEC's evaluation board.

EXAMPLE OF TEST CIRCUIT 1 ASSEMBLED ON EVALUATION BOARD

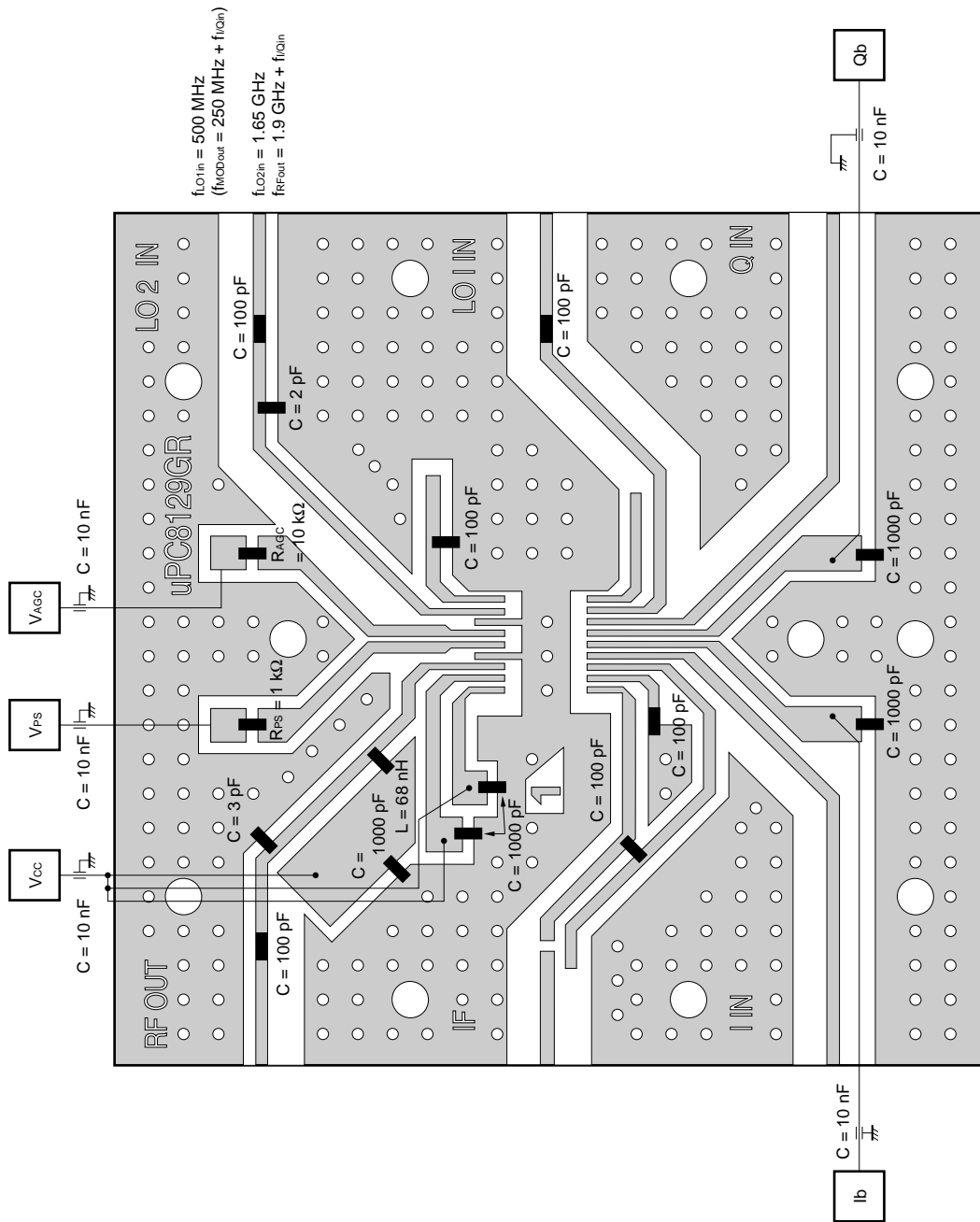


- Notes**
1. Double-sided patterning with 35  $\mu$ m thick copper on 50  $\times$  50  $\times$  0.4 mm polyimide board.
  2. GND pattern on backside.
  3. Solder coating over patterns.
  4.  $\circ$ ,  $\bigcirc$  indicate through-holes.

**NOTICE** The test circuits and board pattern on data sheet are for performance evaluation use only. In the case of actual design-in, matching circuit should be determined using S-parameter of desired frequency in accordance to actual mounting pattern.



EXAMPLE OF TEST CIRCUIT 2 ASSEMBLED ON EVALUATION BOARD

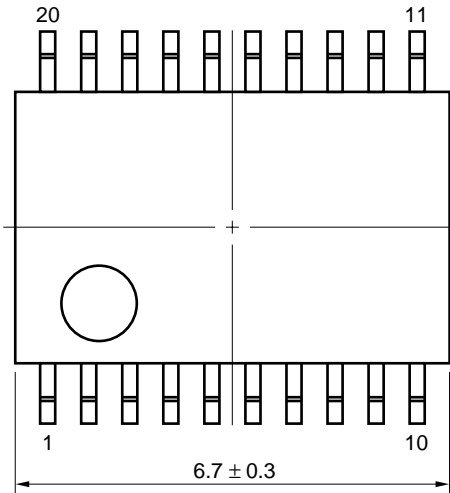


- Notes**
1. Double-sided patterning with 35  $\mu$ m thick copper on polyimide board.
  2. GND pattern on backside.
  3. Solder coating over patterns.
  4.  $\circ$ ,  $\bigcirc$  indicate through-holes.

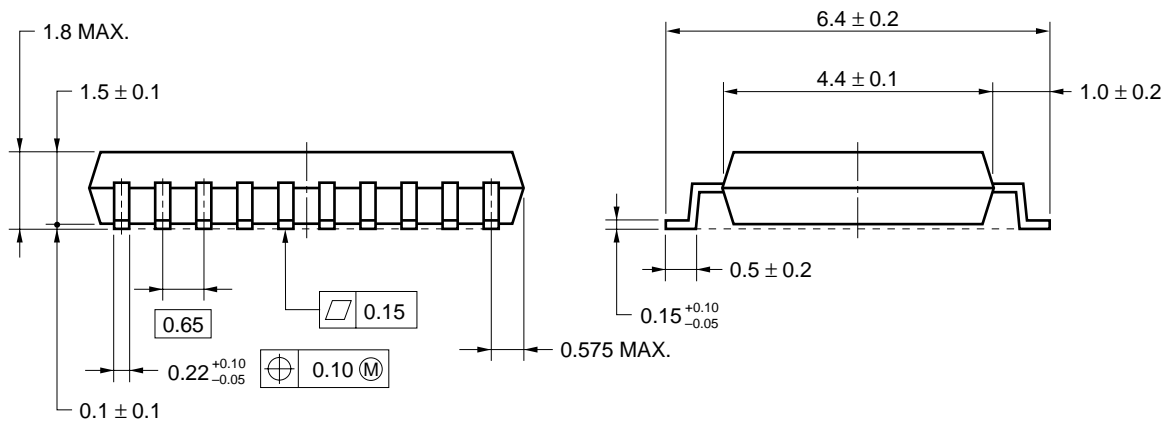
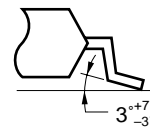
**NOTICE** The test circuits and board pattern on data sheet are for performance evaluation use only. In the case of actual design-in, matching circuit should be determined using S-parameter of desired frequency in accordance to actual mounting pattern.

PACKAGE DIMENSIONS

★ 20 PIN PLASTIC SSOP (225 mil) (UNIT: mm)



detail of lead end



**NOTE** Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

**NOTE ON CORRECT USE**

- (1) Observe precautions for handling because of electrostatic sensitive devices.
- (2) Form a ground pattern as widely as possible to minimize ground impedance (to prevent undesired oscillation).
- (3) Keep the track length of the ground pins as short as possible.
- (4) Connect a bypass capacitor (e.x. 1000 pF) to the Vcc pin.

**RECOMMENDED SOLDERING CONDITIONS**

This product should be soldered in the following recommended conditions. Other soldering method and conditions than the recommended conditions are to be consulted with sales representatives.

**μPC8129GR**

| Soldering process      | Soldering conditions  | Symbol    |
|------------------------|---|-----------|
| Infrared ray reflow    | Peak package's surface temperature: 235 °C or below,<br>Reflow time: 30 seconds or below (210 °C or higher)<br>Number of reflow process: 2, Exposure limit <sup>Note</sup> : None | IR35-00-2 |
| VPS                    | Peak package's surface temperature: 215 °C or below,<br>Reflow time: 40 seconds or below (200 °C or higher)<br>Number of reflow process: 2, Exposure limit <sup>Note</sup> : None | VP15-00-2 |
| Wave soldering         | Solder temperature: 260 °C or below,<br>Flow time: 10 seconds or below,<br>Number of flow process: 1, Exposure limit <sup>Note</sup> : None                                       | WS60-00-1 |
| Partial heating method | Terminal temperature: 300 °C or below,<br>Flow time: 3 seconds/pin or below,<br>Exposure limit <sup>Note</sup> : None   |           |

**Note** Exposure limit before soldering after dry-pack package is opened.  
Storage conditions: 25 °C and relative humidity at 65 % or less.

**Caution** Apply only a single process at once, except for “Partial heating method”.  
For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).

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    - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
    - Specific: Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.
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