R8820

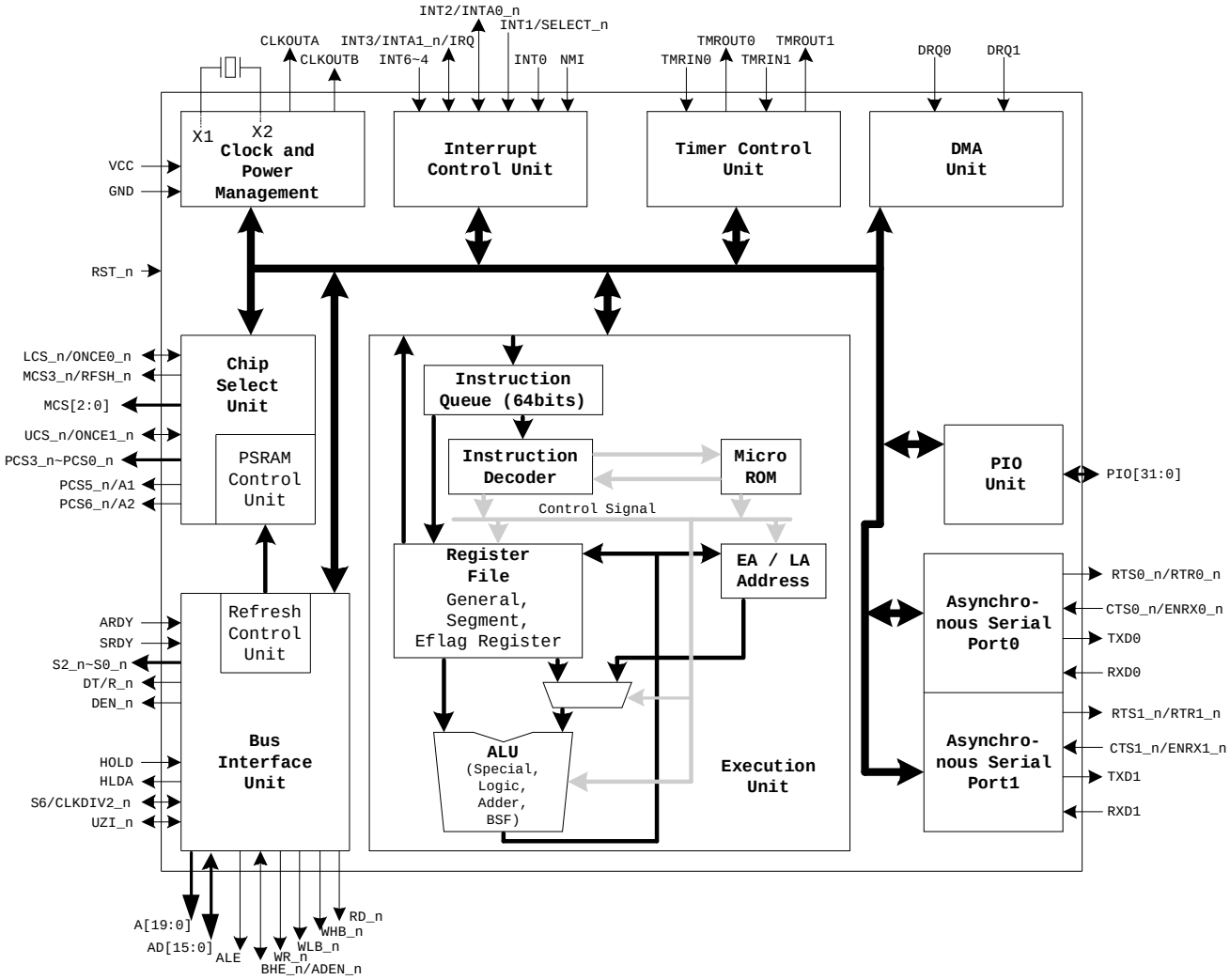
Brief Sheet

16-BIT RISC MICRO CONTROLLER

1. Features

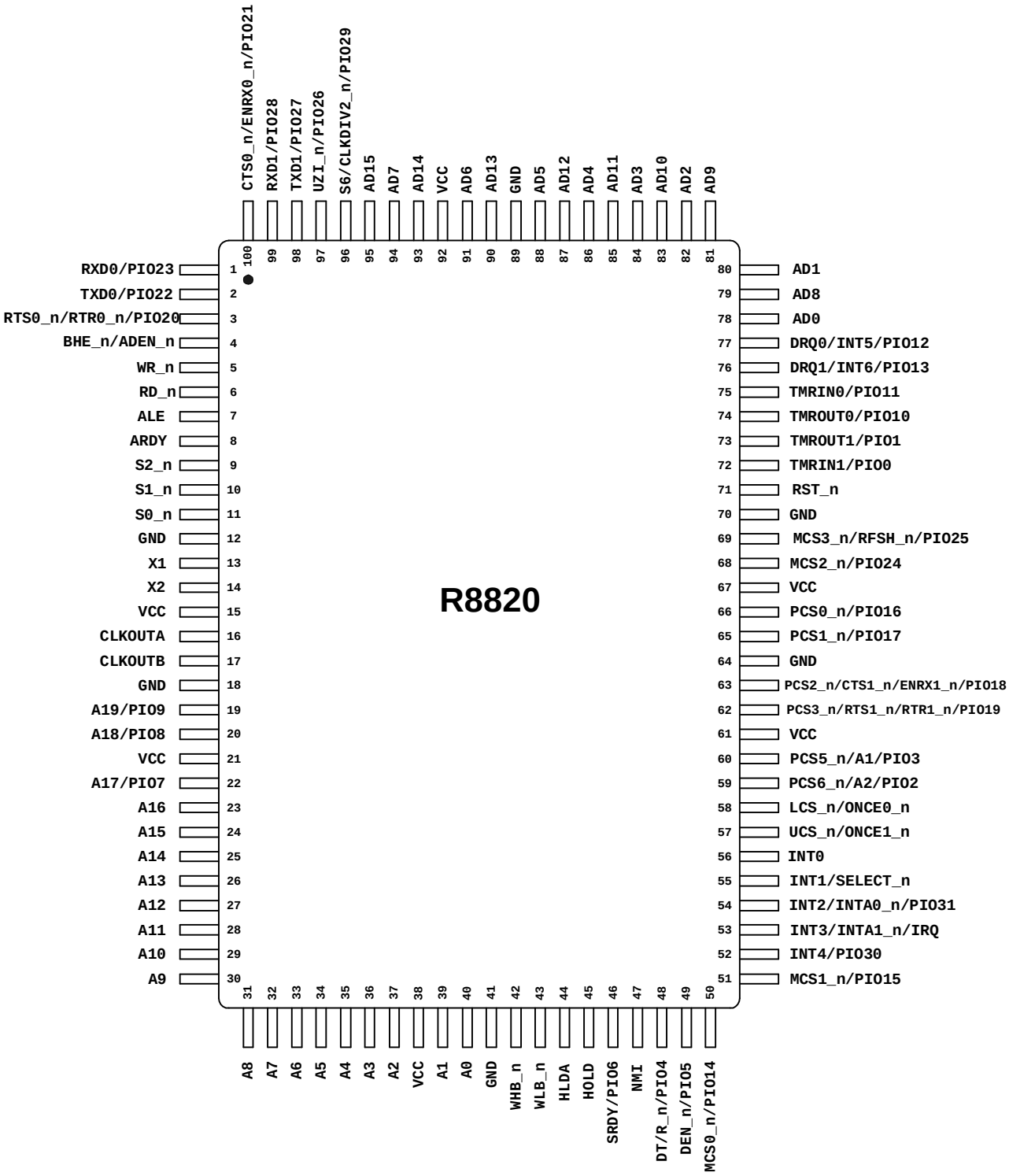
- CPU Core
  - RDC's proprietary RISC architecture
  - Five-stage pipeline
  - CPU clock speed up to 25 MHz
  - Supports CPU ID
  - Supports 32 PIO pins
  - Static & synthesizable design
- Bus Interface
  - A multiplexed address and data bus which is compatible with the 80C186 microprocessor
  - Supports a non-multiplexed address bus A[19:0]
- ROM/RAM Controller and Addressing Space
  - 1M-byte memory address space
  - 64K-byte I/O space
- PSRAM Interface
  - PSRAM (Pseudo static RAM) interface with auto-refresh control
- Two Independent DMA Channels
  - Supports serial ports with DMA transfers
- Asynchronous Serial Channels
  - Supports two asynchronous serial channels with hardware handshaking signals
- Interrupt Controller
  - The interrupt controller with seven maskable external interrupts and one non-maskable external interrupt
- Programmable Chip-select Logic
  - Programmable chip-select logic for memory or I/O bus cycle decoder
- Programmable Wait-state Generators
- Counter/Timers
  - Three independent 16-bit timers and one independent watchdog timer
- Software is compatible with the 80C186 microprocessor
- Operating Voltage Range
  - Core voltage: 5V ± 5%
  - I/O voltage: 5V ± 10%
- Operating Temperature: -40 ~ +85°C
- Package Type
  - 100-pin PQFP
  - 100-pin LQFP
- A Green Product

2. Block Diagram

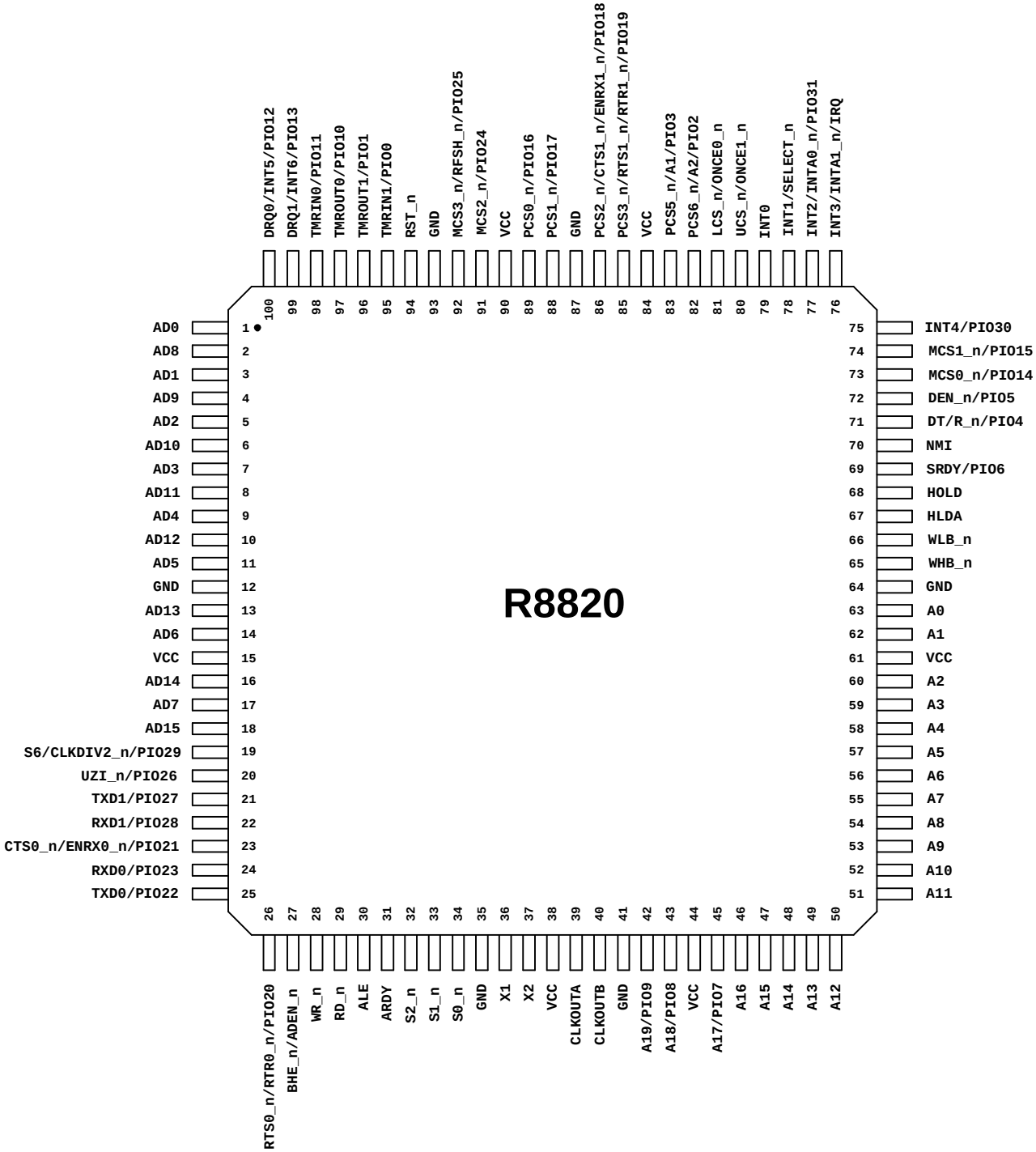


3. PIN Placement

3.1 PQFP 100 pins

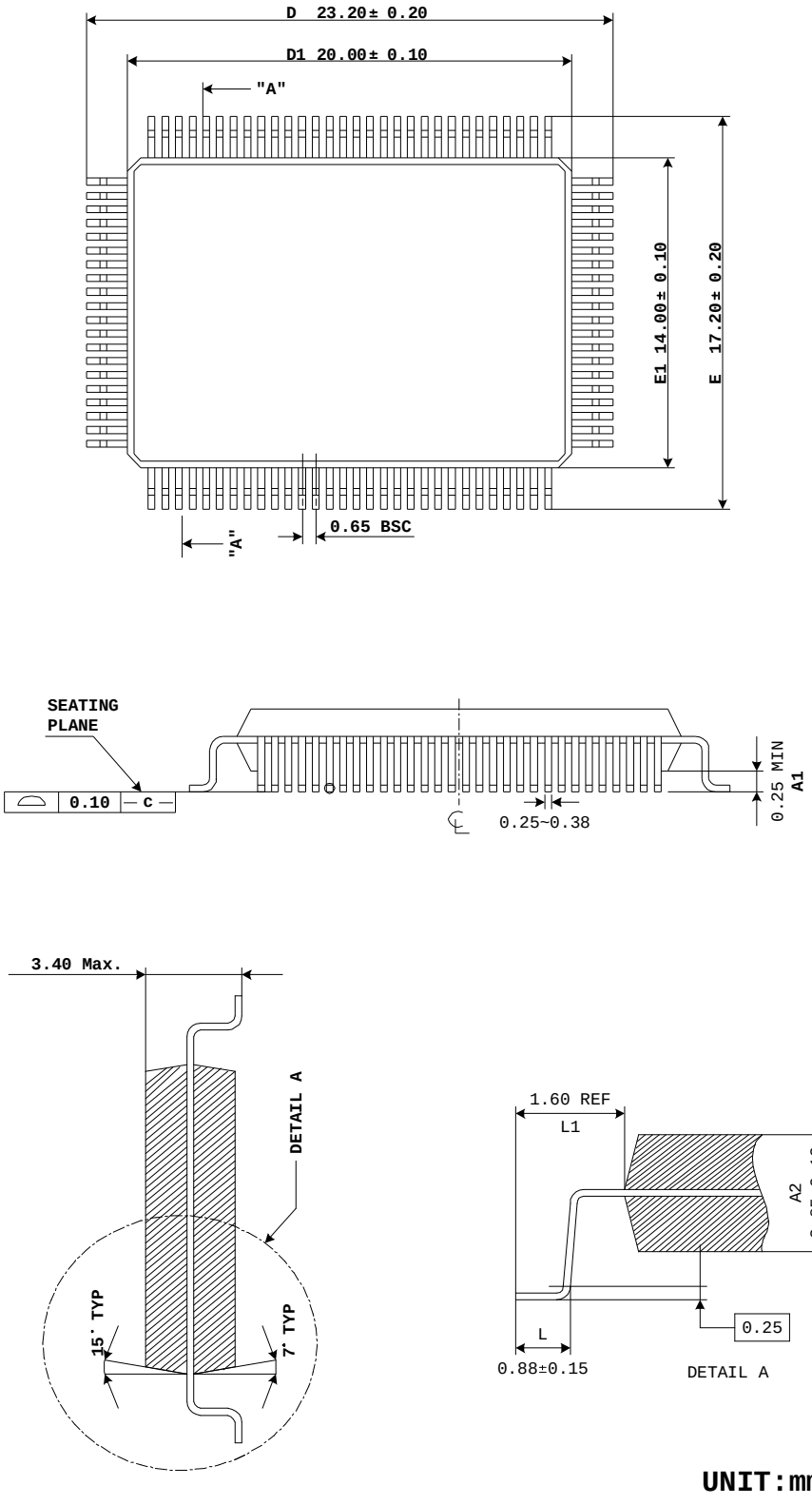


3.2 LQFP 100 pins



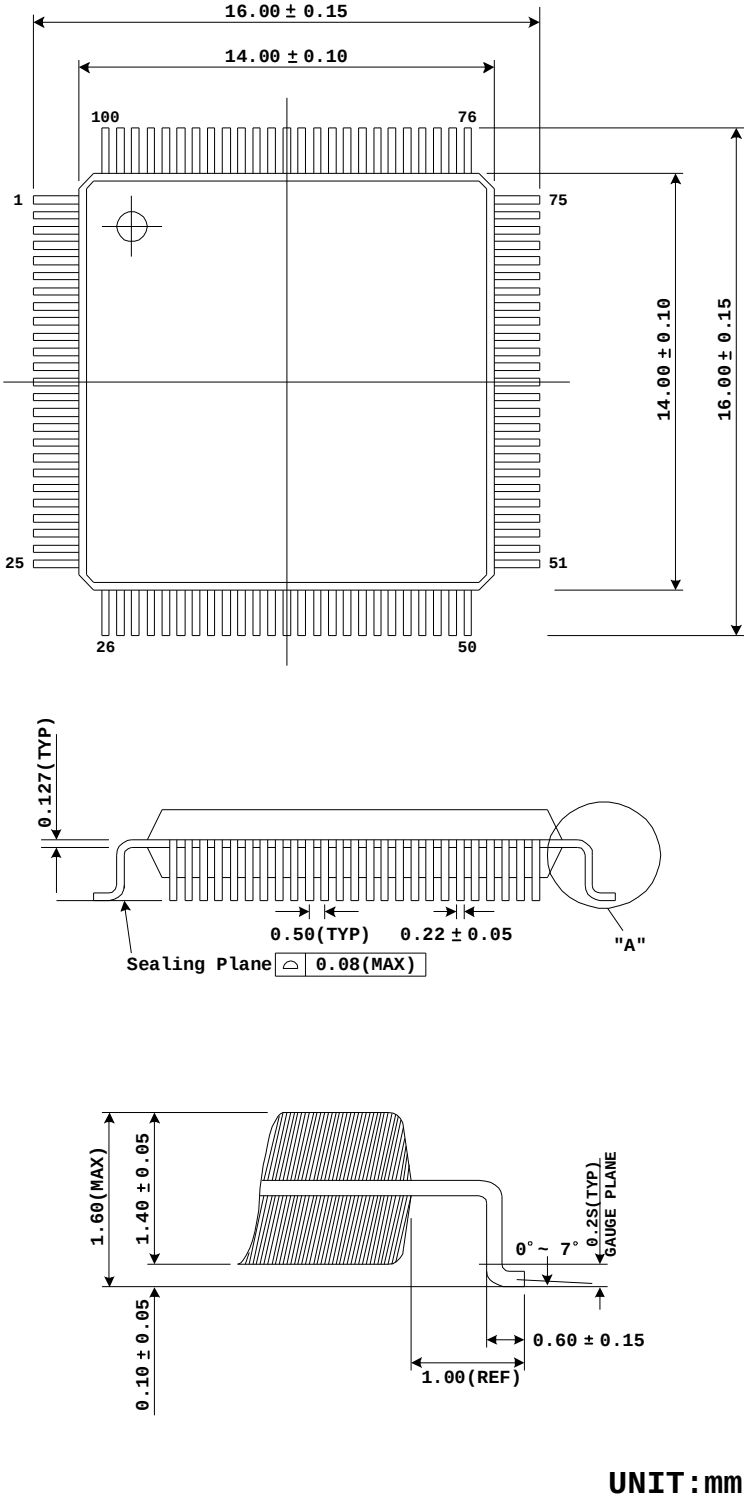
4. Package Information

4.1 PQFP 100 pins



UNIT:mm

4.2 LQFP 100 pins



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