

NP74N04YUG

MOS FIELD EFFECT TRANSISTOR

R07DS0017EJ0100 Rev.1.00 Jul 01, 2010

Description

The NP74N04YUG is N-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Low on-state resistance
 - --- $R_{DS(on)}$ = 5.5 mΩ MAX. (V_{GS} = 10 V, I_D = 37.5 A)
- Low Ciss: Ciss = 3620 pF TYP. $(V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V})$
- Designed for automotive application and AEC-Q101 qualified
- Small size package 8-pin HSON

Ordering Information

Ī	Part No.	LEAD PLATING	PACKING	Package
Ī	NP74N04YUG -E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	8-pin HSON, Taping (E1 type)
	NP74N04YUG -E2-AY *1			8-pin HSON, Taping (E2 type)

Note: *1. Pb-free (This product does not contain Pb in the external electrode.)

Absolute Maximum Ratings ($T_A = 25$ °C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V _{GS} = 0 V)	V _{DSS}	40	V
Gate to Source Voltage (V _{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T _C = 25°C)	I _{D(DC)}	±75	Α
Drain Current (pulse) *1	I _{D(pulse)}	±225	Α
Total Power Dissipation (T _C = 25°C)	P _{T1}	120	W
Total Power Dissipation (T _A = 25°C) *2	P _{T2}	1.0	W
Channel Temperature	T _{ch}	175	°C
Storage Temperature	T _{stg}	-55 to +175	°C
Repetitive Avalanche Current *3	I _{AR}	32	Α
Repetitive Avalanche Energy *3	E _{AR}	102	mJ

Thermal Resistance

Notes: *1. $T_C = 25^{\circ}C$, PW $\leq 10 \mu s$, Duty Cycle $\leq 1\%$

*2. Mounted on glass epoxy substrate of 40 mm x 40 mm x 0.8 mmt

*3. $T_{ch(peak)} \le 150^{\circ}C$, $R_G = 25 \Omega$

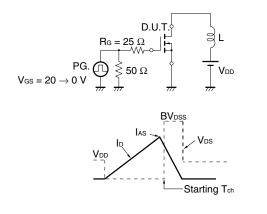
Electrical Characteristics (T_A = 25°C)

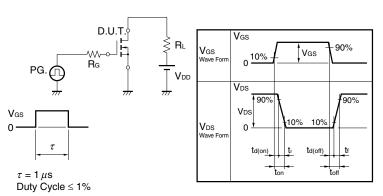
Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}			1	μΑ	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$
Gate Leakage Current	I _{GSS}			±100	nA	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$
Gate to Source Threshold Voltage	$V_{GS(th)}$	2.0	3.0	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$
Forward Transfer Admittance *1	y _{fs}	21	42		S	$V_{DS} = 5 \text{ V}, I_{D} = 37.5 \text{ A}$
Drain to Source On-state Resistance *1	R _{DS(on)}		4.2	5.5	mΩ	V_{GS} = 10 V, I_{D} = 37.5 A
Input Capacitance	C _{iss}		3620	5430	pF	$V_{DS} = 25 V$,
Output Capacitance	Coss		330	500	pF	$V_{GS} = 0 V$,
Reverse Transfer Capacitance	C _{rss}		220	400	pF	f = 1 MHz
Turn-on Delay Time	$t_{d(on)}$		26	52	ns	$V_{DD} = 20 \text{ V}, I_D = 37.5 \text{ A},$
Rise Time	t _r		10	25	ns	V_{GS} = 10 V ,
Turn-off Delay Time	$t_{d(off)}$		62	124	ns	$R_G = 0 \Omega$
Fall Time	t _f		6	15	ns	
Total Gate Charge	Q_G		64	96	nC	$V_{DD} = 32 V$,
Gate to Source Charge	Q_{GS}		17		nC	V_{GS} = 10 V ,
Gate to Drain Charge	Q_{GD}		21		nC	I _D = 75 A
Body Diode Forward Voltage *1	$V_{F(S-D)}$		0.94	1.5	V	I _F = 75 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}		38		ns	I _F = 75 A, V _{GS} = 0 V,
Reverse Recovery Charge	Q _{rr}		44		nC	di/dt = 100 A/μs

Note: *1. Pulsed

TEST CIRCUIT 1 AVALANCHE CAPABILITY

TEST CIRCUIT 2 SWITCHING TIME

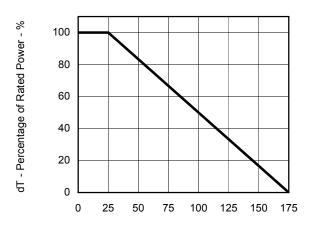




TEST CIRCUIT 3 GATE CHARGE

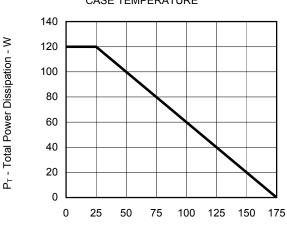
Typical Characteristics ($T_A = 25^{\circ}C$)

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



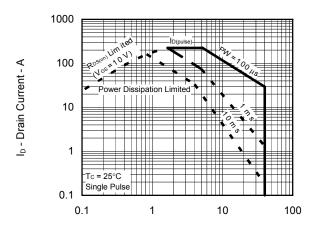
T_C - Case Temperature - °C

TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



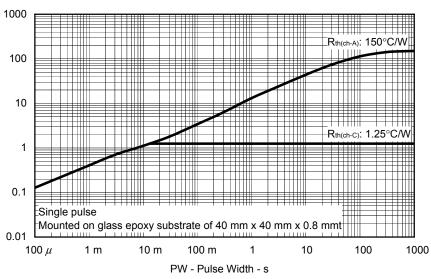
T_C - Case Temperature - °C

FORWARD BIAS SAFE OPERATING AREA



 V_{DS} - Drain to Source Voltage - V

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

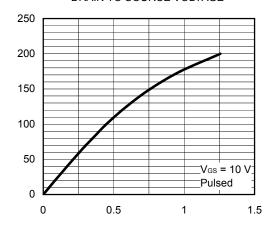




I_D - Drain Current - A

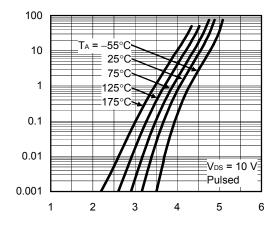
V_{GS(th)} - Gate to Source Threshold Voltage - V





 V_{DS} - Drain to Source Voltage - V

FORWARD TRANSFER CHARACTERISTICS

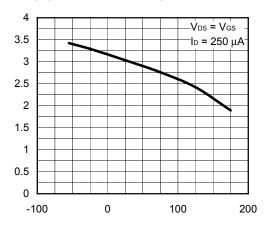


I_D - Drain Current - A

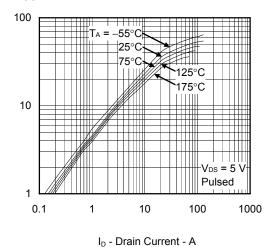
y_{fs} | - Forward Transfer Admittance - S

 V_{GS} - Gate to Source Voltage - V

GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE

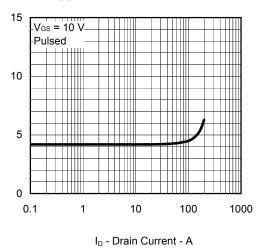


FORWARD TRANSFER ADMITTANCE vs. DRAIN **CURRENT**

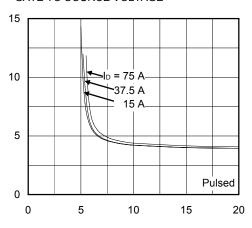


T_{ch} - Channel Temperature - °C

DRAIN TO SOURCE ON-STATE RESISTANCE vs. **DRAIN CURRENT**



DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



 V_{GS} - Gate to Source Voltage - V

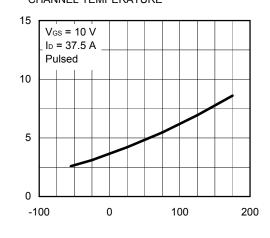
 $\mathsf{R}_{\mathsf{DS}(\mathsf{on})}$ - Drain to Source On-state Resistance - $m\Omega$

 $R_{\text{DS}(\text{on})}$ - Drain to Source On-state Resistance - $m\Omega$

t_{d(on)}, t_r, t_{d(off)}, t_f - Switching Time - ns

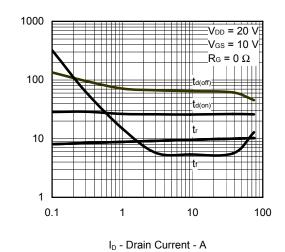
I_F - Diode Forward Current - A

DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

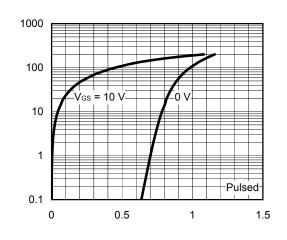


T_{ch} - Channel Temperature - °C

SWITCHING CHARACTERISTICS

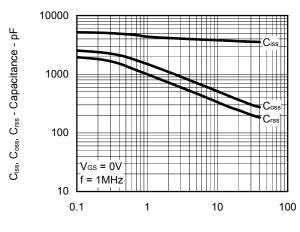


SOURCE TO DRAIN DIODE FORWARD VOLTAGE



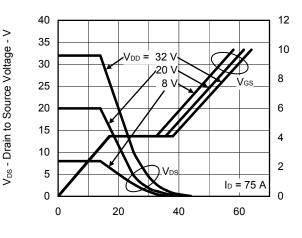
 $V_{F(S\text{-}D)}$ - Source to Drain Voltage - V

CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



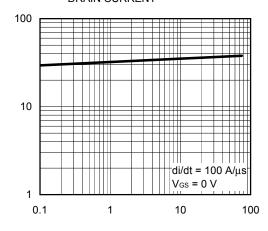
V_{DS} - Drain to Source Voltage - V

DYNAMIC INPUT/OUTPUT CHARACTERISTICS



Q_G - Gate Charge - nC

REVERSE RECOVERY TIME vs. DRAIN CURRENT

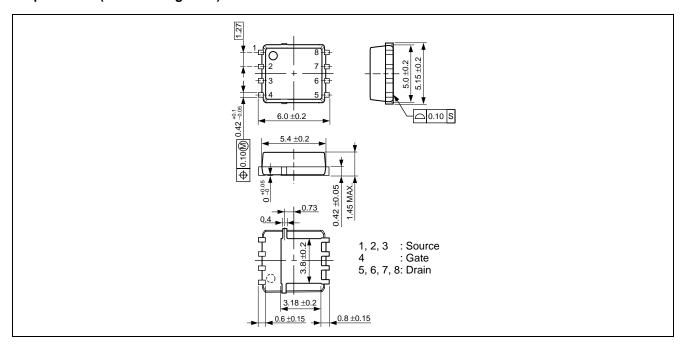


I_F - Drain Current - A

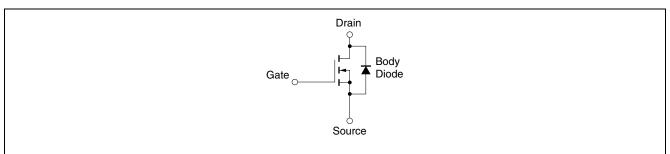
t_{rr} - Reverse Recovery Time - ns

Package Drawings (Unit: mm)

8-pin HSON (Mass: 0.13 g TYP.)



Equivalent Circuit



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Revision History NP74N04YUG

		Description				
Rev.	Date	Page	ge Summary			
1.00	Jul 01, 2010	-	First Eddition Issued			

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