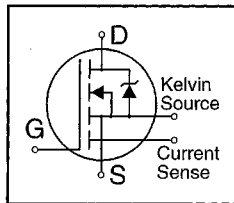


HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Current Sense
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements

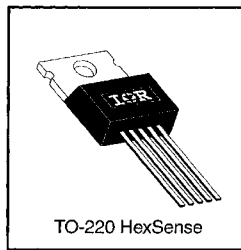


$V_{DSS} = 200V$   
 $R_{DS(on)} = 0.40\Omega$   
 $I_D = 9.0A$

**Description**

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The HEXSense device provides an accurate fraction of the drain current through the additional two leads to be used for control or protection of the device. These devices exhibit similar electrical and thermal characteristics as their IRF-series equivalent part numbers. The provision of a kelvin source connection effectively eliminates problems of common source inductance when the HEXSense is used as a fast, high-current switch in non current-sensing applications.



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**Absolute Maximum Ratings**

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	9.0	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	5.7	
$I_{DM}$	Pulsed Drain Current ①	36	
$P_D @ T_C = 25^\circ C$	Power Dissipation	74	W
	Linear Derating Factor	0.59	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy ②	150	mJ
$I_{AR}$	Avalanche Current ①	9.0	A
$E_{AR}$	Repetitive Avalanche Energy ①	7.4	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf·in (1.1 N·m)	

**Thermal Resistance**

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	1.7	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62	

# IRC630



## Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

Parameter	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	200	—	—	V	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA
ΔV <sub>(BR)DSS/ΔT<sub>J</sub></sub>	Breakdown Voltage Temp. Coefficient	—	0.24	—	V/°C	Reference to 25°C, I <sub>D</sub> =1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	0.40	Ω	V <sub>GS</sub> =10V, I <sub>D</sub> =5.4A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA
g <sub>fs</sub>	Forward Transconductance	2.6	—	—	S	V <sub>DS</sub> =50V, I <sub>D</sub> =5.4A ④
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	25	μA	V <sub>DS</sub> =200V, V <sub>GS</sub> =0V
		—	—	250	μA	V <sub>DS</sub> =160V, V <sub>GS</sub> =0V, T <sub>J</sub> =125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>DS</sub> =20V
	Gate-to-Source Reverse Leakage	—	—	-100	nA	V <sub>GS</sub> =-20V
Q <sub>g</sub>	Total Gate Charge	—	—	43	nC	I <sub>D</sub> =5.9A
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	7.0	nC	V <sub>DS</sub> =160V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	—	23	nC	V <sub>GS</sub> =10V See Fig. 6 and 13 ④
t <sub>d(on)</sub>	Turn-On Delay Time	—	9.4	—	ns	V <sub>DD</sub> =100V I <sub>D</sub> =5.9A R <sub>G</sub> =12Ω R <sub>D</sub> =16Ω See Figure 10 ④
t <sub>r</sub>	Rise Time	—	28	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	39	—		
t <sub>f</sub>	Fall Time	—	20	—		
L <sub>D</sub>	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L <sub>S</sub>	Internal Source Inductance	—	7.5	—		
C <sub>iss</sub>	Input Capacitance	—	800	—	pF	V <sub>GS</sub> =0V V <sub>DS</sub> =25V f=1.0MHz See Figure 5
C <sub>oss</sub>	Output Capacitance	—	240	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	76	—		
r	Current Sensing Ratio	1410	—	1570	—	I <sub>D</sub> =9.0A, V <sub>GS</sub> =10V
C <sub>oss</sub>	Output Capacitance of Sensing Cells	—	9.0	—	pF	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V, f=1.0MHz

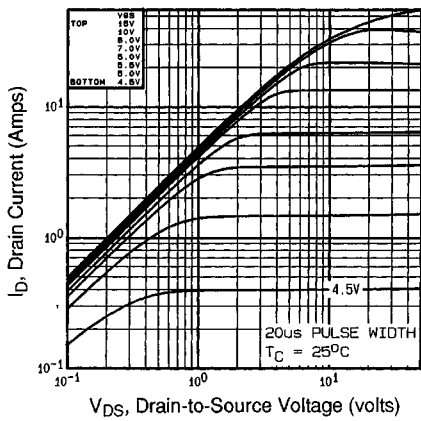


## Source-Drain Ratings and Characteristics

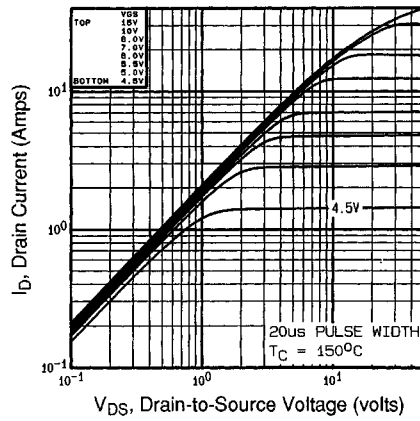
Parameter	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	9.0	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	36		
V <sub>SD</sub>	Diode Forward Voltage	—	—	2.0	V	T <sub>J</sub> =25°C, I <sub>S</sub> =9.0A, V <sub>GS</sub> =0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	170	340	ns	T <sub>J</sub> =25°C, I <sub>F</sub> =5.9A
Q <sub>rr</sub>	Reverse Recovery Charge	—	1.1	2.2	μC	di/dt=100A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ② V<sub>DD</sub>=50V, starting T<sub>J</sub>=25°C, L=2.8mH, R<sub>G</sub>=25Ω, I<sub>AS</sub>=9.0A (See Figure 12)
- ③ I<sub>SD</sub>≤9.0A, di/dt≤120A/μs, V<sub>DD</sub>≤V<sub>(BR)DSS</sub>, T<sub>J</sub>≤150°C
- ④ Pulse width ≤ 300 μs; duty cycle ≤2%.

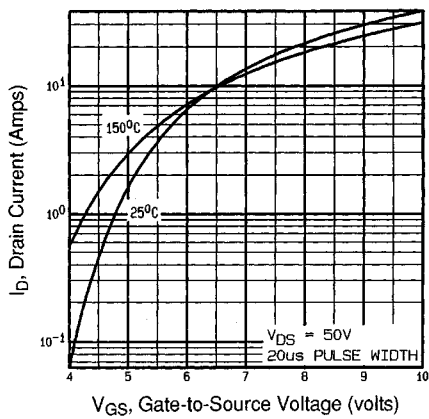


**Fig 1.** Typical Output Characteristics,  $T_C=25^\circ\text{C}$

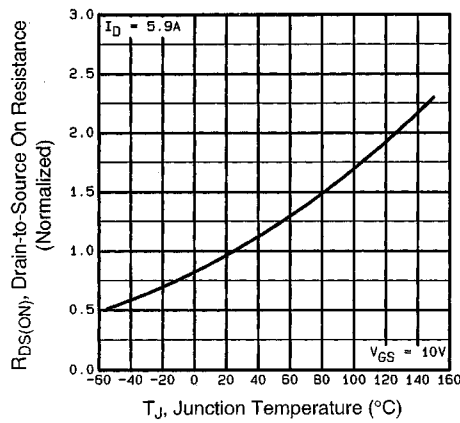


**Fig 2.** Typical Output Characteristics,  $T_C=150^\circ\text{C}$

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**Fig 3.** Typical Transfer Characteristics



**Fig 4.** Normalized On-Resistance Vs. Temperature

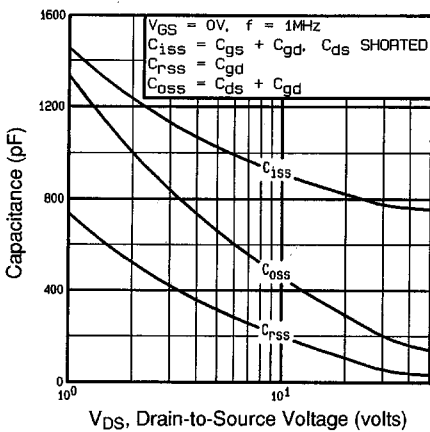


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

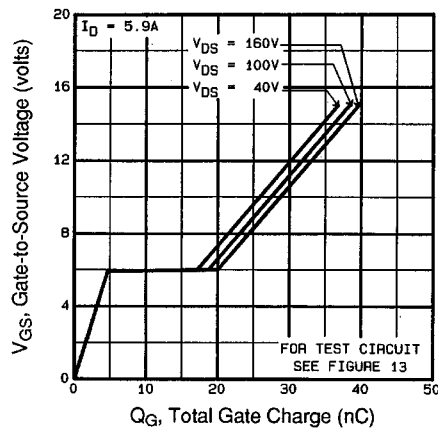


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

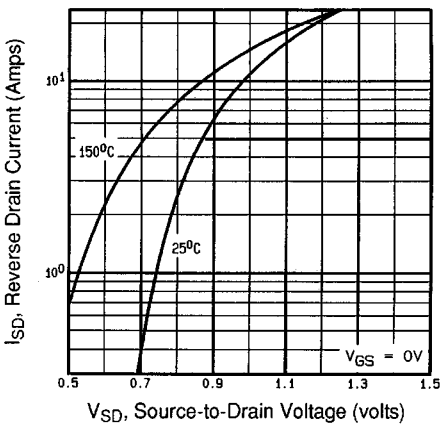


Fig 7. Typical Source-Drain Diode Forward Voltage

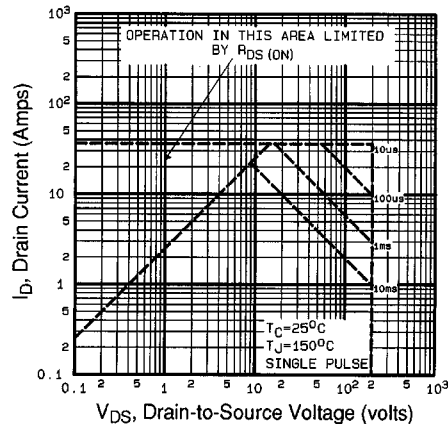


Fig 8. Maximum Safe Operating Area

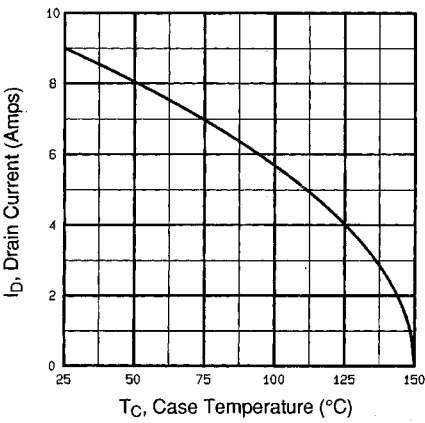


Fig 9. Maximum Drain Current Vs. Case Temperature

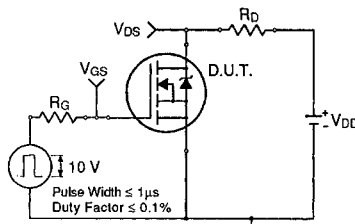


Fig 10a. Switching Time Test Circuit

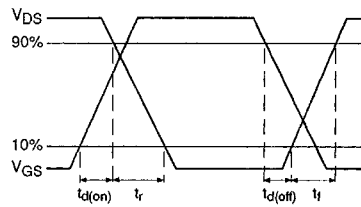


Fig 10b. Switching Time Waveforms

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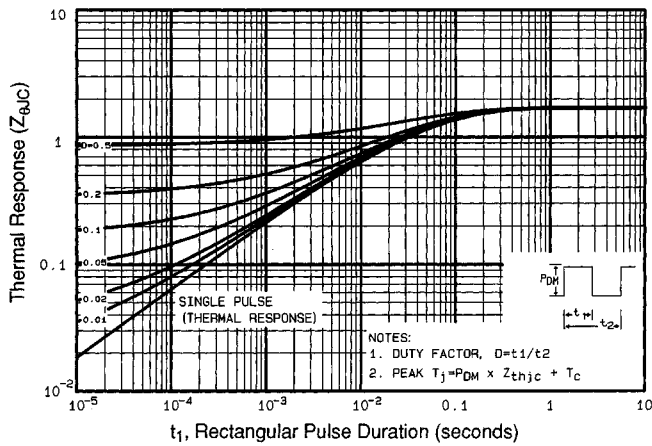


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

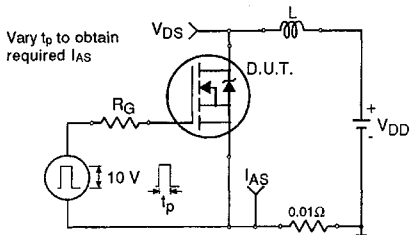


Fig 12a. Unclamped Inductive Test Circuit

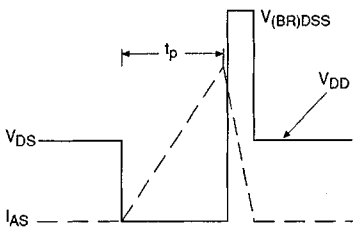


Fig 12b. Unclamped Inductive Waveforms

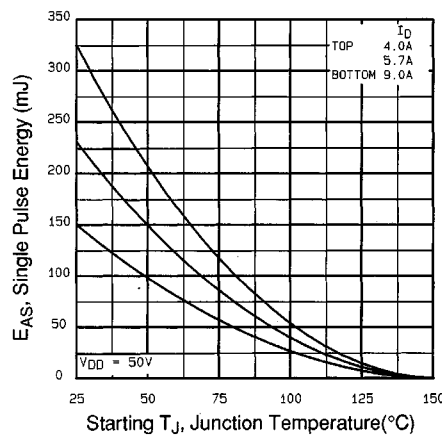


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

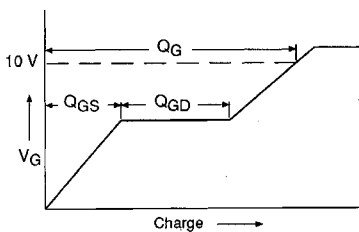


Fig 13a. Basic Gate Charge Waveform

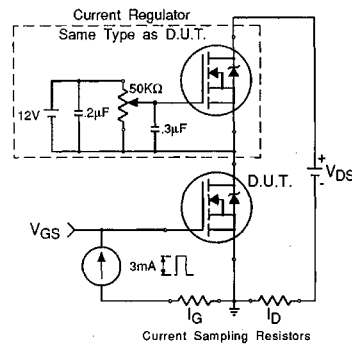
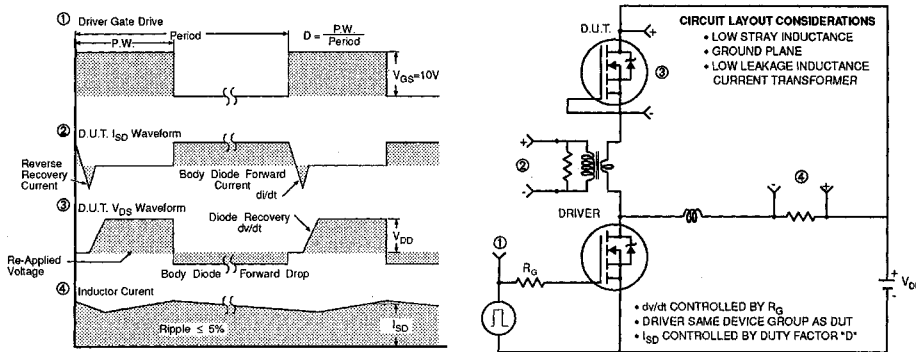
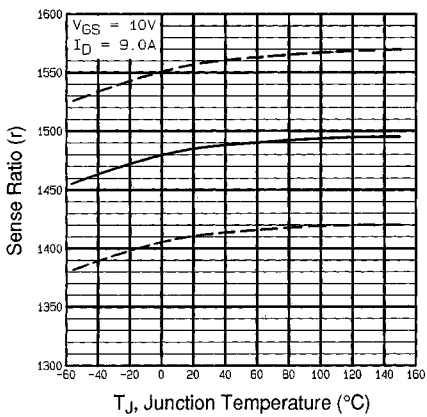


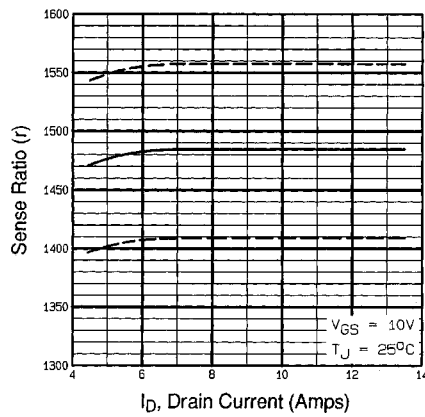
Fig 13b. Gate Charge Test Circuit



**Fig 14. Peak Diode Recovery dv/dt Test Circuit**



**Fig 15. Typical HEXSense Ratio Vs. Junction Temperature**



**Fig 16. Typical HEXSense Ratio Vs. Drain Current**

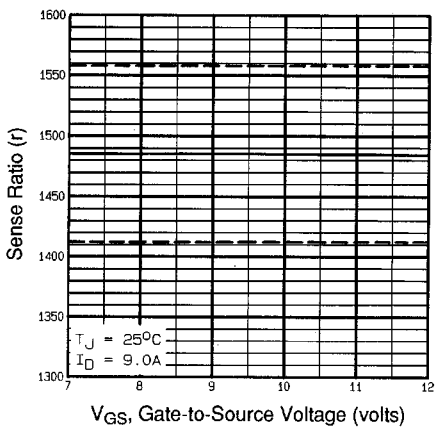
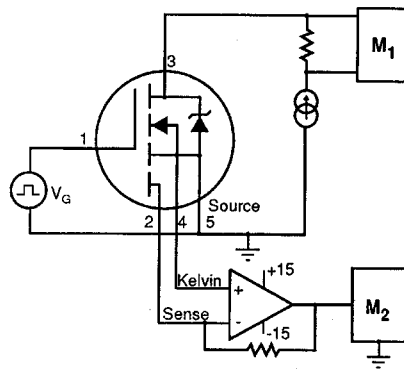


Fig 17. Typical HEXSense Ratio Vs. Gate Voltage



M1, M2 = HIGH SPEED DIGITAL VOLTMETERS

Fig 18. HEXSense Ratio Test Circuit

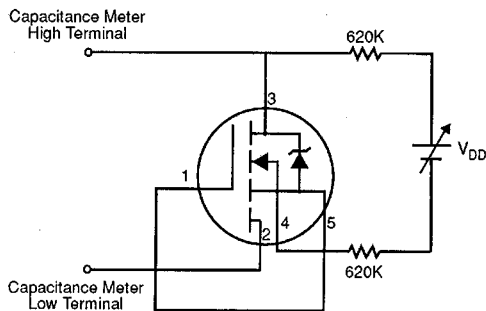


Fig 19. HEXSense Sensing Cell Output Capacitance Test Circuit

Appendix B: Package Outline Mechanical Drawing – See page 1510

Appendix C: Part Marking Information – See page 1517