REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27						
REV STATUS OF SHEETS				REV															
				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

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AMSC N/A

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DRAWING APPROVAL DATE
94-09-28

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS, 8-BIT MEMORY PROCESSING UNIT, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-94537
B	67268	

SHEET 1 OF 27

DESC FORM 193
JUL 91

5962-E163-94

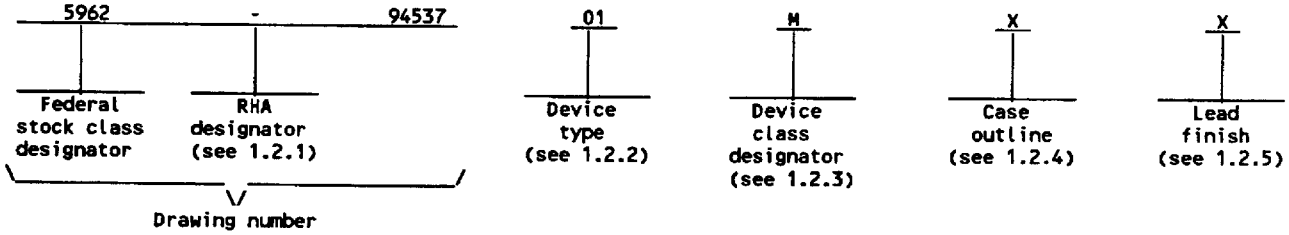
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

9004708 0007816 567

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	Z80180-8	8-bit Memory processing unit

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA15-P68	68	pin grid array

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.3 V dc to +7.0 V dc
Input voltage range (V_{IN})	-0.3 V dc to V_{CC} + 0.3 V dc
Maximum power dissipation (P_D):	
Normal operation	330 mW
System stop mode	96.25 mW
Operating junction temperature	145°C
Operating case temperature	-55°C to +125°C
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 5 seconds)	275°C
Thermal resistance, junction to case (θ_{JC})	See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage range	+4.5 V dc to +5.5 V dc
Case operating temperature range	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 2/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Values will be added when they become available.

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be specified when applicable.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-I-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ $4.5V \le V_{CC} \le 5.5V$, $V_{SS}=0.0V$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
High level input voltage RESET, EXTAL, NMI	V_{IH1}	V_{CC} = 4.5V	1,2,3	V_{CC}-0.6	V_{CC}+0.3	V
High level input voltage except RESET, EXTAL, NMI	V_{IH2}			2.0	V_{CC}+0.3	
Low level input voltage RESET, EXTAL, NMI	V_{IL1}			-0.3	0.6	
Low level input voltage except RESET, EXTAL, NMI	V_{IL2}			-0.3	0.8	
High level ouput voltage	V_{OH}	I_{OH} = -200 µA, V_{CC} = 4.5V		2.4		
		I_{OH} = -20 µA, V_{CC} = 4.5V		V_{CC}-1.2		
Low level ouput voltage	V_{OL}	I_{OL} = 2.2 mA, V_{CC} = 4.5V			0.45	
High level ouput voltage EXTAL, E	V_{OHC}	I_{OH} = -200 µA, V_{CC} = 4.5V		V_{CC}-0.6		
Low level ouput voltage EXTAL, E	V_{OLC}	I_{OL} = 2.2 mA, V_{CC} = 4.5V			0.4	
Input leakage current All inputs except XTAL, EXTAL	I_{IL}	$0.5 V \le V_{IN} \le V_{CC}$-0.5V V_{CC} = 5.5V			1.0	µA
Three state leakage current	I_{TL}				1.0	
Supply current	I_{CC}	f = 8 MHz, P_D in Normal operation, V_{CC} = 5.5V			60	mA
		f = 8 MHz, P_D in System stop mode, V_{CC} = 5.5V			17.5	
Pin capacitance	C_P	see 4.4.1c V_{IN} = 0.0V, f = 1 MHz			12	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ $4.5V \le V_{CC} \le 5.5V$, $V_{SS}=0.0V$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Functional tests		See 4.4.1b	7, 8			
Clock cycle time	t_{CYC} (1)	See figure 3 V_{CC} = 4.5 V	9,10,11	125	2000	ns
Clock high pulse width	t_{CHW} (2)			50		
Clock low pulse width	t_{CLW} (3)			50		
Clock fall time	t_{CF} (4)				15	
Clock rise time	t_{CR} (5)				15	
ϕ ↑ to address valid delay	t_{AD} (6)				80	
Address valid to $\overline{MREQ}$ ↓ or $\overline{IORQ}$ ↓	t_{AS} (7)			20		
ϕ ↓ to $\overline{MREQ}$ ↓ delay	t_{MED1} (8)				50	
ϕ ↓ to $\overline{RD}$ ↓ delay, I_{OC} = 1	t_{RDD1} (9)				50	
ϕ ↑ to $\overline{RD}$ ↓ delay, I_{OC} = 0	t_{RDD1} (9)				60	
ϕ ↑ to $\overline{M1}$ ↓ delay	t_{M1D1} (10)				70	
Address hold time from $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, $\overline{WR}$	t_{AH} (11)			20		
ϕ ↓ to $\overline{MREQ}$ ↑ delay	t_{MED2} (12)				50	
ϕ ↓ to $\overline{RD}$ ↑ delay	t_{RDD2} (13)				50	
ϕ ↑ to $\overline{M1}$ ↑ delay	t_{M1D2} (14)				70	
Data read setup time	t_{DRS} (15)			30		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ $4.5V \le V_{CC} \le 5.5V$, $V_{SS}=0.0V$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Data read hold time	t_{DRH} (16)	See figure 3 V_{CC} = 4.5 V	9,10,11	0		ns
ϕ ↓ to ST ↓ delay	t_{STD1} (17)				70	
ϕ ↓ to ST ↑ delay	t_{STD2} (18)				70	
$\overline{WAIT}$ set-up time to ϕ ↓	t_{WS} (19)			40		
$\overline{WAIT}$ hold time from ϕ ↓	t_{WH} (20)			40		
ϕ ↑ to data float display	t_{WDZ} (21)				70	
ϕ ↑ to $\overline{WR}$ ↓ delay	t_{WRD1} (22)				60	
ϕ ↓ to write data delay time	t_{WDD} (23)				80	
Write data set-up time to $\overline{WR}$ ↓	t_{WDS} (24)			20		
ϕ ↓ to $\overline{WR}$ ↑ delay	t_{WRD2} (25)				60	
$\overline{WR}$ pulse width memory write cycle	t_{WRP} (26a)			130		
$\overline{WR}$ pulse width I/O write cycle	t_{WRP} (26)			255		
Write data hold time from $\overline{WR}$ ↑	t_{WDH} (27)			15		
ϕ ↓ to $\overline{IORQ}$ ↓ delay ($\overline{IOC}$ = 1)	t_{IOD1} (28)				50	
ϕ ↑ to $\overline{IORQ}$ ↓ delay ($\overline{IOC}$ = 0)	t_{IOD1} (28)				60	
ϕ ↓ to $\overline{IORQ}$ ↑ delay	t_{IOD2} (29)				50	

See footnotes at end of table

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ $4.5V \le V_{CC} \le 5.5V$, $V_{SS}=0.0V$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
$\overline{M1}$ ↓ to $\overline{IORQ}$ ↓ delay	t_{IOD3} (30)	See figure 3 V_{CC} = 4.5 V	9,10,11	250		ns
$\overline{INT}$ setup time to φ ↓	t_{INTS} (31)			40		
$\overline{INT}$ hold time from φ ↓	t_{INTH} (32)			40		
$\overline{NMI}$ pulse width	t_{NMIW} (33)			100		
$\overline{BUSREQ}$ setup time to φ ↓	t_{BRS} (34)			40		
$\overline{BUSREQ}$ hold time from φ ↓	t_{BRH} (35)			40		
φ ↑ to $\overline{BUSACK}$ ↓ delay	t_{BAD1} (36)				70	
φ ↓ to $\overline{BUSACK}$ ↑ delay	t_{BAD2} (37)				70	
φ ↑ to bus floating delay time	t_{BZD} (38)				90	
$\overline{MREQ}$ pulse width high	t_{MEWH} (39)			90		
$\overline{MREQ}$ pulse width low	t_{MEWL} (40)			100		
φ ↑ to $\overline{RFSH}$ ↓ delay	t_{RFD1} (41)				80	
φ ↓ to $\overline{RFSH}$ ↑ delay	t_{RFD2} (42)				80	

See footnotes at end of table

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ $4.5V \le V_{CC} \le 5.5V$, $V_{SS}=0.0V$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
ϕ ↑ to $\overline{HALT}$ ↓ delay	t_{HAD1} (43)	See figure 3 V_{CC} = 4.5 V	9,10,11		80	ns
ϕ ↑ to $\overline{HALT}$ ↑ delay	t_{HAD2} (44)				80	
$\overline{DREQi}$ setup time to ϕ ↑	t_{DRQS} (45)			40		
$\overline{DREQi}$ hold time from ϕ ↑	t_{DRQH} (46)			40		
ϕ ↓ to $\overline{TENDi}$ ↓ delay	t_{TED1} (47)				60	
ϕ ↓ to $\overline{TENDi}$ ↑ delay	t_{TED2} (48)				60	
ϕ ↑ to E ↑ delay	t_{ED1} (49)				70	
ϕ ↓ or ↑ to E ↓ delay	t_{ED2} (50)				70	
E pulse width high	P_{WEH} (51)			65		
E pulse width low	P_{WEL} (52)			130		
Enable rise time	t_{Er} (53)				20	
Enable fall time	t_{Ef} (54)				20	
ϕ ↓ to timer output delay	t_{TOD} (55)				200	

See footnotes at end of table

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ $4.5V \le V_{CC} \le 5.5V$, $V_{SS}=0.0V$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
CSI 0 transmit data delay time (internal clock operation)	t_{STDI} (56)	See figure 3 V_{CC} = 4.5 V	9,10,11		200	ns
CSI 0 transmit data delay time (external clock operation)	t_{STDE} (57)				$7.5t_{cyc}+200$	
CSI 0 receive data setup time (internal clock operation)	t_{SRSI} (58)			1		tcyc
CSI 0 receive data hold time (internal clock operation)	t_{SRHI} (59)			1		
CSI 0 receive data setup time (external clock operation)	t_{SRSE} (60)			1		
CSI 0 receive data hold time (external clock operation)	t_{SRHE} (61)			1		
$\overline{\text{RESET}}$ setup time to $\phi\downarrow$	t_{RES} (62)			100		ns
$\overline{\text{RESET}}$ hold time to $\phi\downarrow$	t_{REH} (63)			70		
Oscillator stabilization time	t_{OSC} (64)				20	ms
External clock rise time(EXTAL)	t_{EXr} (65)				25	ns
External clock fall time(EXTAL)	t_{EXf} (66)				25	
$\overline{\text{RESET}}$ rise time	t_{Rr} (67)				50	
$\overline{\text{RESET}}$ fall time	t_{Rf} (68)				50	

See footnotes at end of table

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ $4.5V \le V_{CC} \le 5.5V$, $V_{SS}=0.0V$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Input rise time (except EXTAL and $\overline{RESET}$)	t_{Ir} (69)	See figure 3 V_{CC} = 4.5 V	9,10,11		100	ns
Input fall time (except EXTAL and $\overline{RESET}$	t_{If} (70)				100	

1/ Unless otherwise specified all test conditions are worst case condition.

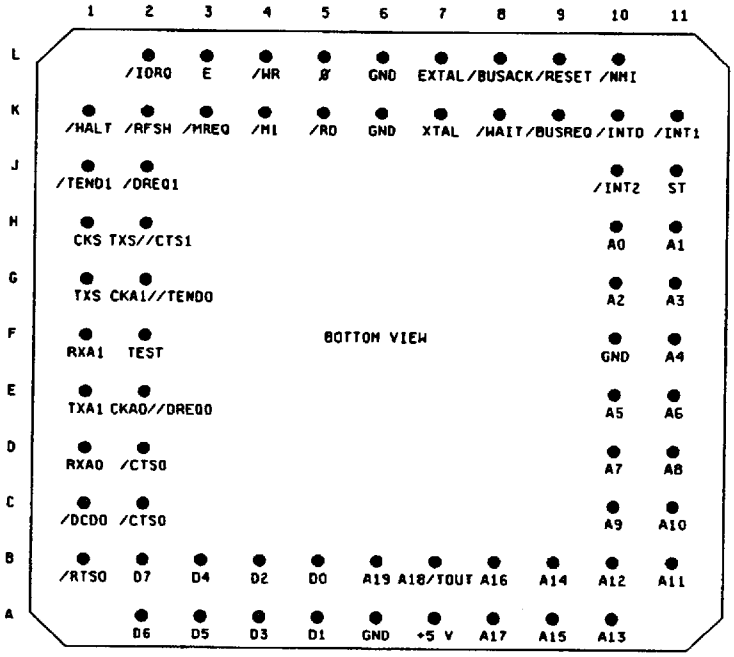


FIGURE 1. Terminal connections.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-94537
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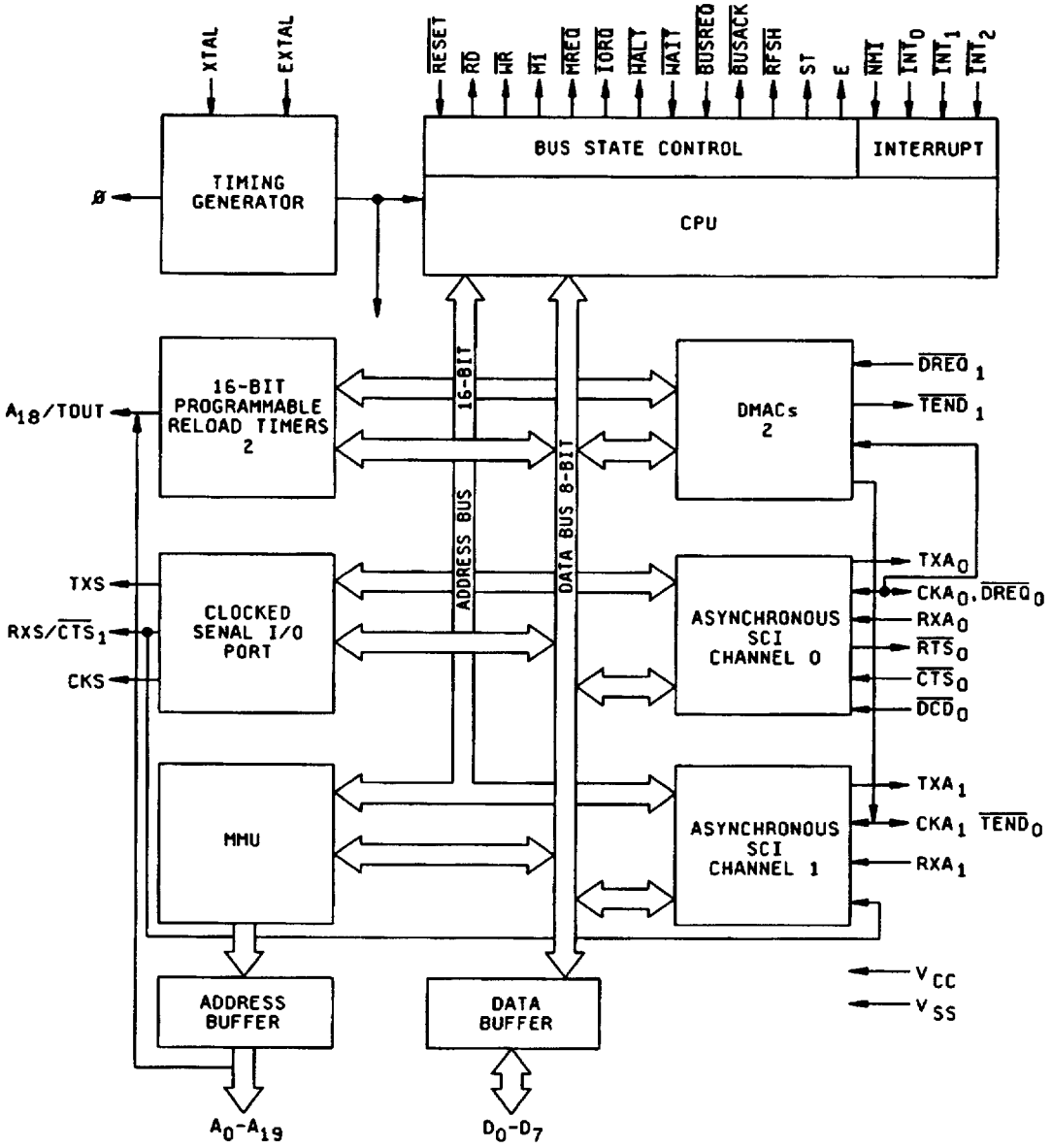
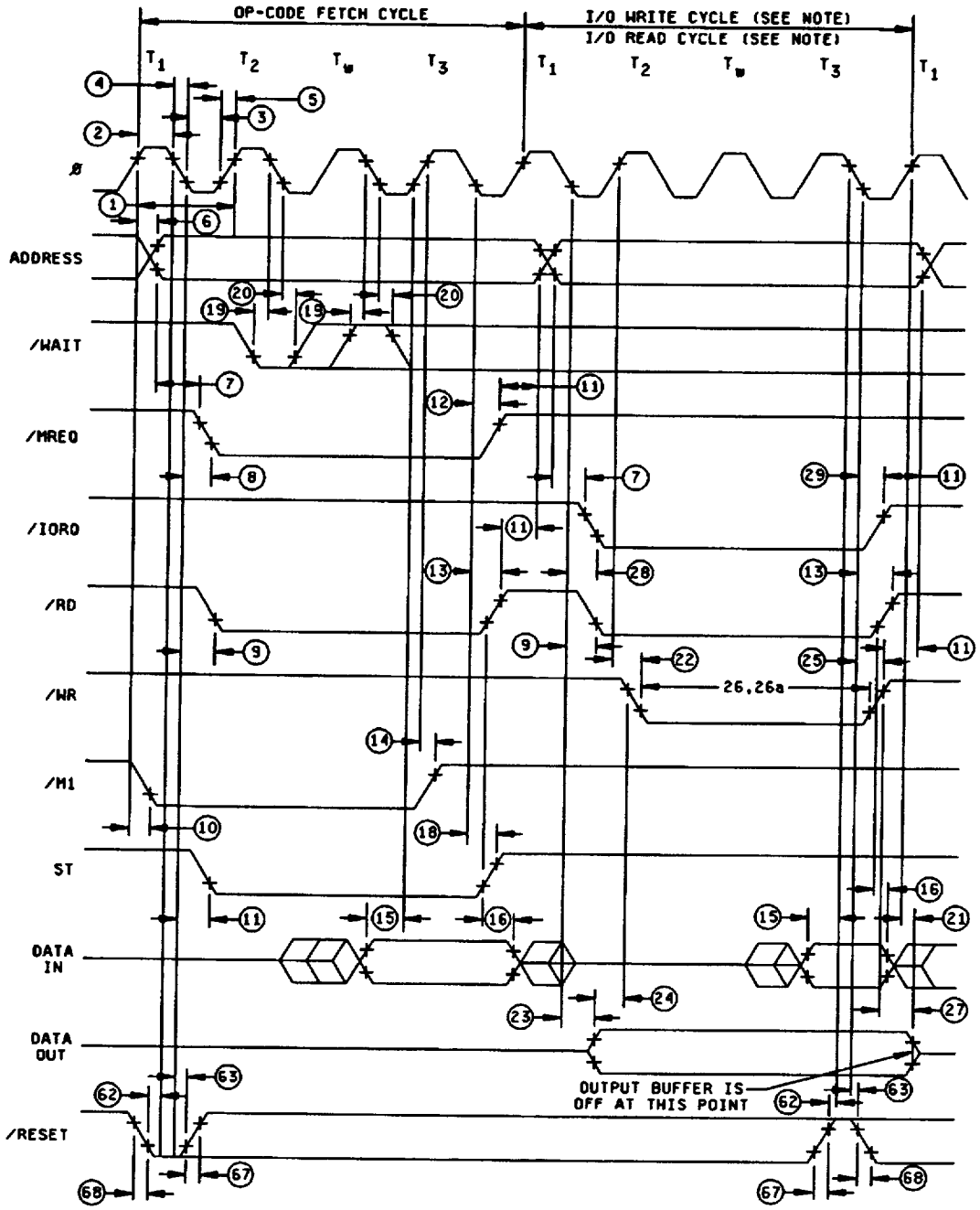


FIGURE 2. Functional block diagram.



Notes:
Memory read/write cycle timing is the same as I/O read/write cycle timing except there are no automatic wait states (T_W), and MREQ is active instead of IORQ.

Figure 3. Switching waveforms and test circuit.

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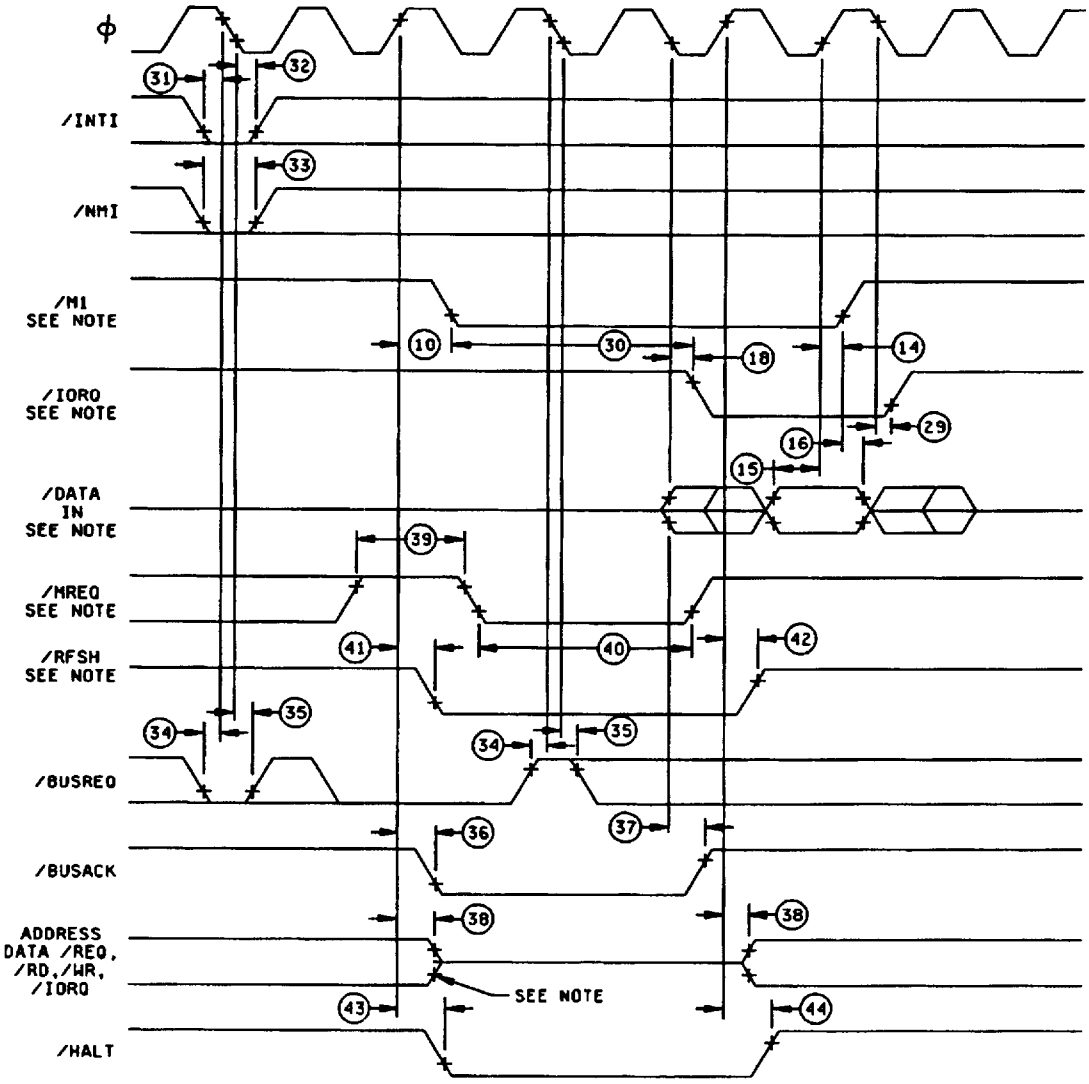
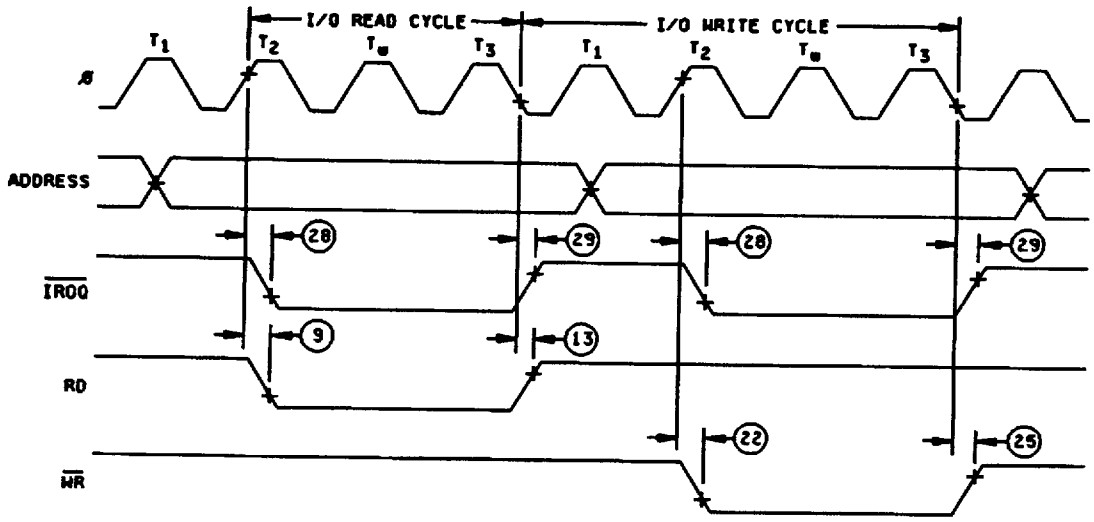


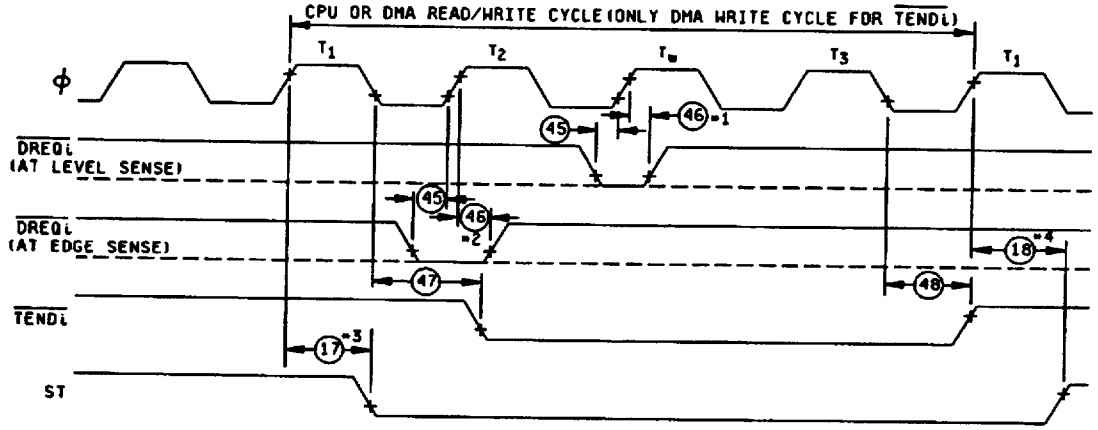
INTO ACKNOWLEDGE CYCLE, REFRESH CYCLE, BUS RELEASE MODE,
HALT MODE, SLEEP MODE, SYSTEM STOP MODE

Notes 1) During INTO acknowledge cycle.
2) During Refresh cycle.
3) Output buffer is off at this point.

Figure 3. Switching waveforms and test circuit - continued.



CPU TIMING ($\overline{IOC}$ = 0)
{I/O READ CYCLE
I/O WRITE CYCLE}



Notes: 1) t_{DRQS} and t_{DRQH} are specified for the rising edge of clock followed by T_3.
2) t_{DRQS} and t_{DRQH} are specified for the rising edge of clock.
3) DMA cycle starts.
4) CPU cycle starts.

Figure 3. Switching waveforms and test circuit - continued.

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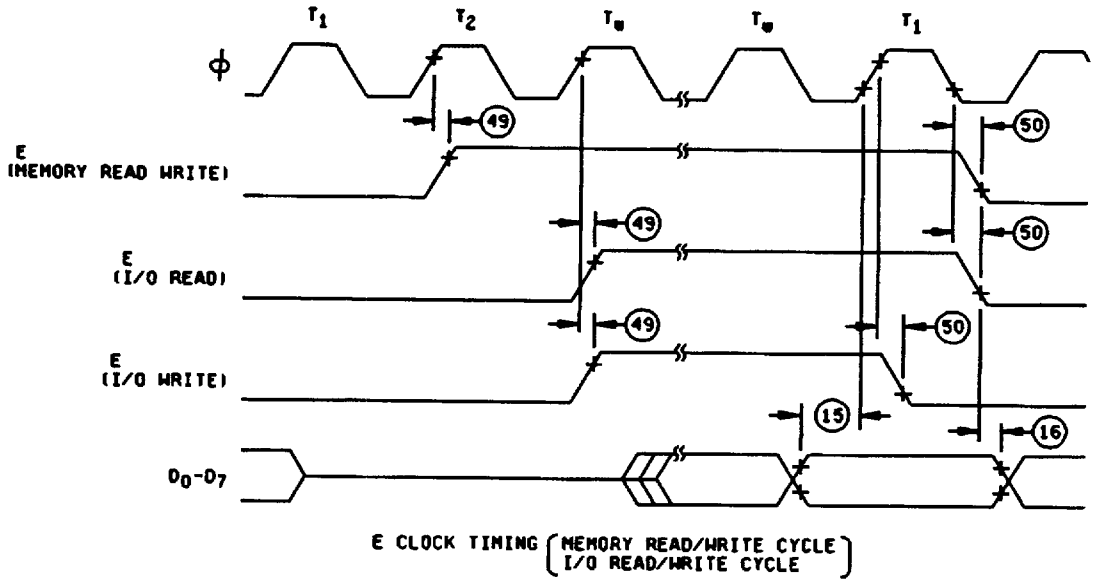
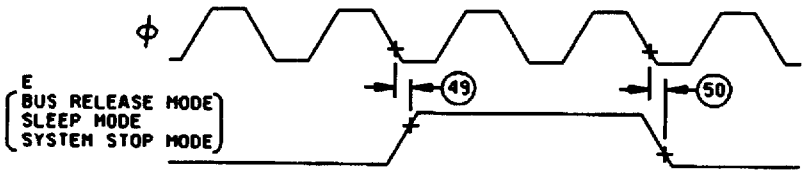
		REVISION LEVEL	SHEET 16

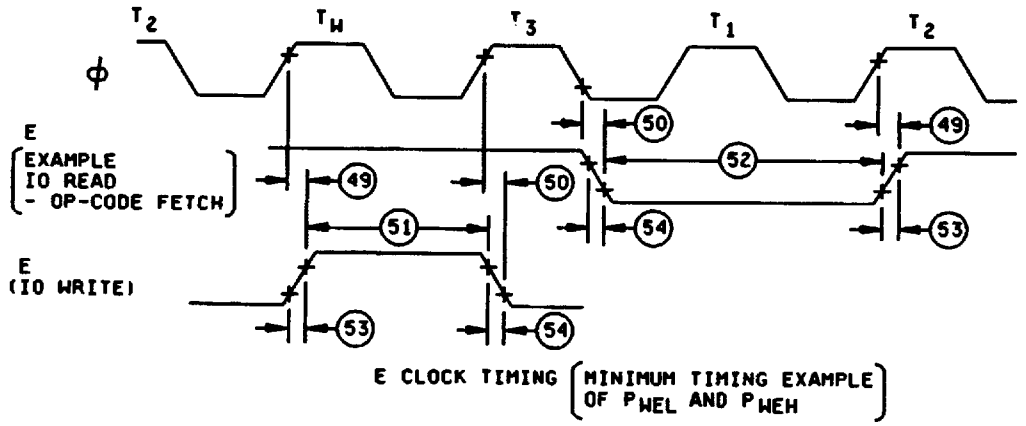


E CLOCK TIMING { MEMORY READ/WRITE CYCLE, I/O READ/WRITE CYCLE }

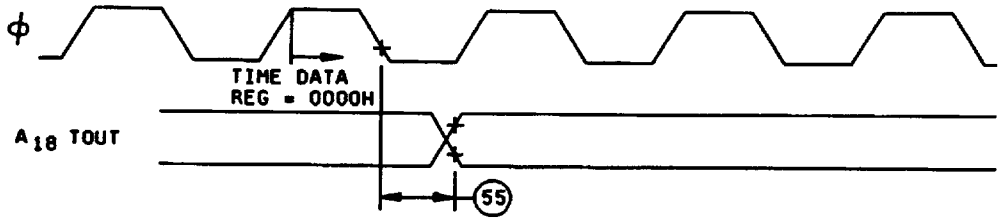


E CLOCK TIMING { BUS RELEASE MODE, SLEEP MODE, SYSTEM STOP MODE }

Figure 3. Switching waveforms and test circuit - continued.

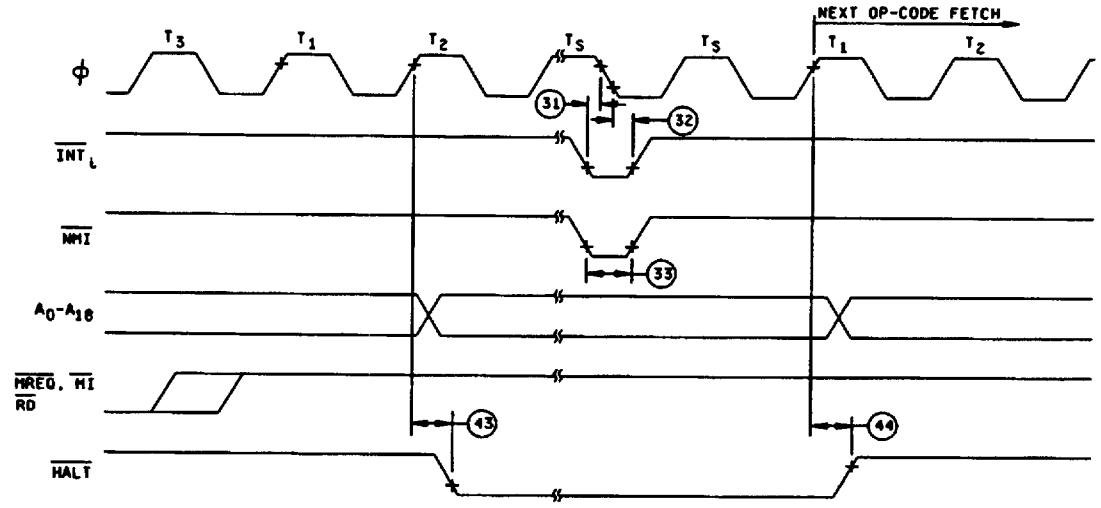


E CLOCK TIMING (MINIMUM TIMING EXAMPLE OF P_{WEL} AND P_{WEH})

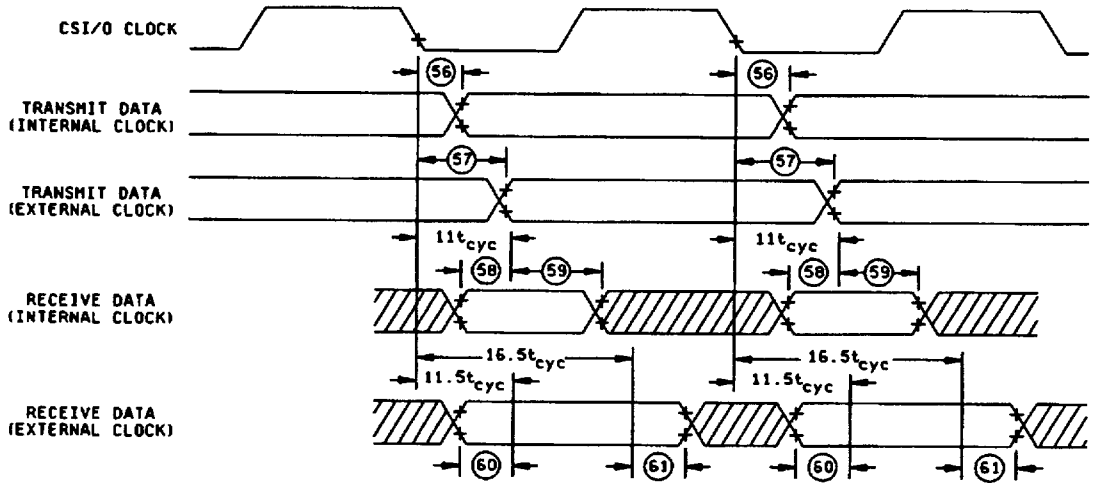


TIMER OUTPUT TIMING

Figure 3. Switching waveforms and test circuit - continued.

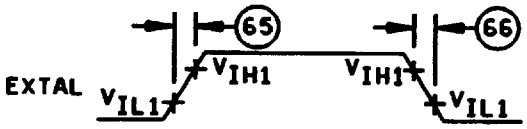


SLP EXECUTION CYCLE

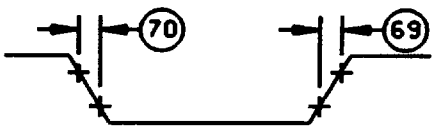


CSI/O RECEIVE/TRANSMIT TIMING

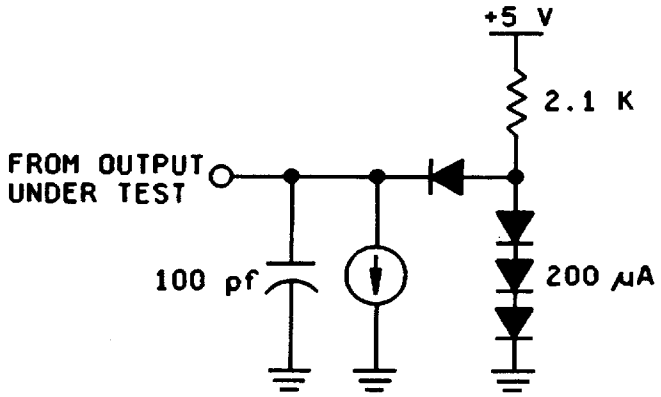
Figure 3. Switching waveforms and test circuit - continued.



EXTERNAL CLOCK RISE TIME
AND FALL TIME



INPUT RISE TIME AND FALL TIME
(EXCEPT EXTAL, RESET)



Note: The DC charaacteristics and capacitance sections above apply to the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows in to the referenced pin. All AC parameters assume a load capacitance of 100 pF. Add 10 ns delay for each 50 pF increase in load up to a maximum of 200 pF for the data bus and 100 pF for the address and control lines. AC timing measurements are referenced to 1.5 volts (except for CLOCK, which is referenced to the 10% and 90% points).

Figure 3. Switching waveforms and test circuit - continued.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_p) measurements shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of five devices with zero rejects shall be required.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,7,9	1,7,9	1,7,9
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9, 10, 11	1/ 1, 2, 3, 7, 8, 9, 10, 11	2/ 1, 2, 3, 7 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)			

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5765, or telephone (513) 296-8526.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535, MIL-STD-1331 and as follows:

A_0 - A_{19}	**Address Bus** (Output, active high, three-state). A_0 - A_{19} form a 20-bit address bus. The address bus provides the address for memory data bus exchanges, up to 1 Mbyte, and I/O data bus exchanges, up to 64 K. The address bus enters a high impedance state during reset and external bus acknowledge cycles. Address line A_{18} is multiplexed with the output of PRT channel 1 (TOUT, selected as address output on reset).
$\overline{BUSACK}$	**Bus Acknowledge** (Output, active low). Indicates the requesting device, the MPU adress and data bus, and some control signals, have entered their high impedance state.
$\overline{BUSREQ}$	**Bus Request** (Input, active low). This input is used by external devices (such as DMA controllers) to request access to the system bus. This request has a higher priority than NMI and is always recognized at the end of the current machine cycle. This signal will stop the CPU from executing further instructions and places the address and data buses, and other control signals, into the high impedance state.
CKA_0, CKA_1	**Asynchronous Clock 0 and 1** (Bidirectional, active high). These pins are the transmit and receive clocks for the synchronous channels. CKA_0 is multiplexed with $\overline{DREQ_0}$ and CKA_1 is multiplexed with $\overline{TEND_0}$.
CKS	**Serial Clock** (Bidirectional, active high). This line is clock for the CSIO channel.
CLOCK	**System Clock** (Output, active high). The output is used as a reference clock for the MPU and the external system. The frequency of this output is equal to one-half that of the crystal or input clock frequency.
CTS_0 - CTS_1	**Clear to send 0 and 1** (Inputs, active low). These lines are modem control signals for the ASCI channels. CTS1 is multiplexed with RXS.
D_0 - D_7	**Data bus** (Bidirectional, active high, three-state). D_0 - D_7 constitute an 8-bit bidirectional data bus, used for the transfer of information to and from I/O and memory devices. The data bus enters the high impedance state during reset and external bus acknowledge cycles.
$\overline{DCD_0}$	**Data carrier detect 0** (Input, active low). This is a programmable modem control signal for ASCI channel 0.
$\overline{DREQ_0}$, $\overline{DREQ_1}$	**DMA request 0 and 1** (Input, active low). $\overline{DREQ}$ is used to request a DMA transfer from one of the on-chip DMA channels. The DMA channels monitor these inputs to determine when an external device is ready for a read or write operation. These inputs can be programmed to be either level or edge sensed. $DREQ_0$ is multiplexed with CKA_0.
E	**Enable clock** (Output, active high). Synchronous machine cycle clock output during bus transactions.
EXTAL	**External clock/crystal** (Input, active high). Crystal oscillator connection. An external clock can be input to the device on this pin when a crystal is not used. This input is Schmitt triggered.
$\overline{HALT}$	**Halt/sleep status** (Output, active low). This output is asserted after the CPU has executed either the HALT or SLP instruction, and is waiting for either non-maskable or maskable interrupt before operation can resume. It is also used with the M1 and ST signals to decode status of the CPU machine cycle.
$\overline{INT_0}$	**Maskable interrupt request 0** (Input, active low). This signal is generated by external I/O devices. The CPU will honor this request at the end of the current instruction cycle as long as the NMI and BUSREQ signals are inactive. The CPU acknowledges this interrupt request with an interrupt acknowledge cycle. During this cycle, both the M1 and IORQ signals will become active.

6.5 Abbreviations, symbols and definitions - Continued

$\overline{INT_1}$, $\overline{INT_2}$	**Maskable interrupt requests 1 and 2** (Inputs, active low). This signal is generated by external I/O devices. The CPU will honor these requests at the end of the current instruction cycle as long as the NMI, BUSREQ, and $\overline{INT_0}$ signals are inactive. The CPU will acknowledge these interrupt requests with an interrupt acknowledge cycle. Unlike the acknowledgement for $\overline{INT_0}$ during this cycle neither the M1 or IORQ signals will become active.
$\overline{IORQ}$	**I/O request** (Output, active low, three-state). $\overline{IORQ}$ indicates that the address bus contains a valid I/O address for an I/O read or I/O writ operation. IORQ is also generated, along with M1, during the acknowledgement of the $\overline{INT_0}$ input signal to indicate that an interrupt response vector can be placed onto the data bus.
$\overline{M1}$	**Machine cycle 1** (Output, active low). Together with $\overline{MREQ}$, $\overline{M1}$ indicates that the current cycle is the opcode fetch cycle of an instruction execution. Together with IORQ, M1 indicates that the current cycle is for an interrupt acknowledge. It is also used with the HALT and ST signal to decode status of the CPU machine cycle.
$\overline{MREQ}$	**Memory request** (Output, active low, three-state). MREQ indicates that the address bus holds a valid address for a memory read or memory write operation.
$\overline{NMI}$	**Non-maskable interrupt** (Input, negative edge triggered). $\overline{NMI}$ has a higher priority than $\overline{INT}$ and is always recognized at the end of an instruction, regardless of the state of the interrupt enable flip-flops. This signal forces CPU execution to continue at location 0066H.
$\overline{RD}$	**Read** (Output, active low, three-state). $\overline{RD}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O or memory device should use this signal to gate data onto the CPU data bus.
$\overline{RFSH}$	**Refresh** (Output, active low). Together with $\overline{MREQ}$, $\overline{RFSH}$ indicates that the current CPU machine cycle and the contents of the address bus should be used for refresh of dynamic memories. The low order 8 bits of the address bus (A_7 - A_0) contain the refresh address.
$\overline{RTS_0}$	**Request to send 0** (Output, active low). This is a programmable modem control signal for ASCI channel 0.
RXA_0, RXA_1	**Receive data 0 and 1** (Inputs, active high). These signals are the receive data to the ASCI channels.
RXS	**Clocked serial receive data** (Input, active high). This line is the receiver data for the CSIO channel. RXS is multiplexed with the CTS1 signal for ASCI channel 1.

6.5 Abbreviations, symbols and definitions - Continued

ST — **Status** (Output, active high). This signal is used with the $\overline{M1}$ and $\overline{HALT}$ output to decode the status of the CPU machine cycle.

(The output from M1 is affected by the status of the M1E bit in OMCR register. The following shows the status while M1E = 1.)

$\overline{ST}$	$\overline{HALT}$	$\overline{M1}$	Operation
0	1	0	CPU operation (1st op-code fetch)
1	1	0	CPU operation (2nd op-code and 3rd op-code fetch)
1	1	1	CPU operation (MC except for op-code fetch)
0	X	1	DMA operation
0	0	0	HALT mode
1	0	1	SLEEP mode (including SYSTEM STOP mode)

X = Don't care
MC = Machine cycle

$\overline{TEND_0}$, $\overline{TEND_1}$ — **Transfer end 0 and 1** (Outputs, active low). This output is asserted active during the last write cycle of a DMA operation. It is used to indicate the end of the block transfer. $TEND_0$ in multiplexed with CKA_1.

TOUT — **Timer out** (Output, active high). TOUT is the pulse output from PRT channel 1. This line is multiplexed with A_{18} of the address bus.

TEST — **Test** (output). This pin is for test and should be left open.

TXA_0, TXA_1 — **Transmit data 0 and 1** (Outputs, active high). These signals are the transmitted data from the ASCI channels. Transmitted data changes are with respect to the falling edge of the transmit clock.

TXS — **Clocked serial transmit data** (Output, active high). This line is the transmitted data from the CSIO channel.

$\overline{WAIT}$ — **Wait** (Input, active low). $\overline{WAIT}$ indicates to the MPU that the addressed memory or I/O devices are not ready for a data transfer. This input is used to induce additional clock cycles into the current machine cycle. The WAIT input is sampled on the falling edge of T_2 (and subsequent wait states are inserted until the WAIT input is sampled high, at which time execution will continue.

$\overline{WR}$ — **Write** (Output, active low, three-state). $\overline{WR}$ indicates that the CPU data bus holds valid data to be stored at the addressed I/O or memory location.

XTAL — **Crystal** (Input, active high). Crystal oscillator connection. This pin should be left open if an external clock is used instead of a crystal. The oscillator input is not a TTL level (reference DC characteristics in Table I).

Multiplexed pins

$A_{18}/\overline{TOUT}$ — During RESET, this pin is initialized as A_{18} pin. If either TOC1 or TOC0 bit of the timer control register (TCR) is set to 1, TOUT function is selected. If TOC1 and TOC0 bits are cleared to 0, A_{18} function is selected.

$CKA_0/\overline{DREQ_0}$ — During RESET, this pin is initialized as CKA_0 pin. If either DM1 or SM1 in DMA mode register (DMODE) is set to 1, $DREQ_0$ function is always selected.

6.5 Abbreviations, symbols, and definitions - continued.

$CKA_1/\overline{TEND}_0$	During RESET, this pin is initialized as CKA_1 pin. If CKA1D bit in ASCI control register ch 1 (CNTLA1) is set to 1, $TEND_0$ function is selected. If CKA1D bit is set to 0, CKA_1 function is selected.
$RXS/\overline{CTS}_1$	During RESET, this pin is initialized as RXS pin. If CTS1E bit in ASCI status register ch1 (STAT1) is set to 1, $\overline{CTS}_1$ function is selected. If CTS1E bit is set to 0, RXS function is selected

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.