REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																								
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REV STATUS OF SHEETS	REV																							
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17						

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE: 11 MAY 1988

REVISION LEVEL:

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, LINEAR, 9 BIT A/D CONVERTER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-88532

SHEET 1 OF 17

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E740

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-88532	01	X	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	TDC1049	9-Bit A/D converter

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
X	D-13(64-lead, 3.240" X .920" X .225"), dual-in-line package, config. 3 only
Y	See figure 1 (64-lead, 3.240" X .810" X .225"), dual-in-line package
Z	C-7 (68-terminal, .962" X 962" X .120"), square chip carrier package

1.3 Absolute maximum ratings.

V_{EED} to D_{GND}	+0.5 V dc to -7.0 V dc
V_{EEA} to A_{GND}	+0.5 V dc to -7.0 V dc
V_{EEA} to V_{EED}	+0.5 V dc to -0.5 V dc
A_{GND} to D_{GND}	+1.0 V dc to -1.0 V dc
V_{IN}, V_{RT}, or V_{RB} to A_{GND}	+0.5 V dc to V_{EE}
$\overline{CONV}$ or CONV to D_{GND}	+0.5 V dc to V_{EE}
V_{RT} to V_{RB}	+2.5 V dc to -2.5 V dc
Output short circuit duration	Indefinite
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Power dissipation, worst case (P_D)	6.07 W
Thermal resistance, junction-to-case (θ_{JC}):	
Cases X and Z	See MIL-M-38510, appendix C
Case Y	12°C/W
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Digital supply voltage to D_{GND} (V_{EED})	-4.9 V dc to -5.5 V dc
Analog supply voltage to A_{GND} (V_{EEA})	-4.9 V dc to -5.5 V dc
Analog ground voltage to A_{GND} (V_{AGND})	-0.1 V dc to +0.1 V dc
Supply voltage differential (V_{EEA} - V_{EED})	-0.1 V dc to +0.1 V dc
CONV pulse width, low (t_{PWL})	12 ns minimum
CONV pulse width, high (t_{PWH})	15 ns minimum
CONV input voltage, common mode (V_{ICM})	-0.5 V dc to -2.5 V dc
CONV input voltage, differential (V_{IDF})	+0.3 V dc to +1.2 V dc
Most positive reference input (V_{RT}) 1/	-0.1 V dc to +0.1 V dc
Most negative reference input (V_{RB}) 1/	-1.9 V dc to -2.1 V dc
Voltage reference differential (V_{RT} - V_{RB})	1.8 V dc to 2.1 V dc
Input voltage (V_{IN})	V_{RB} to V_{RT}
Operating case temperature range (T_C)	-55°C to + 125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

1/ V_{RT} must be more positive than V_{RB}, and V_{RT} - V_{RB} must be within the specified range.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.2 Block diagram. The block diagram shall be as specified on figure 3.

3.2.3 Truth table. The truth table shall be as specified on figure 4.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Supply current	I_{EE}	$V_{EED} = V_{EEA} = -5.5$ V	1, 2, 3		-1090	mA
Reference current	I_{REF}	$V_{RT} = 0.0$ V, $V_{RB} = -2.0$ V V_{EEA}, $V_{EED} = -5.5$ V	1, 2, 3		36	mA
Total reference resistance 2/	R_{REF}	$V_{RT} = 0.0$ V, $V_{RB} = -2.0$ V	1, 2, 3	56	200	Ω
Input equivalent resistance 2/	R_{IN}	$V_{RT} = 0.0$ V, $V_{RB} = -2.0$ V	1, 2, 3	16		kΩ
Input capacitance 2/	C_{IN}	$V_{RT} = 0.0$ V, $V_{RB} = -2.0$ V	4, 5, 6		160	pF
Input constant bias current	I_{CB}	$V_{IN} = 0.0$ V, $V_{EEA} = V_{EED} = 5.5$ V	1, 2, 3		750	µA
Digital input current (CONV, $\overline{CONV}$)	I_I	$V_I = -0.7$ V, $V_{EEA} = V_{EED} = -5.5$ V	1, 2, 3		180	µA
Output low voltage	V_{OL}	V_{EEA}, $V_{EED} = -4.9$ V 3/	1, 2, 3		-1.5	V
Output high voltage	V_{OH}	V_{EEA}, $V_{EED} = -5.5$ V 3/	1, 2, 3	-1.1		V
Digital input capacitance 2/	C_I	$T_A = 25°C$, f = 1.0 MHz	4		20	pF
Maximum conversion rate 2/	F_S	V_{EEA}, $V_{EED} = -4.9$ V	4, 5, 6	30		MSPS 4/
Functional tests		V_{EEA}, $V_{EED} = -5.2$ V, $F_S = 1.0$ MSPS (check output coding), see 4.3.1b	7, 8			
Sampling time offset 2/	t_{STO}	See figure 5	9,10,11	-2.0	6.0	ns
Digital output delay	t_D	V_{EEA}, $V_{EED} = -4.9$ V See figure 4 3/	9,10,11		31	ns
Digital output hold time 2/	t_{HO}	See figure 5	9,10,11	3.0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
Linearity error integral	E_{LI}	V_{RT} = 0.0 V, V_{RB} = -2.0 V F_S = 100 kHz		4, 5, 6		0.2	%
Linearity error, differential	E_{LD}	V_{RT} = 0.0 V, V_{RB} = -2.0 V F_S = 100 kHz		4, 5, 6		0.1	%
Nominal code size	Q	V_{RT} = 0.0 V, VRB = -2.0 V F_S = 100 kHz		4, 5, 6	15	185	%
Offset error, top 2/	E_{OTS}	$V_{IN} = V_{RT}$, R_{TS} connected		1, 2, 3		±4.0	mV
	E_{OT}	$V_{IN} = V_{RT}$		1, 2, 3	0	+30	
Offset error, bottom 2/	E_{OBS}	$V_{IN} = V_{RB}$, R_{BS} connected		1, 2, 3		±4.0	mV
	E_{OB}	$V_{IN} = V_{RB}$		1, 2, 3	0	-30	
Temperature coefficient of offset error 2/	$\frac{\Delta E_O}{\Delta T}$	$V_{IN} = V_{RB}$		1, 2, 3		20	µV/°C
Bandwidth, full power input 2/	BW			4, 5, 6	15		MHz
Signal-to-noise ratio (30 MSPS conversion rate, 10 MHz bandwidth) 2/	SNR	Peak signal/ RMS noise	1.25 MHz input	4, 5, 6	57		dB
			5.0 MHz input	4, 5, 6	53		
		RMS signal/ RMS noise	1.25 MHz input	4, 5, 6	48		
			5.0 MHz input	4, 5, 6	44		
Differential phase error 2/	DP	F_S = 4 X NTSC subcarrier		4, 5, 6		0.5	degrees
Differential gain error 2/	DG	F_S = 4 X NTSC subcarrier		4, 5, 6		1.5	%

1/ Unless otherwise specified, characteristics apply over the recommended operating conditions specified in 1.4 herein.
2/ Guaranteed if not tested.
3/ Test load = 500 ohms to -2.0 V, and 20 pF to ground.
4/ Mega samples per second.

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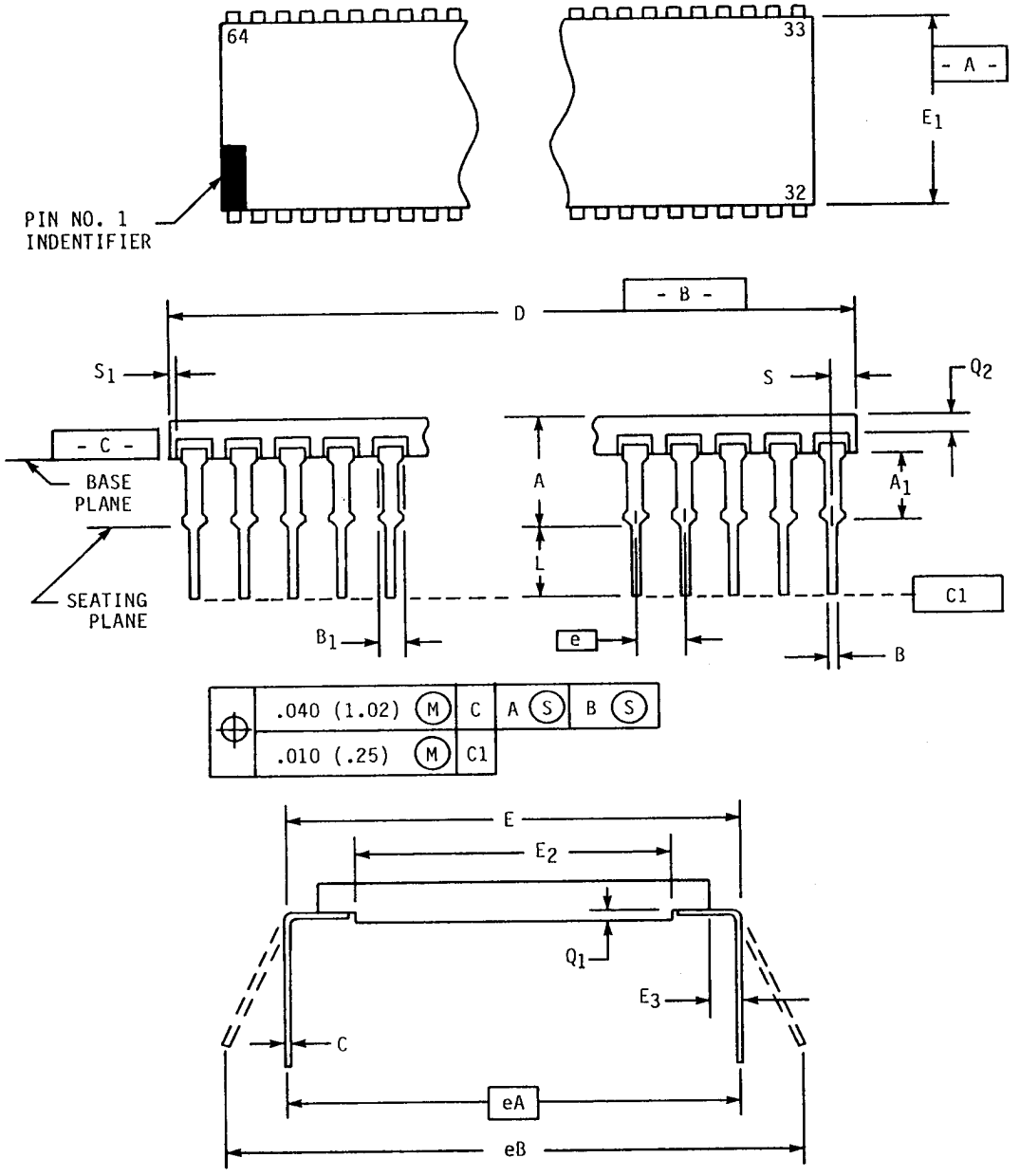

FIGURE 1. Case outline Y.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-88532
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SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.110	.225	2.79	5.72	3
A1	.050	.105	1.27	2.67	3
B	.014	.023	0.35	0.58	
B1	.030	.070	0.78	1.78	
C	.007	.015	0.18	0.38	
D	3.170	3.240	80.52	82.30	4
E	.880	.940	22.35	23.88	5
E1	.790	.810	20.07	20.57	4
E2	.640	.680	16.26	17.27	

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
E3	.025	--	.053	--	
e	.100 BSC		2.54 BSC		
eA	.900 BSC		22.86 BSC		5
eB	--	1.050	--	26.67	6
L	.125	.200	3.17	5.08	3
Q1	.026	.035	0.66	0.89	
Q2	.005	--	0.13	--	9
S	.030	.100	0.76	2.54	
S1	.005	.060	0.13	1.52	9

NOTES:

1. In case of conflict between the English and metric dimensions, the English dimensions control.
2. Dimensioning and tolerance per ANSI-Y14.5M-1982.
3. Dimensions A, A1, and L are measured with the package seating in JEDEC Seating Plane Gauge GS-3.
4. D and E1 dimensions include allowance for package irregularities and lid misalignment.
5. E and eA measured with the lead constrained to be perpendicular to plane C.
6. eB measured at the lead tips with the leads unconstrained.
7. Pointed or rounded lead tips are preferred to ease insertion.
8. To facilitate automatic insertion, any raised irregularity on the top surface (step, mass, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.
9. Metallization of closest approach (pad or lead) to package edge.

FIGURE 1. Case outline - continued.

Device type 01

CASE X

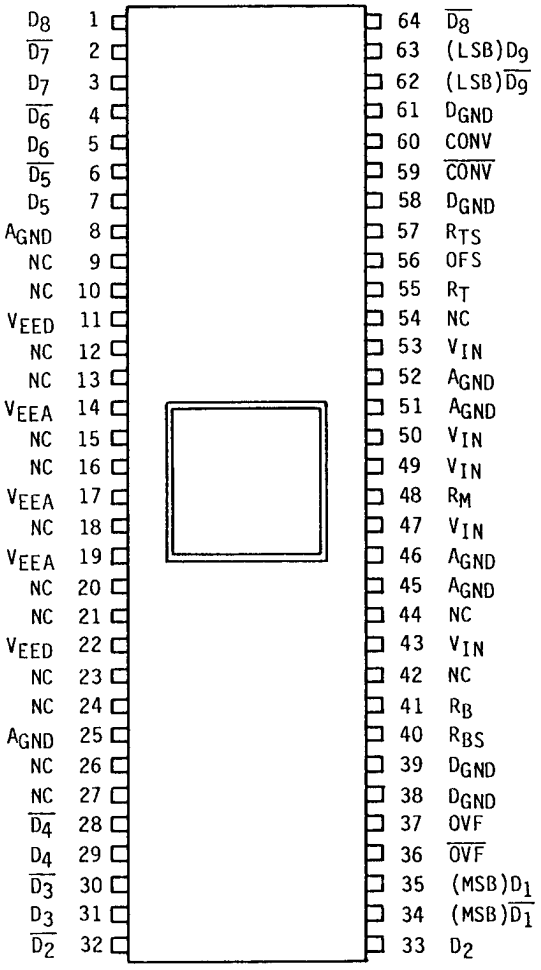

FIGURE 2. Terminal connections (top view).

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Device type 01

CASE Y

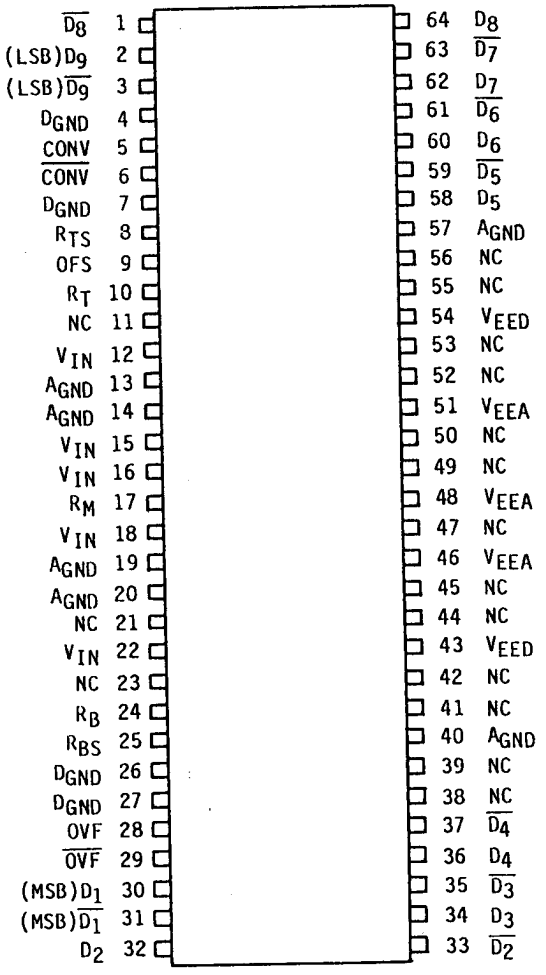

FIGURE 2. Terminal connections (top view) - continued.

Device type 01

CASE Z

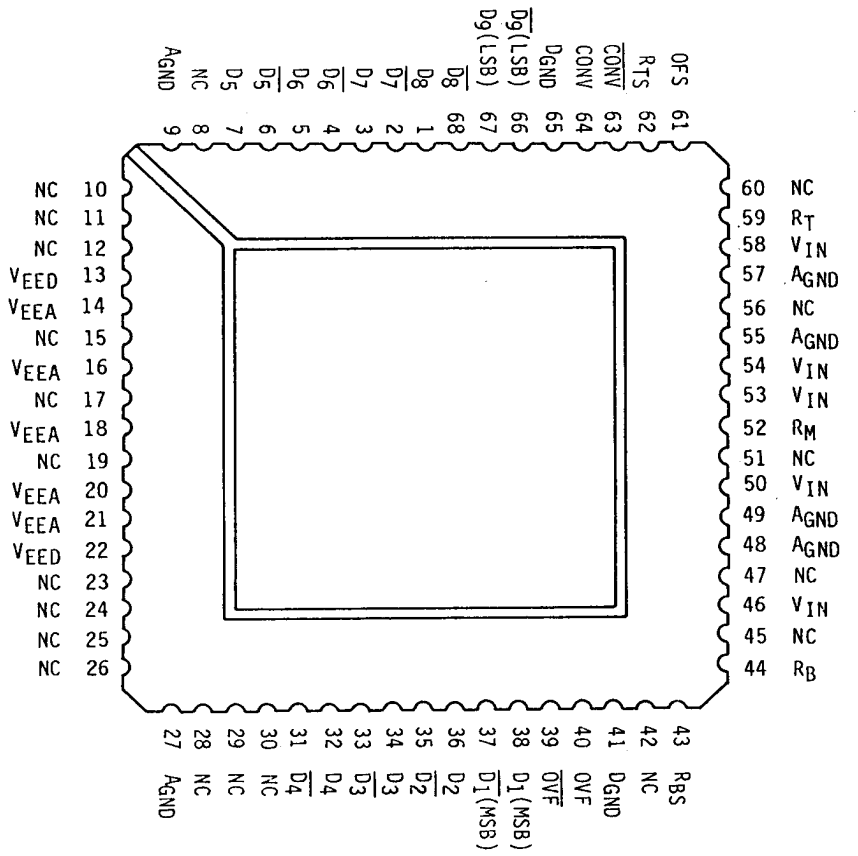

FIGURE 2. Terminal connections (top view) - continued.

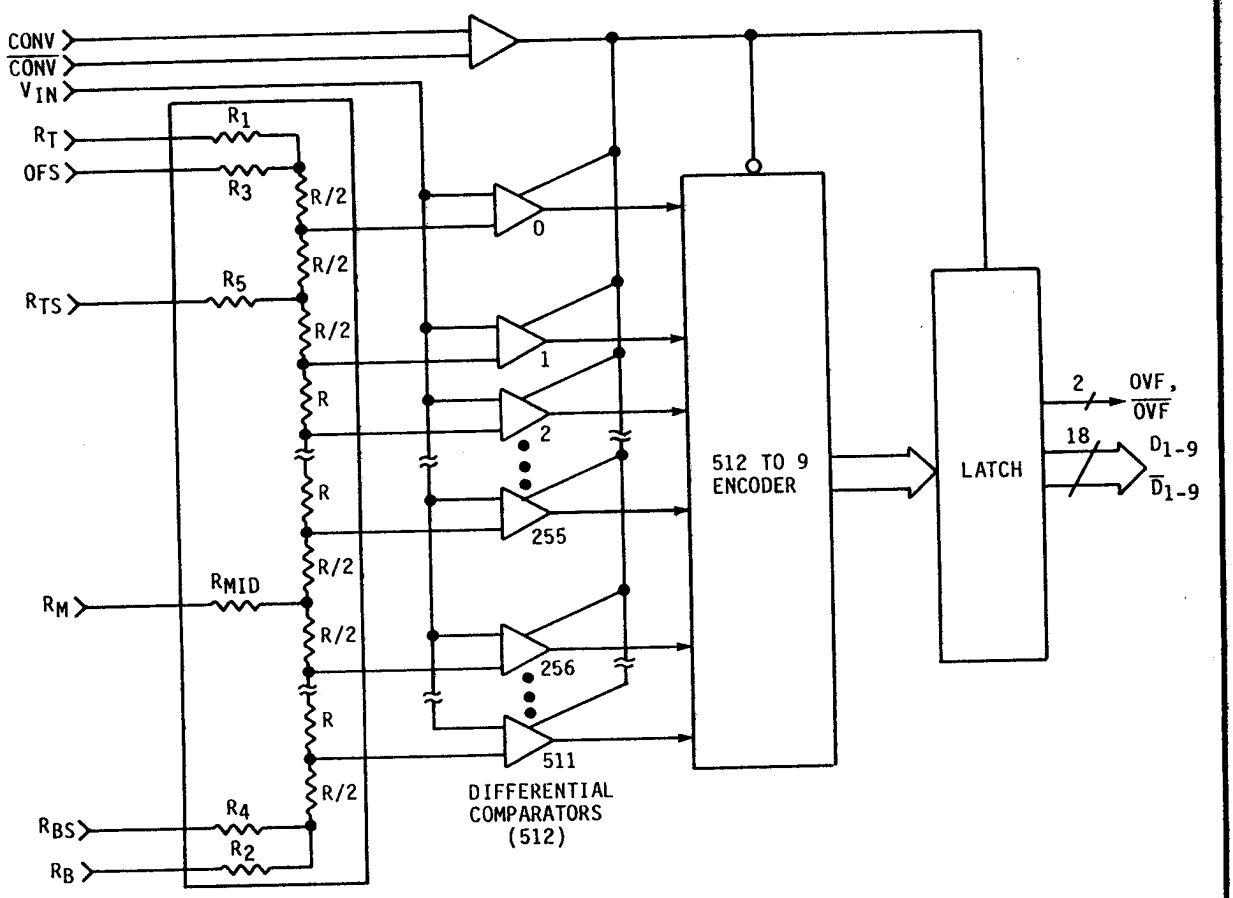

FIGURE 3. Block diagram.

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V_{IN}	OVF	D_1(MSB) - D_9(LSB)
+0.0039V	1	000000000
0.0000V	0	000000000
-0.0039V	0	000000001
.	.	.
.	.	.
.	.	.
-0.9980V	0	011111111
-1.0020V	0	100000000
-1.0059V	0	100000001
.	.	.
.	.	.
.	.	.
-1.9961V	0	111111110
-2.0000V	0	111111111

NOTE:

1. Voltages are code midpoints.

FIGURE 4. Truth table.

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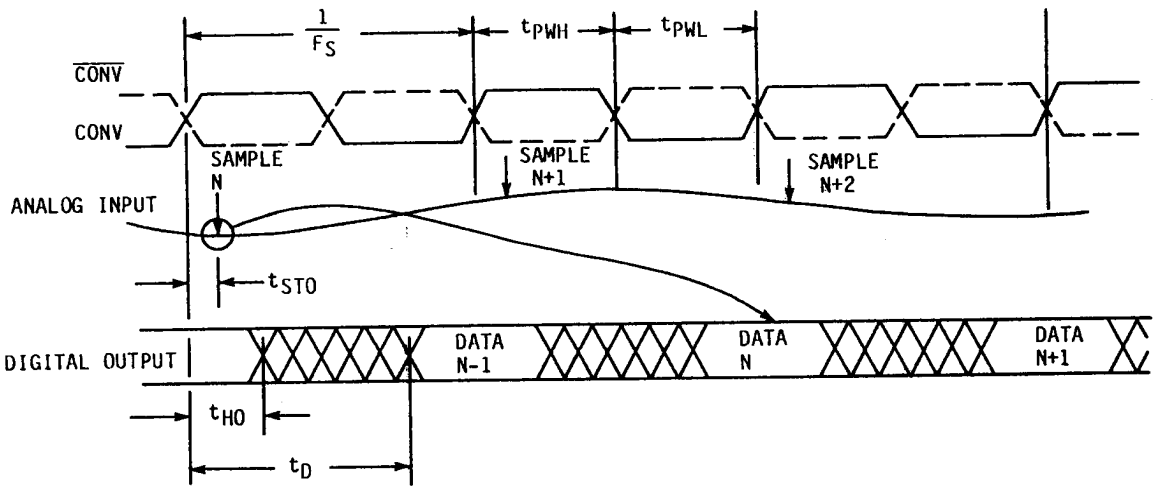

FIGURE 5. Timing diagram.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7 and 8 tests sufficient to verify the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1, 4, 7, 9
Final electrical test parameters (method 5004)	1*,2,3,4,5,6 7*,8,9,10,11
Group A test requirements (method 5005)	1,2,3,4,5,6, 7,8,9,10,11
Groups C and D end-point electrical parameters (method 5005)	1,4,7,9

* PDA applies to subgroups 1 and 7.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8853201XX	59621	TDC1049J0V
5962-8853201YX	59621	TDC1049J3V
5962-8853201ZX	59621	TDC1049C1V

1/ Caution. Do not use this number for item acquisition. Items acquired by this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
59621	TRW/LSI Products Division 4243 Campus Point Court San Diego, CA 92126

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