PM7346

S/UNI™ QJET

S/UNI-QJET

SATURN QUAD USER NETWORK INTERFACE FOR J2/E3/T3

DATASHEET

PROPRIETARY AND CONFIDENTIAL

ISSUE 6: MAY 1999

REVISION HISTORY

Issue No.	Issue Date	Details of Change
6	May 14, 1999	• The S/UNI-QJET requires a software initialization sequence in order to guarantee proper device operation and long term reliability. Please refer to Section 12.1 of this document for the details on how to program this sequence. • Updated the RFCLK and TFCLK pin descriptions to reflect that these pins are not 5V tolerant. Both pins are 3.3V only input pins. • Documentation clarifications.

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1 FEATURES

- Single chip quad ATM User Network Interface operating at 44.736 Mbit/s, 34.368 Mbit/s, and 6.312 Mbit/s conforming to ATMF-95-1207R1, ATMF-94-0406R5, and AF-PHY-0029.000. Each line can be individually configured for the desired rate.
- Implements ATM Direct Cell Mapping into DS1, DS3, E1, E3, and J2 transmission systems according to ITU-T Recommendation G.804.
- Provides a UTOPIA Level 2 compatible ATM-PHY Interface.
- Implements the Physical Layer Convergence Protocol (PLCP) for DS1 and DS3 transmission systems according to the ATM Forum User Network Interface Specification and ANSI TA-TSY-000773, TA-TSY-000772, and E1 and E3 transmission systems according to the ETSI 300-269 and ETSI 300-270.
- Support is provided for SMDS and ATM mappings into various rate transmission systems as follows:

Table 1 - Supported Operating Formats

Rate	Format	Framer Only	SMDS PLCP Mapping	ATM Direct Mapping
T3 (44.736 Mbit/s)	C-bit Parity	YES	YES	YES
	M23	YES	YES	YES
E3 (34.368 Mbit/s)	G.751	YES	YES	YES
	G.832	YES	n/a	YES
J2 (6.312 Mbit/s)	G.704 & NTT	YES	n/a	YES
E1 (2.048 Mbit/s)	CRC-4	external	YES	YES
	PCM30	external	YES	YES
T1 (1.544 Mbit/s)	ESF	external	YES	YES
	SF	external	YES	YES
Arbitrary Cell Rate (up to 52 Mbit/s)		bypass	n/a	YES

- Implements the ATM physical layer for Broadband ISDN according to ITU-T Recommendation I.432.
- Provides on-chip DS3, E3 (G.751 and G.832), and J2 framers.
- Can be configured to be used solely as a DS3, E3, or J2 Framer.
- When configured to operate as a DS3, E3, or J2 Framer, gapped transmit and receive clocks can be optionally generated for interface to devices which only need access to payload data bits.
- Provides support for an arbitrary rate external transmission system interface up to a maximum rate of 52 Mbit/s which enables the S/UNI-QJET to be used as a quad ATM cell delineator.
- Uses the PMC-Sierra PM4341 T1XC, PM4344 TQUAD, PM6341 E1XC, and PM6344 EQUAD T1 and E1 framer/line interface chips for DS1 and E1 applications.
- Provides programmable pseudo-random test pattern generation, detection, and analysis features.
- Provides integral transmit and receive HDLC controllers with 128-byte FIFO depths.
- Provides performance monitoring counters suitable for accumulation periods of up to 1 second.
- Provides an 8-bit microprocessor interface for configuration, control and status monitoring.
- Provides a standard 5 signal P1149.1 JTAG test port for boundary scan board test purposes.
- Low power 3.3V CMOS technology with 5V tolerant inputs.
- Available in a high density 256-pin SBGA package (27mm x 27mm).

The receiver section:

- Provides frame synchronization for the M23 or C-bit parity DS3 applications, alarm detection, and accumulates line code violations, framing errors, parity errors, path parity errors and FEBE events. In addition, far end alarm channel

codes are detected, and an integral HDLC receiver is provided to terminate the path maintenance data link.

- Provides frame synchronization for the G.751 or G.832 E3 applications, alarm detection, and accumulates line code violations, framing errors, parity errors, and FEBE events. In addition, in G.832, the Trail Trace is detected, and an integral HDLC receiver is provided to terminate either the Network Requirement or the General Purpose data link.

- Provides frame synchronization for G.704 and NTT 6.312 Mbit/s J2 applications, alarm detection, and accumulates line code violations, framing errors, and CRC parity errors. An integral HDLC receiver is provided to terminate the data link.

- Provides frame synchronization, cell delineation and extraction for DS3, G.751 E3, G.832 E3, and G.704 and NTT J2 ATM direct-mapped formats.

- Provides PLCP frame synchronization, path overhead extraction, and cell extraction for DS1 PLCP, DS3 PLCP, E1 PLCP, and G.751 E3 PLCP formatted streams.

- Provides a 50 MHz 8-bit wide or 16-bit wide Utopia FIFO buffer in the receive path with parity support, and multi-PHY (Level 2) control signals.

- Provides ATM framing using cell delineation. ATM cell delineation may optionally be disabled to allow passing of all cell bytes regardless of cell delineation status.

- Provides cell descrambling, header check sequence (HCS) error detection, idle cell filtering, header descrambling (for use with PPP packets), and accumulates the number of received idle cells, the number of received cells written to the FIFO, and the number of HCS errors.

- Provides a four cell FIFO for rate decoupling between the line, and a higher layer processing entity. FIFO latency may be reduced by changing the number of operational cell FIFOs.

- Provides a receive HDLC controller with a 128-byte FIFO to accumulate data link information.

- Provides detection of yellow alarm and loss of frame (LOF), and accumulates BIP-8 errors, framing errors and FEBE events.

- Provides programmable pseudo-random test-sequence detection (up to 2^{32}-1 bit length patterns conforming to ITU-T O.151 standards) and analysis features.

The transmitter section:

- Provides frame insertion for the M23 or C-bit parity DS3 applications, alarm insertion, and diagnostic features. In addition, far end alarm channel codes may be inserted, and an integral HDLC transmitter is provided to insert the path maintenance data link.

- Provides frame insertion for the G.751 or G.832 E3 applications, alarm insertion, and diagnostic features. In addition, for G.832, the Trail Trace is inserted, and an integral HDLC transmitter is provided to insert either the Network Requirement or the General Purpose data link.

- Provides frame insertion for G.704 6.312 Mbit/s J2 applications, alarm insertion, and diagnostic features. An integral HDLC transmitter is provided to insert the path maintenance data link.

- Provides frame insertion and path overhead insertion for DS1, DS3, E1 or E3 based PLCP formats. In addition, alarm insertion and diagnostic features are provided.

- Provides a 50 MHz 8-bit wide or 16-bit wide Utopia FIFO buffer in the transmit path with parity support and multi-PHY (Level 2) control signals.

- Provides optional ATM cell scrambling, header scrambling (for use with PPP packets), HCS generation/insertion, programmable idle cell insertion, diagnostics features and accumulates transmitted cells read from the FIFO.

- Provides a four cell FIFO for rate decoupling between the line and a higher layer processing entity. FIFO latency may be reduced by changing the number of operational cell FIFOs.

- Provides a transmit HDLC controller with a 128-byte FIFO.

- Provides an 8 kHz reference input for locking the transmit PLCP frame rate to an externally applied frame reference.

- Provides programmable pseudo-random test sequence generation (up to 2^{32}-1 bit length sequences conforming to ITU-T O.151 standards).

Diagnostic abilities include single bit error insertion or error insertion at bit error rates ranging from 10^{-1} to 10^{-7}.

Bypass and Loopback features:

- Allows bypassing of the DS3, E3, and J2 framers to enable transmission system sublayer processing by an external device (for example, the PM4344 Quad DS1 Framer may be used for DS1-based services, and the PM6344 Quad E1 Framer may be used for E1-based services).
- Allows bypassing of the PLCP and ATM functions to enable use of the S/UNI-QJET as a quad DS3, E3, or J2 framer.
- Provides for diagnostic loopbacks, line loopbacks, and payload loopbacks.

2 APPLICATIONS

- ATM or SMDS Switches, Multiplexers, and Routers
- SONET/SDH Mux E3/DS3 Tributary Interfaces
- PDH Mux J2/E3/DS3 Line Interfaces
- DS3/E3/J2 Digital Cross Connect Interfaces
- DS3/E3/J2 PPP Internet Access Interfaces
- DS3/E3/J2 Frame Relay Interfaces

3 REFERENCES

1. ANSI T1.627 - 1993, "Broadband ISDN - ATM Layer Functionality and Specification".

2. ANSI T1.107a - 1990, "Digital Hierarchy - Supplement to Formats Specifications (DS3 Format Applications)".

3. ANSI T1.107 - 1995, "Digital Hierarchy - Formats Specifications".

4. ANSI T1.646 - 1995, "Broadband ISDN - Physical Layer Specification for User-Network Interfaces Including DS1/ATM".

5. ATM Forum - ATM User-Network Interface Specification, V3.1, October, 1995.

6. ATM Forum - “UTOPIA, An ATM PHY Interface Specification, Level 2, Version 1”, June, 1995.

7. ATM Forum, 94-0406R5, "E3 (34,368 kbps) Physical Layer Interface", Dec. 21, 1994.

8. ATM Forum, 95-1207R1, "DS3 Physical Layer Interface Specification", December 1995.

9. ATM Forum, af-phy-0029.000, "6,312 Kbps UNI Specification, Version 1.0", June 1995.

10. Bell Communications Research, TA-TSY-000773 - “Local Access System Generic Requirements, Objectives, and Interface in Support of Switched Multi-megabit Data Service” Issue 2, March 1990 and Supplement 1, December 1990.

11. ETS 300 269 Draft Standard T/NA(91)17 - “Metropolitan Area Network Physical Layer Convergence Procedure for 2.048 Mbit/s”, April 1994.

12. ETS 300 270 Draft Standard T/NA(91)18 - “Metropolitan Area Network Physical Layer Convergence Procedure for 34.368 Mbit/s”, April 1994.

13. ITU-T Recommendation O.151 - "Error Performance Measuring Equipment Operating at the Primary Rate and Above", October, 1992.

14. ITU-T Recommendation I.432 - "B-ISDN User-Network Interface - Physical Layer Specification", 1993

15. ITU-T Recommendation G.703 - "Physical/Electrical Characteristics of Hierarchical Digital Interfaces", 1991.

16. ITU-T Recommendation G.704 - "General Aspects of Digital Transmission Systems; Terminal Equipments - Synchronous Frame Structures Used At 1544, 6312, 2048, 8488 and 44 736 kbit/s Hierarchical Levels", July, 1995.

17. ITU-T Recommendation G.751 - CCITT Blue Book Fasc. III.4, "Digital Multiplex Equipments Operating at the Third Order Bit Rate of 34,368 kbit/s and the Fourth Order Bit Rate of 139,264 kbit/s and Using Positive Justification", 1988.

18. ITU-T Draft Recommendation G.775 - "Loss of Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection and Clearance Criteria", October 1993.

19. ITU-T Recommendation G.804 - "ATM Cell Mapping into Plesiochronous Digital Hierarchy (PDH)", 1993.

20. ITU-T Recommendation G.832 - "Transport of SDH Elements on PDH Networks: Frame and Multiplexing Structures", 1993.

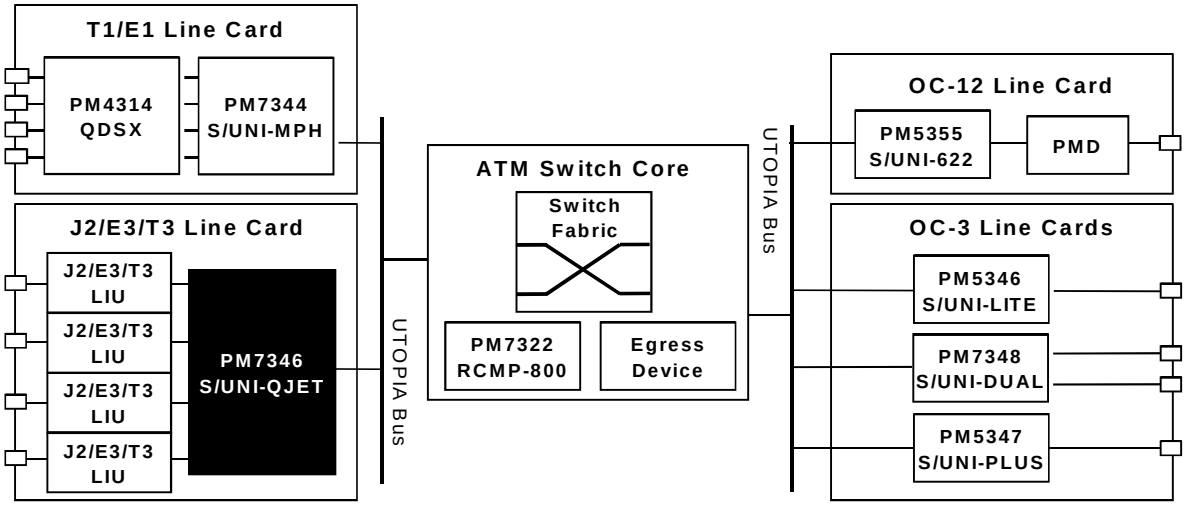
21. ITU-T Recommendation Q.921 - "ISDN User-Network Interface - Data Link Layer Specification", March, 1993.

22. NTT Technical Reference, "NTT Technical Reference for High-Speed Digital Leased Circuit Services", 1991.

4 APPLICATION EXAMPLES

The S/UNI-QJET can be configured as an ATM physical layer device. On the line side, it connects to one or more J2/E3/T3 line interface units and on the system side, the S/UNI-QJET interfaces to the ATM layer device, such as PM7322 RCMP-800, over an 8 or 16 bit wide UTOPIA Level 2 interface (as shown in Figure 1).

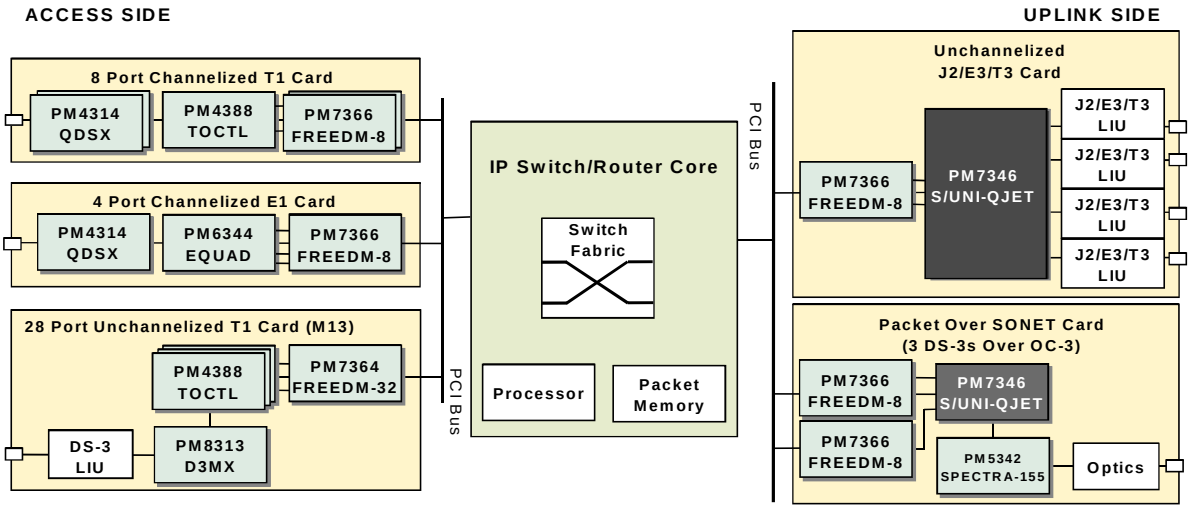
Figure 1 - S/UNI-QJET, as an ATM PHY, in an ATM Switch



S/UNI-QJET can be configured as a quad J2/E3/T3 framer for use in router, frame relay switch and multiplexer applications (as shown in Figure 2). In an unchannelized J2/E3/T3 line card, S/UNI-QJET interfaces directly to one or more PM7366 FREEDM-8 HDLC controllers. Each FREEDM-8 can process two high-speed links, such as T3 and E3, or it can process up to eight lower speed links such as J2. The S/UNI-QJET can gap all the overhead bits such that only the payload data is passed to and from FREEDM-8. On the line side, S/UNI-QJET is connected to one or more J2/E3/T3 line interface units. On the system side, S/UNI-QJET interfaces with a data link device over a serial bit interface.

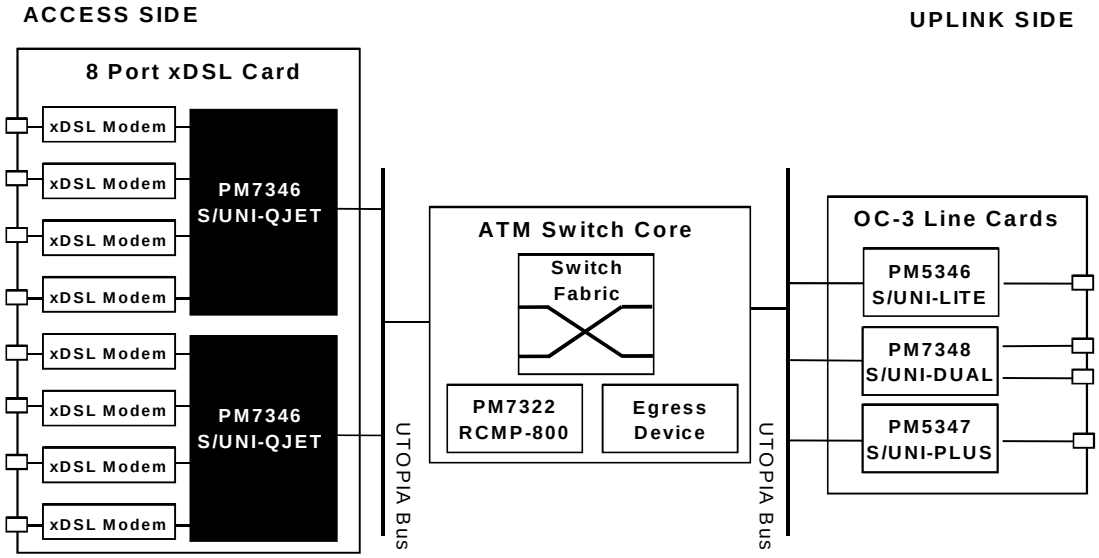
In a PPP-Over-SONET application, the S/UNI-QJET interfaces to PM5342 SPECTRA-155 to map three T3 data streams onto three corresponding STS-1 services that are collectively carried over an OC-3 link.

Figure 2 - S/UNI-QJET, as a Quad Framer Device, in Frame Relay Equipment



The S/UNI-QJET can be configured as a cell processor to provide cell mapping functions for xDSL modems in an ATM based Digital Subscriber Loop Access Multiplexer (DSLAM) equipment. As shown in Figure 3, each S/UNI-QJET provides four cell processors. Two S/UNI-QJETs are required in an 8 port xDSL line card.

Figure 3 - S/UNI-QJET, as a Cell Processor, in DSLAM Equipment



5 BLOCK DIAGRAM

Figure 4 - Normal Operating Mode

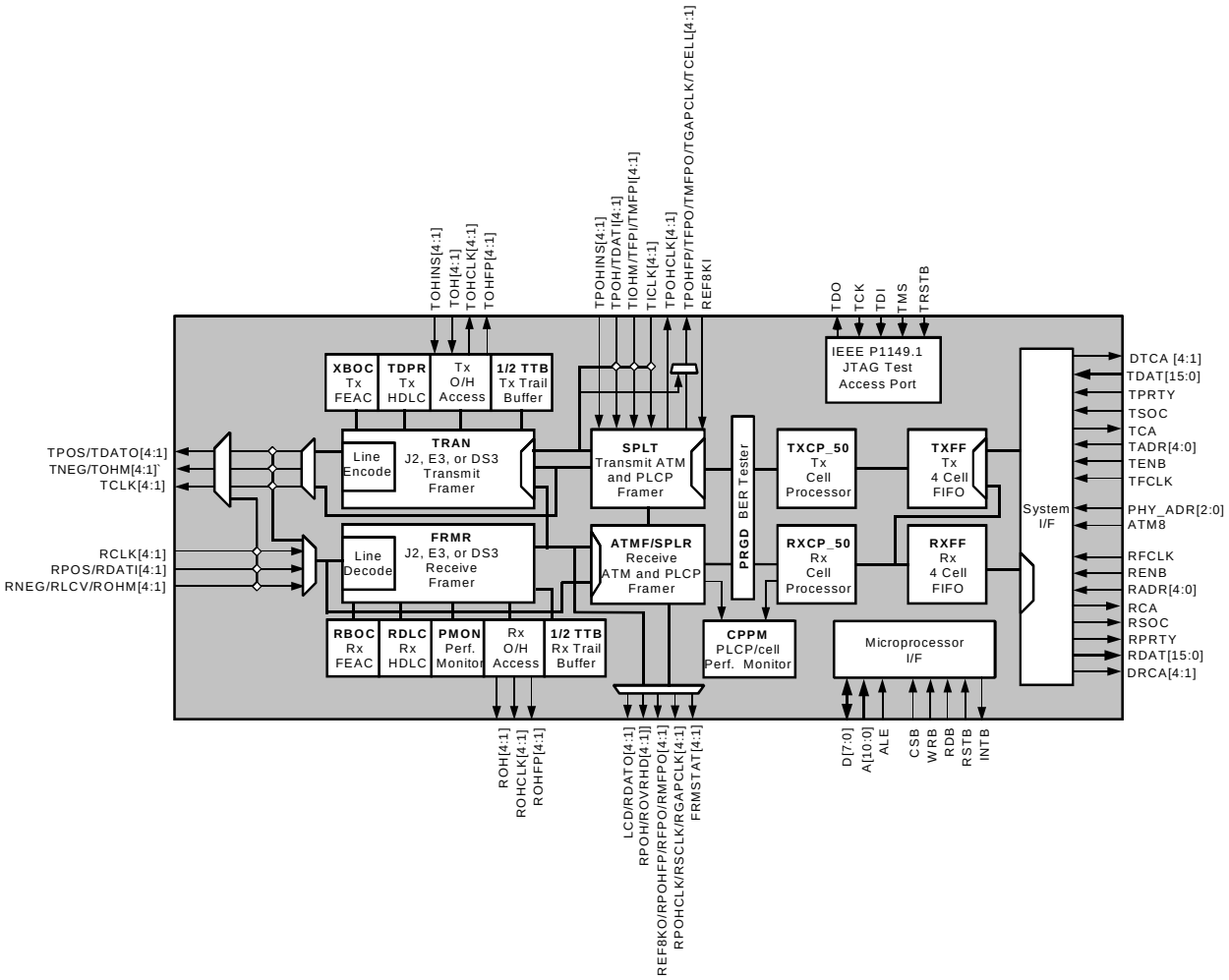


Figure 5 - DS3/E3/J2 Framers Bypassed

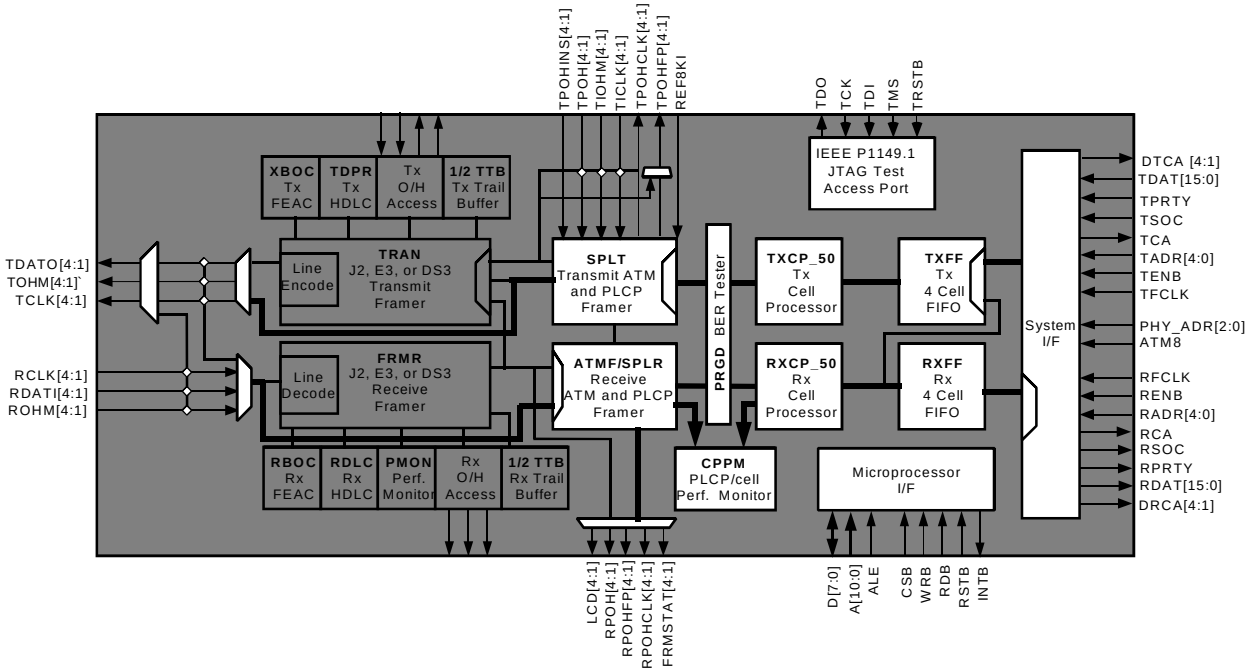


Figure 6 - DS3/E3/J2 Transceiver Mode

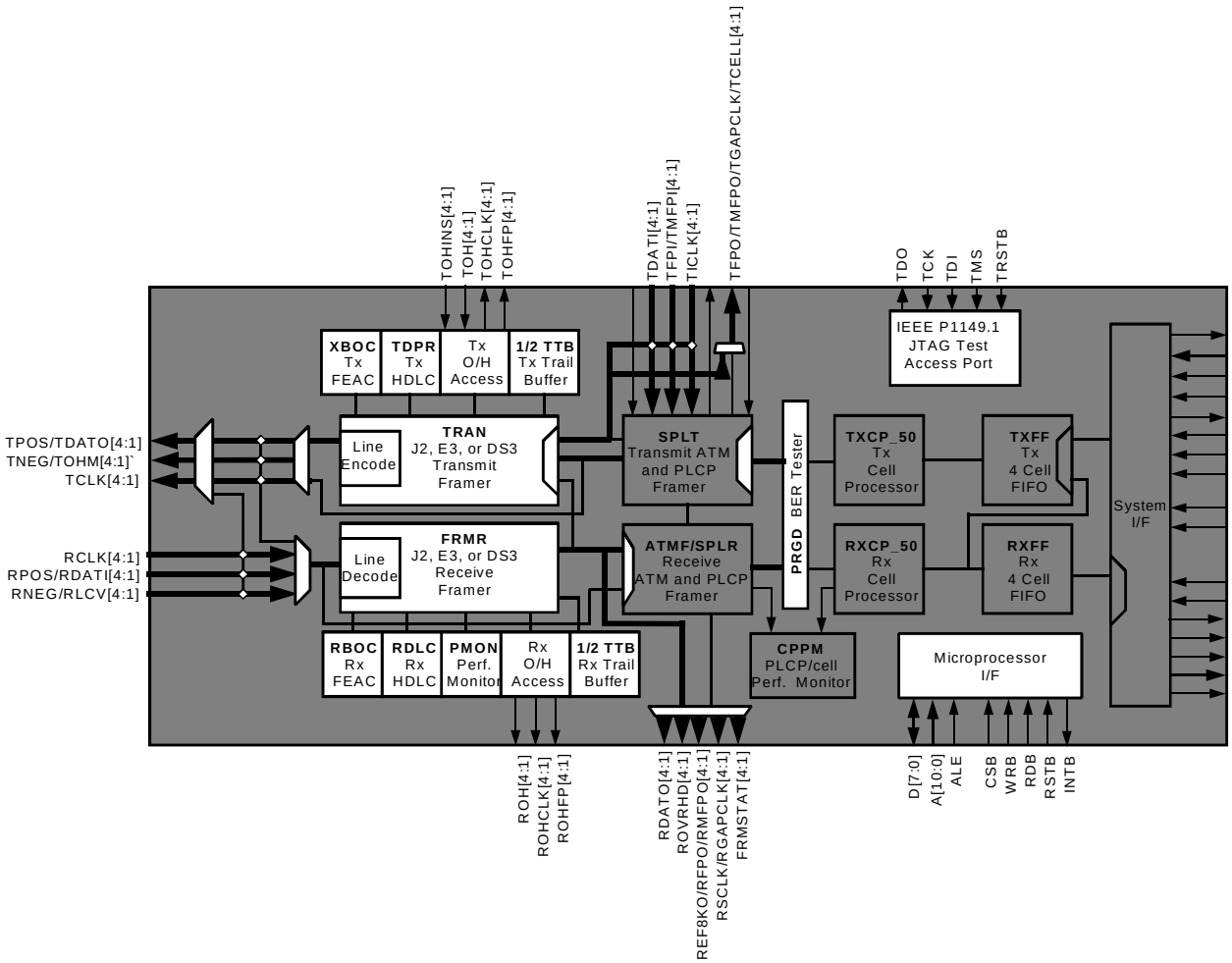
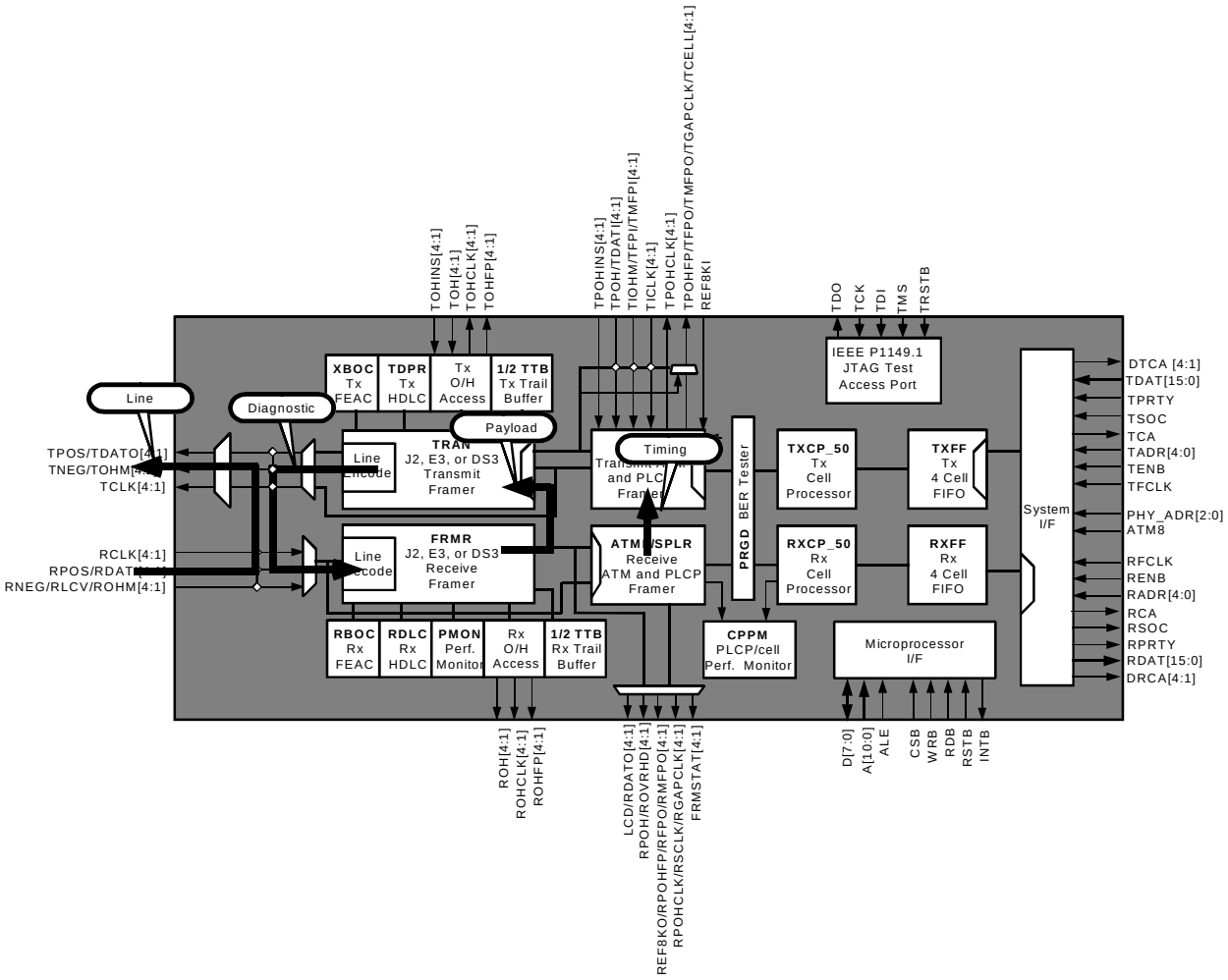


Figure 7 - Loopback Modes



6 DESCRIPTION

The PM7346 S/UNI-QJET is a quad ATM physical layer processor with integrated DS3, E3, and J2 framers. PLCP sublayer DS1, DS3, E1, and E3 processing is supported as is ATM cell delineation.

The S/UNI-QJET contains integral DS3 framers, which provide DS3 framing and error accumulation in accordance with ANSI T1.107, and T1.107a, integral E3 framers, which provide E3 framing in accordance with ITU-T Recommendations G.832 and G.751, and integral J2 framers, which provide J2 framing in accordance with ITU-T Recommendation G.704 and I.432.

When configured for DS3 transmission system sublayer processing, the S/UNI-QJET accepts and outputs both digital B3ZS-encoded bipolar and unipolar signals compatible with M23 and C-bit parity applications.

When configured for E3 transmission system sublayer processing, the S/UNI-QJET accepts and outputs both HDB3-encoded bipolar and unipolar signals compatible with G.751 and G.832 applications.

When configured for J2 transmission system sublayer processing, the S/UNI-QJET accepts and outputs both B8ZS-encoded bipolar and unipolar signals compliant with G.704 and NTT 6.312 Mbit/s applications.

When configured for DS1, or E1 transmission system sublayer processing, the S/UNI-QJET accepts and outputs unipolar signals with appropriate clock and frame pulse signals for physical sublayer processing. When configured for other transmission systems, the S/UNI-QJET provides a generic interface for physical sublayer processing.

In the DS3 receive direction, the S/UNI-QJET frames to DS3 signals with a maximum average reframe time of 1.5 ms and detects line code violations, loss of signal, framing bit errors, parity errors, path parity errors, AIS, far end receive failure and idle code. The DS3 overhead bits are extracted and presented on serial outputs. When in C-bit parity mode, the Path Maintenance Data Link and the Far End Alarm and Control (FEAC) channels are extracted. HDLC receivers are provided for Path Maintenance Data Link support. In addition, valid bit-oriented codes in the FEAC channels are detected and are available through the microprocessor port.

In the E3 receive direction, the S/UNI-QJET frames to G.751 and G.832 E3 signals with a maximum average reframe times of 135µs for G.751 frames and 250µs for G.832 frames. Line code violations, loss of signal, framing bit errors,

AIS, and remote alarm indication are detected. Further, when processing G.832 formatted data, parity errors, far end receive failure, and far end block errors are also detected; and the Trail Trace message may be extracted and made available through the microprocessor port. HDLC receivers are provided for either the G.832 Network Requirement or the G.832 General Purpose Data Link support.

In the J2 receive direction, the S/UNI-QJET frames to G.704 6.312 MHz signals with a maximum average reframe time of 5.07ms. An alternate framing algorithm which uses the CRC-5 bits to rule out 99.9% of all static mimic framing patterns is available with a maximum average reframe time of 10.22ms when operating with a 10^{-4} bit error rate. The alternate framing algorithm can be selected via the CRC_REFR bit in the J2-FRMR Configuration Register. Line code violations, loss of signal, loss of frame, framing bit errors, physical layer AIS, payload AIS, CRC-5 errors, Remote End Alarm, and Remote Alarm Indication are detected. HDLC receivers are provided for Data Link support.

Error event accumulation is also provided by the S/UNI-QJET. Framing bit errors, line code violations, parity errors, path parity errors and far end block errors are accumulated, when appropriate, in saturating counters for DS3, E3, and J2 frames. Loss of Frame detection for DS3, E3, and J2 is provided as recommended by ITU-T G.783 with integration times of 1ms, 2ms, and 3ms.

In the DS3 transmit direction, the S/UNI-QJET inserts DS3 framing, X and P bits. When enabled for C-bit parity operation, bit-oriented code transmitters and HDLC transmitters are provided for insertion of the FEAC channels and the Path Maintenance Data Links into the appropriate overhead bits. Alarm Indication Signals can be inserted by using internal register bits; other status signals such as the idle signal can be inserted when enabled by internal register bits. When M23 operation is selected, the C-bit Parity ID bit (the first C-bit of the first M sub-frame) is forced to toggle so that downstream equipment will not confuse an M23-formatted stream with stuck-at 1 C-bits for C-bit Parity application.

In the E3 transmit direction, the S/UNI-QJET inserts E3 framing in either G.832 or G.751 format. When enabled for G.832 operation, an HDLC transmitter is provided for insertion of either the Network Requirement or General Purpose Data Link into the appropriate overhead bits. The Alarm Indication Signal and other status signals can be inserted by internal register bits.

In the J2 transmit direction, the S/UNI-QJET inserts J2 6.312 Mbit/s G.704 framing. HDLC transmitter are provided for insertion of the Data Links. CRC-5 check bits are calculated and inserted into the J2 multiframe. External pins are provided to enable overwriting of any of the overhead bits within the J2 frame.

The S/UNI-QJET also supports diagnostic options which allow it to insert, when appropriate for the transmit framing format, parity or path parity errors, F-bit framing errors, M-bit framing errors, invalid X or P-bits, line code violations, all-zeros, AIS, Remote Alarm Indications, and Remote End Alarms.

The S/UNI-QJET provides cell delineation for ATM cells using the PLCP framing format, or by using the header check sequence octet in the ATM cell header as specified by ITU-T Recommendation I.432. DS1, DS3, E1 and E3 based PLCP frame formats can be processed. Non-PLCP-based cell delineation is accomplished with either bit, nibble, or byte-wide search algorithms, depending on the line interface used. An interface consistent with the generic physical interface defined by ITU-T Recommendation I.432 is provided for arbitrary rates up to 52 Mbit/s. This interface is used to provide physical layer support for transmission systems that do not have an associated PLCP sublayer, or to provide an efficient means of directly mapping ATM cells to existing transmission system formats (such as DS3 and DS1).

In the PLCP receive direction, framing, path overhead extraction and cell extraction is provided. BIP-8 error events, frame octet error events and far end block error events are accumulated.

In the PLCP transmit direction, the S/UNI-QJET provides overhead insertion using inputs or internal registers, DS3 nibble and E3 byte stuffing, automatic BIP-8 octet generation and insertion and automatic far end block error insertion. Diagnostic features for BIP-8 error, framing error and far end block error insertion are also supported.

In the cell receive path, idle cells may be dropped according to a programmable filter. By default, incoming cells with single bit HCS errors are corrected and written to the FIFO buffer. Optionally, cells can be dropped upon detection of a HCS error. Cell delineation may optionally be disabled to allow passing of all cells, regardless of cell delineation status. The ATM cell payloads are optionally descrambled. ATM cell headers may optionally be descrambled (for use with PPP packets). Assigned cells containing no detectable HCS errors are written to a FIFO buffer. Cells data is read from the FIFO using a synchronous 50 MHz 8-bit wide or 16-bit wide SCI-PHY^{TM} and Utopia Level 2 compatible interface. Cell data parity is also provided. Counts of error-free assigned cells, and cells containing HCS errors are accumulated independently for performance monitoring purposes.

In the cell transmit path, cell data is written to a FIFO buffer using a synchronous 50 MHz 8-bit wide or 16-bit wide SCI-PHY^{TM} compatible interface. Cell data parity is also examined for errors. Idle cells are automatically inserted when the FIFO contains less than one full cell. HCS generation, cell payload scrambling,

and cell header scrambling (for use with PPP packets) are optionally provided. Counts of transmitted cells are accumulated for performance monitoring purposes.

Both receive and transmit cell FIFOs provide buffering for four cells. The FIFOs provide the rate matching interface between the higher layer ATM entity and the S/UNI-QJET.

The S/UNI-QJET is configured, controlled and monitored via a generic 8-bit microprocessor bus through which all internal registers are accessed. All sources of interrupts can be identified, acknowledged, or masked via this interface.

7 PIN DIAGRAM

The S/UNI-QJET is packaged in a 256-pin SBGA package having a body size of 27mm by 27mm and a pin pitch of 1.27 mm.

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	VSS	VSS	VSS	TDAT[10]	TDAT[14]	D[1]	D[5]	VSS	A[3]	A[7]	VSS	VSS	ALE	INTB	TRSTB	TNEG[4]	RCLK[4]	VSS	VSS	VSS	A
B	VSS	VDD	VDD	TDAT[9]	TDAT[13]	D[0]	D[4]	A[0]	A[2]	A[6]	A[9]	A[10]	WRB	TDO	TCK	TCLK[4]	TPOS[3]	VDD	VDD	VSS	B
C	VSS	VDD	VDD	TDAT[7]	TDAT[11]	TDAT[15]	D[2]	D[6]	A[1]	A[5]	A[8]	CSB	RSTB	TMS	TPOS[4]	RNEG[4]	TCLK[3]	VDD	VDD	VSS	C
D	TDAT[3]	TDAT[4]	TDAT[6]	NC	TDAT[8]	TDAT[12]	VDD	D[3]	D[7]	A[4]	VDD	RDB	TDI	VDD	RPOS[4]	TNEG[3]	BIAS	TPOS[2]	TCLK[2]	RPOS[3]	D
E	TFCLK	TDAT[0]	TDAT[2]	TDAT[5]													TNEG[2]	RNEG[3]	RPOS[2]	RNEG[2]	E
F	TADR[2]	TADR[3]	TADR[4]	TDAT[1]													RCLK[3]	RCLK[2]	TPOS[1]	TNEG[1]	F
G	TSOC	TPRTY	TADR[1]	VDD													VDD	TCLK[1]	RNEG[1]	RCLK[1]	G
H	BIAS	TCA	TENB	TADR[0]													RPOS[1]	TOH[4]	TOHCLK[4]	VSS	H
J	VSS	DTCA[2]	DTCA[3]	DTCA[4]													TOHINS[4]	TOHFP[4]	ROH[4]	ROHFP[4]	J
K	VSS	DTCA[1]	PHY_ADR[2]	VDD						BOTTOM VIEW							ROHCLK[4]	TOH[3]	TOHINS[3]	TOHCLK[3]	K
L	PHY_ADR[1]	PHY_ADR[0]	ATM8	DRCA[4]													VDD	TOHFP[3]	ROH[3]	VSS	L
M	DRCA[3]	DRCA[2]	DRCA[1]	RSOC													TOHINS[2]	ROHCLK[3]	ROHFP[3]	VSS	M
N	VSS	RCA	RENB	RADR[3]													ROHCLK[2]	TOHFP[2]	TOHCLK[2]	TOH[2]	N
P	RFCLK	RADR[4]	RADR[2]	VDD													VDD	TOH[1]	ROHFP[2]	ROH[2]	P
R	RADR[1]	RADR[0]	RPRTY	RDAT[13]													ROHCLK[1]	TOHFP[1]	TOHCLK[1]	TOHINS[1]	R
T	RDAT[15]	RDAT[14]	RDAT[12]	RDAT[9]													FRMSTAT[2]	REF8KI	ROHFP[1]	ROH[1]	T
U	RDAT[11]	RDAT[10]	RDAT[8]	BIAS	RDAT[6]	RDAT[2]	VDD	TPOHCLK[4]	REF8KO[4]	VDD	RPOHCLK[3]	TPOHINS[2]	RPOH[2]	VDD	TPOHCLK[1]	RPOHCLK[1]	BIAS	FRMSTAT[1]	FRMSTAT[3]	FRMSTAT[4]	U
V	VSS	VDD	VDD	RDAT[7]	RDAT[3]	TICLK[4]	TPOHINS[4]	RPOH[4]	TIOHM[3]	TPOHCLK[3]	RPOH[3]	TIOHM[2]	TPOHCLK[2]	RPOHCLK[2]	TIOHM[1]	TPOHFP[1]	REF8KO[1]	VDD	VDD	VSS	V
W	VSS	VDD	VDD	RDAT[5]	RDAT[1]	TIOHM[4]	TPOHFP[4]	RPOHCLK[4]	TPOH[3]	TPOHINS[3]	LCD[3]	TICLK[2]	TPOH[2]	LCD[2]	TICLK[1]	TPOHINS[1]	RPOH[1]	VDD	VDD	VSS	W
Y	VSS	VSS	VSS	RDAT[4]	RDAT[0]	TPOH[4]	LCD[4]	TICLK[3]	VSS	VSS	TPOHFP[3]	REF8KO[3]	VSS	TPOHFP[2]	REF8KO[2]	TPOH[1]	LCD[1]	VSS	VSS	VSS	Y
	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

8 PIN DESCRIPTION

Pin Name	Type	Pin No.	Function
TPOS[4] TPOS[3] TPOS[2] TPOS[1] TDATO[4] TDATO[3] TDATO[2] TDATO[1]	Output	C6 B4 D3 F2	Transmit Digital Positive Pulse (TPOS[4:1]). TPOS[4:1] contains the positive pulses transmitted on the B3ZS-encoded DS3, HDB3-encoded E3, or B8ZS-encoded J2 transmission system when the dual-rail output format is selected. Transmit Data (TDATO[4:1]). TDATO[4:1] contains the transmit data stream when the single-rail (unipolar) output format is enabled or when a non-DS3/E3/J2 based transmission system is selected. The TPOS/TDATO[4:1] pin function selection is controlled by the TFRM[1:0] and the TUNI bits in the S/UNI-QJET Transmit Configuration Registers. Output signal polarity control is provided by the TPOSINV bit in the S/UNI-QJET Transmit Configuration Registers. Both TPOS[4:1] and TDATO[4:1] are updated on the falling edge of TCLK[4:1] by default, and may be configured to be updated on the rising edge of TCLK[4:1] through the TCLKINV bit in the S/UNI-QJET Transmit Configuration Registers. Finally, both TPOS[4:1] and TDATO[4:1] can be updated on the rising edge of TICLK[4:1], enabled by the TICLK bit in the S/UNI-QJET Transmit Configuration Registers.
TNEG[4] TNEG[3] TNEG[2] TNEG[1]	Output	A5 D5 E4 F1	Transmit Digital Negative Pulse (TNEG[4:1]). TNEG[4:1] contains the negative pulses transmitted on the B3ZS-encoded DS3, HDB3-encoded E3, or B8ZS-encoded J2 transmission system when the dual-rail NRZ output format is selected.

Pin Name	Type	Pin No.	Function
TOHM[4] TOHM[3] TOHM[2] TOHM[1]	Output	A5 D5 E4 F1	Transmit Overhead Mask (TOHM[4:1]). TOHM[4:1] indicates the position of overhead bits (non-payload bits) in the transmission system stream aligned with TDATO[4:1]. TOHM[4:1] indicates the location of the M-frame boundary for DS3, the position of the frame boundary for E3, and the position of the multi-frame boundary for J2 when the single-rail (unipolar) NRZ input format is enabled. When a PLCP formatted signal is transmitted, TOHM[4:1] is set to logic 1 once per transmission frame, and indicates the DS1 or E1 frame alignment. When a non-PLCP, non-DS3, non-E3, non-J2 based signal is transmitted, TOHM[4:1] is a delayed version of the TIOHM[4:1] input, and indicates the position of each overhead bit in the transmission frame. TOHM[4:1] is updated on the falling edge of TCLK[4:1]. The TNEG/TOHM[4:1] pin function selection is controlled by the TFRM[1:0] and the TUNI bits in the S/UNI-QJET Transmit Configuration Registers. Output signal polarity control is provided by the TNEGINV bit in the S/UNI-QJET Transmit Configuration Registers. Both TNEG[4:1] and TOHM[4:1] are updated on the falling edge of TCLK[4:1] by default, and may be enabled to be updated on the rising edge of TCLK[4:1]. This sampling is controlled by the TCLKINV bit in the S/UNI-QJET Transmit Configuration Registers. Finally, both TNEG[4:1] and TOHM[4:1] can be updated on the rising edge of TICLK[4:1], enabled by the TICLK bit in the S/UNI-QJET Transmit Configuration Registers.

Pin Name	Type	Pin No.	Function
TCLK[4] TCLK[3] TCLK[2] TCLK[1]	Output	B5 C4 D2 G3	Transmit Output Clock (TCLK[4:1]). TCLK[4:1] provides the transmit direction timing. TCLK[4:1] is a buffered version of TICLK[4:1] and can be enabled to update the TPOS/TDATO[4:1] and TNEG/TOHM[4:1] outputs on its rising or falling edge.
RPOS[4] RPOS[3] RPOS[2] RPOS[1]	Input	D6 D1 E2 H4	Receive Digital Positive Pulse (RPOS[4:1]). RPOS[4:1] contains the positive pulses received on the B3ZS-encoded DS3, the HDB3-encoded E3, or the B8ZS-encoded J2 transmission system when the dual-rail NRZ input format is selected.
RDATI[4] RDATI[3] RDATI[2] RDATI[1]			Receive Data (RDATI[4:1]). RDATI[4:1] contains the data stream when the single-rail (unipolar) NRZ input format is enabled or when a non-DS3/E3/J2 based transmission system is being processed (for example RDATI may contain a DS1 or E1 stream). The RPOS/RDATI[4:1] pin function selection is controlled by the RFRM[1:0] bits in the S/UNI-QJET Configuration Registers and by the UNI bits in the DS3 FRMR, the E3 FRMR, or the J2 FRMR Configuration Registers. Both RPOS[4:1] and RDATI[4:1] are sampled on the rising edge of RCLK[4:1] by default, and may be enabled to be sampled on the falling edge of RCLK[4:1]. This sampling is controlled by the RCLKINV bit in the S/UNI-QJET Receive Configuration Registers. In addition, signal polarity control is provided by the RPOSINV bit in the S/UNI-QJET Receive Configuration Registers.

Pin Name	Type	Pin No.	Function
RNEG[4] RNEG[3] RNEG[2] RNEG[1]	Input	C5 E3 E1 G2	Receive Digital Negative Pulse (RNEG[4:1]). RNEG[4:1] contains the negative pulses received on the B3ZS encoded DS3, the HDB3-encoded E3, or the B8ZS-encoded J2 transmission system when the dual-rail NRZ input format is selected.
RLCV[4] RLCV[3] RLCV[2] RLCV[1]			Receive Line Code Violation (RLCV[4:1]). RLCV[4:1] contains line code violation indications when the single-rail (unipolar) NRZ input format is enabled for DS3, E3, or J2 applications. Each line code violation is represented by an RCLK[4:1] period-wide pulse.

Pin Name	Type	Pin No.	Function
ROHM[4] ROHM[3] ROHM[2] ROHM[1]	Input	C5 E3 E1 G2	Receive Overhead Mask (ROHM[4:1]). When a DS1 or E1 PLCP or ATM direct-mapped signal is received, ROHM[4:1] is pulsed once per transmission frame, and indicates the DS1 or E1 frame alignment relative to the RDATI[4:1] data stream. When an alternate frame-based signal is received, ROHM[4:1] indicates the position of each overhead bit in the transmission frame. The RNEG/RLCV/ROHM[4:1] pin function selection is controlled by the RFRM[1:0] bits in the S/UNI-QJET Receive Configuration Registers, the UNI bits in the DS3 FRMR, E3 FRMR, or J2 FRMR Configuration Registers, and the PLCPEN and EXT bits in the SPLR Configuration register. RNEG[4:1], RLCV[4:1], and ROHM[4:1] are sampled on the rising edge of RCLK[4:1] by default, and may be enabled to be sampled on the falling edge of RCLK[4:1]. This sampling is controlled by the RCLKINV bit in the S/UNI-QJET Receive Configuration Registers. In addition, signal polarity control is provided by the RNEGINV bit in the S/UNI-QJET Receive Configuration Registers.
RCLK[4] RCLK[3] RCLK[2] RCLK[1]	Input	A4 F4 F3 G1	Receive Clock (RCLK[4:1]). RCLK[4:1] provides the receive direction timing. RCLK[4:1] is the externally recovered transmission system baud rate clock that samples the RPOS/RDATI[4:1] and RNEG/RLCV/ROHM[4:1] inputs on its rising or falling edge.

Pin Name	Type	Pin No.	Function
TOHINS[4] TOHINS[3] TOHINS[2] TOHINS[1]	Input	J4 K2 M4 R1	Transmit DS3/E3/J2 Overhead Insertion (TOHINS[4:1]). TOHINS[4:1] controls the insertion of the DS3, E3, or J2 overhead bits from the TOH[4:1] input. When TOHINS[4:1] is high, the associated overhead bit in the TOH[4:1] stream is inserted in the transmitted DS3, E3, or J2 frame. When TOHINS[4:1] is low, the DS3, E3, or J2 overhead bit is generated and inserted internally. TOHINS[4:1] is sampled on the rising edge of TOHCLK[4:1]. If TOHINS[4:1] is a logic 1, the TOH[4:1] input has precedence over the internal datalink transmitter, or any internal register bit setting.

Pin Name	Type	Pin No.	Function
TOH[4] TOH[3] TOH[2] TOH[1]	Input	H3 K3 N1 P3	Transmit DS3/E3/J2 Overhead Data (TOH[4:1]). When configured for DS3 operation, TOH[4:1] contains the overhead bits (C, F, X, P, and M) that may be inserted in the transmit DS3 stream. When configured for G.832 E3 operation, TOH[4:1] contains the overhead bytes (FA1, FA2, EM mask, TR, MA, NR, and GC) that may be inserted in the transmit G.832 E3 stream. When configured for G.751 E3 operation, TOH[4:1] contains the overhead bits (RAI, National Use, Stuff Indication, and Stuff Opportunity) that may be inserted in the transmit G.751 E3 stream. When configured for J2 operation, TOH[4:1] contains the overhead bits (TS97, TS98, Framing, X_{1-3}, A, M, E_{1-5}) that may be inserted in the transmit J2 stream. If TOHINS[4:1] is a logic 1, the TOH[4:1] input has precedence over the internal datalink transmitter, or any other internal register bit setting. TOH[4:1] is sampled on the rising edge of TOHCLK[4:1].

Pin Name	Type	Pin No.	Function
TOHFP[4] TOHFP[3] TOHFP[2] TOHFP[1]	Output	J3 L3 N3 R3	Transmit DS3/E3/J2 Overhead Frame Position (TOHFP[4:1]). TOHFP[4:1] is used to align the individual overhead bits in the transmit overhead data stream, TOH[4:1], to the DS3 M-frame or the E3 frame. For DS3, TOHFP[4:1] is high during the X1 overhead bit position in the TOH[4:1] stream. For G.832 E3, TOHFP[4:1] is high during the first bit of the FA1 byte. For G.751 E3, TOHFP[4:1] is high during the RAI overhead bit position in the TOH[4:1] stream. For J2, TOHFP[4:1] is high during the first bit of timeslot 97 in the first frame of a 4-frame multiframe). TOHFP[4:1] is updated on the falling edge of TOHCLK[4:1].
TOHCLK[4] TOHCLK[3] TOHCLK[2] TOHCLK[1]	Output	H2 K1 N2 R2	Transmit DS3/E3/J2 Overhead Clock (TOHCLK[4:1]). TOHCLK[4:1] is active when a DS3, E3, or J2 stream is being processed. TOHCLK[4:1] is nominally a 526 kHz clock for DS3, a 1.072 MHz clock for G.832 E3, a 1.074 MHz clock for G.751 E3, and a gapped 6.312 MHz clock with an average frequency of 168 kHz for J2. TOHFP[4:1] is updated on the falling edge of TOHCLK[4:1]. TOH[4:1], and TOHINS[4:1] are sampled on the rising edge of TOHCLK[4:1].

Pin Name	Type	Pin No.	Function
REF8KI	Input	T3	Reference 8 kHz Input (REF8KI). The PLCP frame rate is locked to an external 8 kHz reference applied on this input . An internal phase-frequency detector compares the transmit PLCP frame rate with the externally applied 8 kHz reference and adjusts the PLCP frame rate. The REF8KI input must transition high once every 125 µs for correct operation. The REF8KI input is treated as an asynchronous signal and must be “glitch-free”. If the LOOPT register bit is logic 1, the PLCP frame rate is locked to the RPOHFP[x] signal instead of the REF8KI input.
TPOHINS[4] TPOHINS[3] TPOHINS[2] TPOHINS[1]	Input	V14 W11 U9 W5	Transmit Path Overhead Insertion (TPOHINS[4:1]). TPOHINS[4:1] controls the insertion of PLCP overhead octets on the TPOH[4:1] input. When TPOHINS[4:1] is logic 1, the associated overhead bit in the TPOH[4:1] stream is inserted in the transmit PLCP frame. When TPOHINS[4:1] is logic 0, the PLCP path overhead bit is generated and inserted internally. TPOHINS[4:1] is sampled on the rising edge of TPOHCLK[4:1]. Note, when operating in G.751 E3 PLCP mode, bits 8, 7 and 6 of the C1 octet should not be manipulated.

Pin Name	Type	Pin No.	Function
TPOH[4] TPOH[3] TPOH[2] TPOH[1]	Input	Y15 W12 W8 Y5	Transmit PLCP Overhead Data (TPOH[4:1]). TPOH[4:1] is valid when the FRMRONLY bit in the S/UNI-QJET Configuration 1 registers is logic 0. TPOH[4:1] contains the PLCP path overhead octets (Zn, F1, B1, G1, M1, M2, and C1) which may be inserted in the transmit PLCP frame. The octet data on TPOH[4:1] is shifted in order from the most significant bit (bit 1) to the least significant bit (bit 8). TPOH[4:1] is sampled on the rising edge of TPOHCLK[4:1].
TDATI[4] TDATI[3] TDATI[2] TDATI[1]			Framer Transmit Data (TDATI[4:1]). TDATI[4:1] contains the serial data to be transmitted when the S/UNI-QJET is configured as a DS3, E3, or J2 framer device for non-ATM applications by setting the FRMRONLY bit in the S/UNI-QJET Configuration 1 Register. TDATI[4:1] is sampled on the rising edge of TICLK[4:1] if the TXGAPEN register bit in the S/UNI-QJET Configuration 2 register is logic 0. If TXGAPEN is logic 1, then TDATI[4:1] is sampled on the falling edge of TGAPCLK[4:1].
TPOHFP[4] TPOHFP[3] TPOHFP[2] TPOHFP[1]	Output	W14 Y10 Y7 V5	Transmit Path Overhead Frame Position (TPOHFP[4:1]). TPOHFP[4:1] is valid when the FRMRONLY bit in the S/UNI-QJET Configuration 1 Registers is logic 0. The TPOHFP[4:1] output locates the individual PLCP path overhead bits in the transmit overhead data stream, TPOH[4:1]. TPOHFP[4:1] is logic 1 while bit 1 (the most significant bit) of the path user channel octet (F1) is present in the TPOH[4:1] stream. TPOHFP[4:1] is updated on the falling edge of TPOHCLK[4:1].

Pin Name	Type	Pin No.	Function
TFPO[4] TFPO[3] TFPO[2] TFPO[1]	Output	W14 Y10 Y7 V5	Framer Transmit Frame Pulse/Multi-frame Pulse Reference (TFPO/TMFPO[4:1]). TFPO/TMFPO[4:1] is valid when the S/UNI-QJET is configured as a DS3, E3, or J2 framer for non-ATM applications by setting the FRMRONLY bit in the S/UNI-QJET Configuration 1 Registers to logic 1 and the TXGAPEN bit in the S/UNI-QJET Configuration Registers to logic 0. TFPO[4:1] pulses high for 1 out of every 85 clock cycles when configured for DS3, giving a free-running mark for all overhead bits in the frame. TFPO[4:1] pulses high for 1 out of every 1536 clock cycles when configured for G.751 E3, giving a free-running reference G.751 indication. TFPO[4:1] pulses high for 1 out of every 4296 clock cycles when configured for G.832 E3, giving a free-running reference G.832 frame indication. TFPO[4:1] pulses high for 1 out of every 789 clock cycles when configured for J2, giving a free-running reference frame indication.
TMFPO[4] TMFPO[3] TMFPO[2] TMFPO[1]			TMFPO[4:1] pulses high for 1 out of every 4760 clock cycles when configured for DS3, giving a free-running reference M-frame indication. TMFPO[4:1] pulses high for 1 out of every 3156 clock cycles when configured for J2, giving a free-running reference multi-frame indication. TMFPO[4:1] behaves the same as TFPO[4:1] for E3 applications. TFPO/TMFPO[4:1] is updated on the rising edge of TICLK[4:1] or RCLK[4:1] if loop-timed.

Pin Name	Type	Pin No.	Function
TGAPCLK[4] TGAPCLK[3] TGAPCLK[2] TGAPCLK[1]	Output	W14 Y10 Y7 V5	Framer Gapped Transmit Clock (TGAPCLK[4:1]). TGAPCLK[4:1] is valid when the S/UNI-QJET is configured as a DS3, E3, or J2 framer for non-ATM applications by setting the FRMRONLY bit in the S/UNI-QJET Configuration 1 Registers and the TXGAPEN bit in the S/UNI-QJET Configuration 2 Registers. TGAPCLK[4:1] is derived from the transmit reference clock TICLK[4:1] or from the receive clock if loop-timed. The overhead bit (gapped) positions are generated internal to the device. TGAPCLK[4:1] is held high during the overhead bit positions. This clock is useful for interfacing to devices which source payload data only. TGAPCLK[4:1] is used to sample TDATI[4:1].
TCELL[4] TCELL[3] TCELL[2] TCELL[1]			Transmit Cell Indication (TCELL[4:1]). TCELL[x] is valid when the TCELL bit in the S/UNI-QJET Misc. register (09BH, 19BH, 29BH, 39BH) is set. TCELL[x] pulses once for every cell (idle or assigned) transmitted. TCELL[x] is updated using timing derived from the transmit input clock (TICLK[x]), and is active for a minimum of 8 TICLK[x] periods (or 8 RCLK[x] periods if loop-timed).

Pin Name	Type	Pin No.	Function
TPOHCLK[4] TPOHCLK[3] TPOHCLK[2] TPOHCLK[1]	Output	U13 V11 V8 U6	Transmit PLCP Overhead Clock (TPOHCLK[4:1]). TPOHCLK[4:1] is active when PLCP processing is enabled. TPOHCLK[4:1] is nominally a 26.7 kHz clock for a DS1 PLCP frame, a 768 kHz clock for a DS3 PLCP frame, a 33.7 kHz clock for an E1 based PLCP frame, and a 576 kHz clock for an G.751 E3 based PLCP frame. TPOHFP[4:1] is updated on the falling edge of TPOHCLK[4:1]. TPOH[4:1], and TPOHINS[4:1] are sampled on the rising edge of TPOHCLK[4:1].
TIOHM[4] TIOHM[3] TIOHM[2] TIOHM[1]	Input	W15 V12 V9 V6	Transmit Input Overhead Mask (TIOHM[4:1]). TIOHM[4:1] is valid only if the FRMRONLY bit in the S/UNI-QJET Configuration 1 register is logic 0. TIOHM[4:1] indicates the position of overhead bits when not configured for DS1, DS3, E1, E3, or J2 transmission system streams. TIOHM[4:1] is delayed internally to produce the TOHM[4:1] output. When configured for operation over a DS1, a DS3, an E1, an E3, or a J2 transmission system sublayer, TIOHM[4:1] is not required, and should be set to logic 0. When configured for other transmission systems, TIOHM[4:1] is set to logic 1 for each overhead bit position. TIOHM[4:1] is set to logic 0 if the transmission system contains no overhead bits. TIOHM[4:1] is sampled on the rising edge of TICLK[4:1].

Pin Name	Type	Pin No.	Function
TFPI[4] TFPI[3] TFPI[2] TFPI[1]	Input	W15 V12 V9 V6	Framer Transmit Frame Pulse/Multiframe Pulse (TFPI/TMFPI[4:1]). TFPI/TMFPI[4:1] is valid when the S/UNI-QJET is configured as a DS3, E3, or J2 framer for non-ATM applications by setting the FRMRONLY bit in the S/UNI-QJET Configuration 1 Register to logic 1. TFPI[4:1] indicates the position of all overhead bits in each DS3 M-subframe, the first bit in each G.751 E3 or G.832 E3 frame, or the first framing bit in each J2 frame. TFPI[4:1] is not required to pulse at every frame boundary in E3 or J2 modes.
TMFPI[4] TMFPI[3] TMFPI[2] TMFPI[1]			TMFPI[4:1] indicates the position of the first bit in each DS3 M-frame, the first bit in each E3 frame, or the first framing bit in each J2 multiframe. TMFPI[4:1] is not required to pulse at every multiframe boundary. TFPI/TMFPI[4:1] is sampled on the rising edge of TICLK[4:1].
TICLK[4] TICLK[3] TICLK[2] TICLK[1]	Input	V15 Y13 W9 W6	Transmit Input Clock (TICLK[4:1]). TICLK[4:1] provides the transmit direction timing. TICLK[4:1] is the externally generated transmission system baud rate clock. It is internally buffered to produce the transmit clock output, TCLK[4:1], and can be enabled to update the TPOS/TDATO[4:1] and TNEG/TOHM[4:1] outputs on the TICLK[4:1] rising edge. The TICLK[4:1] maximum frequency is 52 MHz.

Pin Name	Type	Pin No.	Function
ROHFP[4] ROHFP[3] ROHFP[2] ROHFP[1]	Output	J1 M2 P2 T2	Receive DS3/E3/J2 Overhead Frame Position (ROHFP[4:1]). ROHFP[4:1] locates the individual overhead bits in the received overhead data stream, ROH[4:1]. ROHFP[4:1] is high during the X1 overhead bit position in the ROH[4:1] stream when processing a DS3 stream. ROHFP[4:1] is high during the first bit of the FA1 byte when processing a G.832 E3 stream. ROHFP[4:1] is high during the RAI overhead bit position when processing a G.751 E3 stream. ROHFP[4:1] is high during the first bit in Timeslot 97 in the first frame of the 4-frame multiframe when processing a J2 stream. ROHFP[4:1] is updated on the falling edge of ROHCLK[4:1].
ROH[4] ROH[3] ROH[2] ROH[1]	Output	J2 L2 P1 T1	Receive DS3/E3/J2 Overhead Data (ROH[4:1]). ROH[4:1] contains the overhead bits (C, F, X, P, and M) extracted from the received DS3 stream; ROH[4:1] contains the overhead bytes (FA1, FA2, EM, TR, MA, NR, and GC) extracted from the received G.832 E3 stream; ROH[4:1] contains the overhead bits (RAI, National Use, Stuff Indication, and Stuff Opportunity) extracted from the received G.751 E3 stream; ROH[4:1] contains the overhead bits (Framing, X_{1-3}, A, M, E_{1-5}) extracted from the received J2 stream. ROH[4:1] is updated on the falling edge of ROHCLK[4:1].

Pin Name	Type	Pin No.	Function
ROHCLK[4] ROHCLK[3] ROHCLK[2] ROHCLK[1]	Output	K4 M3 N4 R4	Receive DS3/E3/J2 Overhead Clock (ROHCLK[4:1]). ROHCLK[4:1] is active when a DS3, E3, or J2 stream is being processed. ROHCLK[4:1] is nominally a 526 kHz clock when processing DS3, a 1.072 MHz clock when processing G.832 E3, a 1.074 MHz clock when processing G.751 E3, and a gapped 6.312 MHz clock with an average frequency of 168 kHz for J2. ROH[4:1], and ROHFP[4:1] are updated on the falling edge of ROHCLK[4:1].
REF8KO[4] REF8KO[3] REF8KO[2] REF8KO[1]	Output	U12 Y9 Y6 V4	Reference 8kHz Output (REF8KO[4:1]). REF8KO[4:1] is an 8kHz reference derived from the receive clocks on RCLK[4:1]. A free-running divide-down counter is used to generate REF8KO[4:1] so it will not glitch on reframe actions. REF8KO[4:1] will pulse high for approximately 1 RCLK[4:1] cycle every 125 µs. REF8KO[4:1] should be treated as a glitch-free asynchronous signal.
RPOHFP[4] RPOHFP[3] RPOHFP[2] RPOHFP[1]			Receive PLCP Overhead Frame Position (RPOHFP[4:1]). RPOHFP[4:1] locates the individual PLCP path overhead bits in the receive overhead data stream, RPOH[4:1]. RPOHFP[4:1] is logic 1 while bit 1 (the most significant bit) of the path user channel octet (F1) is present in the RPOH[4:1] stream. RPOHFP[4:1] is updated on the falling edge of RPOHCLK[4:1]. RPOHFP[4:1] is available when the PLCPEN register bit is logic 1 in the SPLR Configuration Register.

Pin Name	Type	Pin No.	Function
RFPO[4] RFPO[3] RFPO[2] RFPO[1] RMFPO[4] RMFPO[3] RMFPO[2] RMFPO[1]	Output	U12 Y9 Y6 V4	Framer Receive Frame Pulse/Multi-frame Pulse (RFPO/RMFPO[4:1]). RFPO/RMFPO[4:1] is valid when the S/UNI-QJET is configured to be in framer only mode. The 8KREFO bit must be set to logic 0 S/UNI-QJET Configuration Register. RFPO[4:1] is aligned to RDATO[4:1] and indicates the position of the first bit in each DS3 M-subframe, the first bit in each G.751 E3 or G.832 E3 frame, or the first framing bit in each J2 frame RMFPO[4:1] is aligned to RDATO[4:1] and indicates the position of the first bit in each DS3 M-frame, the first bit in each G.751 or G.832 E3 multiframe, or the first framing bit in each J2 multiframe. RFPO/RMFPO[4:1] is updated on either the falling or rising edge of RSCLK[4:1] depending on the setting of the RSCLKR bit in the S/UNI-QJET Receive Configuration register.
RPOH[4] RPOH[3] RPOH[2] RPOH[1]	Output	V13 V10 U8 W4	Receive PLCP Overhead Data (RPOH[4:1]). RPOH[4:1] contains the PLCP path overhead octets (Zn, F1, B1, G1, M1, M2, and C1) extracted from the received PLCP frame when the PLCP layer is in-frame. When the PLCP layer is in the loss of frame state, RPOH[4:1] is forced to all ones. The octet data on RPOH[4:1] is shifted out in order from the most significant bit (bit 1) to the least significant bit (bit 8). RPOH[4:1] is updated on the falling edge of RPOHCLK[4:1].

Pin Name	Type	Pin No.	Function
ROVRHD[4] ROVRHD[3] ROVRHD[2] ROVRHD[1]	Output	V13 V10 U8 W4	Framer Receive Overhead Indication (ROVRHD[4:1]). ROVRHD[4:1] is valid when the S/UNI-QJET is configured as a DS3, E3, or J2 framer for non-ATM applications by setting the FRMRONLY bit in the S/UNI-QJET Configuration 1 Registers. ROVRHD[4:1] will be high whenever the data on RDATO[4:1] corresponds to an overhead bit position. ROVRHD[4:1] is updated on the either the falling or rising edge of RSCLK[4:1] depending on the setting of the RSCLKR bit in the S/UNI-QJET Receive Configuration register.
RPOHCLK[4] RPOHCLK[3] RPOHCLK[2] RPOHCLK[1]	Output	W13 U10 V7 U5	Receive PLCP Overhead Clock (RPOHCLK[4:1]). RPOHCLK[4:1] is active when PLCP processing is enabled. The frequency of this signal depends on the selected PLCP format. RPOHCLK[4:1] is nominally a 26.7 kHz clock for a DS1 PLCP frame, a 768 kHz clock for a DS3 PLCP frame, a 33.7 kHz clock for an E1 based PLCP frame, or a 576 kHz clock for a G.751 E3 based PLCP frame. RPOHFP[4:1] and RPOH[4:1] are updated on the falling edge of RPOHCLK[4:1].
RSCLK[4] RSCLK[3] RSCLK[2] RSCLK[1]			Framer Recovered Clock (RSCLK[4:1]). RSCLK[4:1] is valid when the S/UNI-QJET is configured as a DS3, E3, or J2 framer for non-ATM applications by setting the FRMRONLY bit in the S/UNI-QJET Configuration Register. RSCLK[4:1] is the recovered clock and timing reference for RDATO[4:1], RFPO/RMFPO[4:1], and ROVRHD[4:1].

Pin Name	Type	Pin No.	Function
RGAPCLK[4] RGAPCLK[3] RGAPCLK[2] RGAPCLK[1]	Output	W13 U10 V7 U5	Framer Recovered Gapped Clock (RGAPCLK[4:1]). RGAPCLK[4:1] is valid when the S/UNI-QJET is configured as a DS3, E3, or J2 framer for non-ATM applications by setting the FRMRONLY bit in the S/UNI-QJET Configuration 1 Register and the RXGAPEN bit in the S/UNI-QJET Configuration 2 Register. RGAPCLK[4:1] is the recovered clock and timing reference for RDATO[4:1]. RGAPCLK[4:1] is held high for bit positions which correspond to overhead.
LCD[4] LCD[3] LCD[2] LCD[1]	Output	Y14 W10 W7 Y4	Loss of Cell Delineation (LCD[4:1]). LCD[4:1] is an active high signal which is asserted while the ATM cell processor has detected a Loss of Cell Delineation defect. The FRMRONLY bit in the S/UNI-QJET Configuration 1 Register must be set to logic 0 for LCD[4:1] to be valid.
RDATO[4] RDATO[3] RDATO[2] RDATO[1]			Framer Receive Data (RDATO[4:1]). RDATO[4:1] is valid when the S/UNI-QJET is configured as a DS3, E3, or J2 framer for non-ATM applications by setting the FRMRONLY bit in the S/UNI-QJET Configuration 1 Register. RDATO[4:1] is the received data aligned to RFPO/RMFPO[4:1] and ROVRHD[4:1]. RDATO[4:1] is updated on the active edge (as set by the RSCLKR register bit) of RSCLK[4:1] or RGAPCLK[4:1].

Pin Name	Type	Pin No.	Function
FRMSTAT[4] FRMSTAT[3] FRMSTAT[2] FRMSTAT[1]	Output	U1 U2 T4 U3	Framer Status (FRMSTAT[4:1]). FRMSTAT[4:1] is an active high signal which can be configured to show when one of the J2, E3, DS3, or PLCP framers have detected certain conditions. The FRMSTAT[4:1] outputs can be programmed via the STATSEL[2:0] bits in the S/UNI-QJET Configuration 2 Register to indicate: E3/DS3 Loss of Frame or J2 extended Loss of Frame, E3/DS3 Out of Frame or J2 Loss of Frame, PLCP Loss of Frame, PLCP Out of Frame, AIS, Loss of Signal, and DS3 Idle. FRMSTAT[4:1] should be treated as a glitch free asynchronous signal.
ATM8	Input	L18	ATM Interface Bus Width Selection (ATM8). The ATM8 input pin determines whether the S/UNI-QJET works with a 8-bit wide interface (RDAT[7:0] and TDAT[7:0]) or a 16-bit wide interface (RDAT[15:0] and TDAT[15:0]). If ATM8 is set to logic 1, then the 8-bit wide interface is chosen. If ATM8 is set to logic 0, then the 16-bit wide interface is chosen.

Pin Name	Type	Pin No.	Function
TDAT[15]	Input	C15	Transmit Cell Data Bus (TDAT[15:0]). This bus carries the ATM cell octets that are written to the selected transmit FIFO. TDAT[15:0] is sampled on the rising edge of TFCLK and is considered valid only when TENB is simultaneously asserted and the S/UNI-QJET has been selected via the TADR[4:2] and PHY_ADR[2:0] inputs. The S/UNI-QJET can be configured to operate with an 8-bit wide or 16-bit wide ATM data interface via the ATM8 input pin. When configured for the 8-bit wide interface, TDAT[15:8] are not used and should be tied to ground.
TDAT[14]		A16	
TDAT[13]		B16	
TDAT[12]		D15	
TDAT[11]		C16	
TDAT[10]		A17	
TDAT[9]		B17	
TDAT[8]		D16	
TDAT[7]		C17	
TDAT[6]		D18	
TDAT[5]		E17	
TDAT[4]		D19	
TDAT[3]		D20	
TDAT[2]		E18	
TDAT[1]		F17	
TDAT[0]		E19	

Pin Name	Type	Pin No.	Function
TPRTY	Input	G19	Transmit bus parity (TPRTY). The transmit parity (TPRTY) signal indicates the parity of the TDAT[15:0] or TDAT[7:0] bus. If configured for the 8-bit bus (via the ATM8 input pin), then parity is calculated over TDAT[7:0]. If configured for the 16-bit bus, then parity is calculated over TDAT[15:0]. A parity error is indicated by a status bit and a maskable interrupt. Cells with parity errors are inserted in the transmit stream, so the TPRTY input may be unused. Odd or even parity selection is made using the TPTYP register bit. TPRTY is sampled on the rising edge of TFCLK and is considered valid only when TENB is simultaneously asserted and the S/UNI-QJET has been selected via the TADR[4:0] and PHY_ADR[2:0] inputs.
TSOC	Input	G20	Transmit Start of Cell (TSOC). The transmit start of cell (TSOC) signal marks the start of cell on the TDAT bus. When TSOC is high, the first word of the cell structure is present on the TDAT bus. It is not necessary for TSOC to be present for each cell. An interrupt may be generated if TSOC is high during any word other than the first word of the cell structure. TSOC is sampled on the rising edge of TFCLK and is considered valid only when TENB is simultaneously asserted and the S/UNI-QJET has been selected via the TADR[4:2] and PHY_ADR[2:0] inputs.

Pin Name	Type	Pin No.	Function
TENB	Input	H18	Transmit Multi-Phy Write Enable (TENB). The TENB signal is an active low input which is used along with the TADR[4:0] inputs to initiate writes to the transmit FIFOs. When sampled low using the rising edge of TFCLK, the word on the TDAT bus is written into the transmit FIFO selected by the TADR[4:0] address bus. When sampled high using the rising edge of TFCLK, no write is performed, but the TADR[4:0] address is latched to identify the transmit FIFO to be accessed. A complete 53 octet cell must be written to the transmit FIFO before it is inserted into the transmit stream. Idle cells are inserted when a complete cell is not available.
TADR[4] TADR[3] TADR[2] TADR[1] TADR[0]	Input	F18 F19 F20 G18 H17	Transmit Address (TADR[4:0]). The TADR[4:0] bus is used to select the FIFO (and hence port) that is written to using the TENB signal and the FIFO whose cell-available signal is visible on the TCA output. TADR[4:0] is sampled on the rising edge of TFCLK together with TENB. Note that the null-PHY address 1FH is an invalid address and will not be identified to any port on the S/UNI-QJET.

Pin Name	Type	Pin No.	Function
TCA	Output	H19	Transmit Multi-Phy Cell Available (TCA). The TCA signal indicates when a cell is available in the transmit FIFO for the port selected by TADR[4:0]. When high, TCA indicates that the corresponding transmit FIFO is not full and a complete cell may be written. When TCA goes low, it can be configured to indicate either that the corresponding transmit FIFO is near full or that the corresponding transmit FIFO is full. TCA will transition low on the rising edge of TFCLK which samples Payload byte 43 (TCALEVEL0=0) or 47 (TCALEVEL0=1) for the 8-bit interface (ATM8=1), or the rising edge of TFCLK which samples Payload word 19 (TCALEVEL0=0) or 23 (TCALEVEL0=1) for the 16-bit interface (ATM8=0) if the PHY being polled is the same as the PHY in use. To reduce FIFO latency, the FIFO depth at which TCA indicates "full" can be set to one, two, three or four cells. Note that regardless of what fill level TCA is set to indicate "full" at, the transmit cell processor can store 4 complete cells. TCA is tri-stated when either the null-PHY address (1FH) or an address not matching the address space set by PHY_ADR[2:0] is latched (by TFCLK) from the TADR[4:2] inputs. The polarity of TCA (with respect the the description above) is inverted when the TCAINV register bit is set to logic 1.

Pin Name	Type	Pin No.	Function
TFCLK	Input	E20	Transmit FIFO Write Clock (TFCLK). This signal is used to write ATM cells to the four cell transmit FIFOs. TFCLK cycles at a 52 MHz or lower instantaneous rate. Please note that the TFCLK input is **not** 5 V tolerant, it is a 3.3 V only input pin.
DTCA[4] DTCA[3] DTCA[2] DTCA[1]	Output	J17 J18 J19 K19	Direct Access Transmit Cell Available (DTCA[4:1]). These output signals indicate when a cell is available in the transmit FIFO for the corresponding port. When high, DTCA[x] indicates that the corresponding transmit FIFO is not full and a complete cell may be written. DTCA[x] can be configured to indicate either that the corresponding transmit FIFO is near full and can accept no more than four writes or that the corresponding transmit FIFO is full. DTCA[x] will thus transition low on the rising edge of TFLCK which samples Payload byte 43 (TCALEVEL0=0) or 47 (TCALEVEL0=1) for the 8-bit interface (ATM8=1), or the rising edge of TFCLK which samples Payload word 19 (TCALEVEL0=0) or 23 (TCALEVEL0=1) for the 16-bit interface (ATM8=0). To reduce FIFO latency, the FIFO depth at which DTCA[x] indicates "full" can be set to one, two, three or four cells. Note that regardless of what fill level DTCA[x] is set to indicate "full" at, the transmit cell processor can store 4 complete cells. The polarity of DTCA[x] (with respect the the description above) is inverted when the TCAINV register bit is set to logic 1. The DTCA[4:1] outputs can be used to support Utopia Direct Access mode.

Pin Name	Type	Pin No.	Function
RDAT[15] RDAT[14] RDAT[13] RDAT[12] RDAT[11] RDAT[10] RDAT[9] RDAT[8] RDAT[7] RDAT[6] RDAT[5] RDAT[4] RDAT[3] RDAT[2] RDAT[1] RDAT[0]	Output	T20 T19 R17 T18 U20 U19 T17 U18 V17 U16 W17 Y17 V16 U15 W16 Y16	Receive Cell Data Bus (RDAT[15:0]). This bus carries the ATM cell octets that are read from the receive ATM FIFO selected by RADR[4:0]. RDAT[15:0] is tri-stated when RENB is high. RDAT[15:0] is updated on the rising edge of RFCLK. The S/UNI-QJET can be configured to operate with an 8-bit wide or 16-bit wide ATM data interface via the ATM8 input pin. RDAT[15:8] will remain tri-stated if ATM8 is set to logic 1. RDAT[15:0] is tri-stated when either the null-PHY address (1FH) or an address not matching the address space set by PHY_ADR[2:0] is latched from the RADR[4:2] inputs when RENB is high.
RPRTY	Output	R18	Receive Parity (RPRTY). The receive parity (RPRTY) signal indicates the parity of the RDAT bus. The S/UNI-QJET can be configured to operate with an 8-bit wide or 16-bit wide ATM data interface via the ATM8 input pin. In the 8-bit mode, RPRTY reflects the parity of RDAT[7:0]. In the 16-bit mode, RPRTY reflects the parity of RDAT[15:0]. Odd or even parity selection is made using the RXPTYP register bit. RPRTY is tri-stated when either the null-PHY address (1FH) or an address not matching the address space set by PHY_ADR[2:0] is latched from the RADR[4:2] inputs when RENB is high.

Pin Name	Type	Pin No.	Function
RSOC	Output	M17	Receive Start of Cell (RSOC). This signal marks the start of cell on the RDAT bus. RSOC marks the start of the cell on the RDAT bus. RSOC is tri-stated when either the null-PHY address (1FH) or an address not matching the address space set by PHY_ADR[2:0] is latched from the RADR[4:0] inputs when RENB is high.
RENB	Input	N18	Receive Multi-Phy Read Enable (RENB). The RENB signal is used to initiate reads from the receive FIFOs. When sampled low using the rising edge of RFCLK, a byte is read (if one is available) from the receive FIFO selected by the RADR[4:0] address bus and output on the RDAT bus. When sampled high using the rising edge of RFCLK, no read is performed and RDAT[15:0], RPRTY, and RSOC are tri-stated, and the address on RADR[4:0] is latched to select the device or port for the next ATM FIFO access. RENB must operate in conjunction with RFCLK to access the FIFOs at a high enough rate to prevent FIFO overflows. The ATM layer device may de-assert RENB at anytime it is unable to accept another byte.

Pin Name	Type	Pin No.	Function
RADR[4] RADR[3] RADR[2] RADR[1] RADR[0]	Input	P19 N17 P18 R20 R19	Receive Address (RADR[4:0]). The RADR[4:1] signal is used to select the FIFO (and hence port) that is read from using the RENB signal and the FIFO whose cell-available signal is visible on the RCA output. RADR[4:0] is sampled on the rising edge of RFCLK together with RENB. Note that the null-PHY address 1FH is an invalid address and will not be identified to any port on the S/UNI-QJET.
RCA	Output	N19	Receive Multi-Phy Cell Available (RCA). The RCA signal indicates when a cell is available in the receive FIFO for the port selected by RADR[4:0]. RCA can be configured to be de-asserted when either zero or four bytes remain in the selected/addressed FIFO. RCA will thus transition low on the rising edge of RFCLK after Payload byte 48 (RCALEVEL0=1) or 43 (RCALEVEL0=0) is output for the 8-bit interface (ATM8=1), or after Payload word 24 (RCALEVEL0=1) or 19 (RCALEVEL0=0) is output for the 16-bit interface (ATM8=0) if the PHY being polled is the same as the PHY in use. RCA is tri-stated when either the null-PHY address (1FH) or an address not matching the address space set by PHY_ADR[2:0] is latched (by RFCLK) from the RADR[4:2] inputs. The polarity of RCA (with respect to the description above) is inverted when the RCAINV register bit is set to logic 1.

Pin Name	Type	Pin No.	Function
RFCLK	Input	P20	Receive FIFO Read Clock (RFCLK). This signal is used to read ATM cells from the receive FIFOs. RFCLK must cycle at a 52 MHz or lower instantaneous rate, but at a high enough rate to avoid FIFO overflows. Please note that the RFCLK input is **not** 5 V tolerant, it is a 3.3 V only input pin.
DRCA[4] DRCA[3] DRCA[2] DRCA[1]	Output	L17 M20 M19 M18	Direct Access Receive Cell Available (DRCA[4:1]). These output signals indicate when a cell is available in the receive FIFO for the corresponding port. DRCA[4:1] can be configured to be de-asserted when either zero or four bytes remain in the FIFO. DRCA[4:1] will thus transition low on the rising edge of RFCLK after Payload byte 48 (RCALEVEL0=1) or 43 (RCALEVEL0=0) is output for the 8-bit interface (ATM8=1), or after Payload word 24 (RCALEVEL0=1) or 19 (RCALEVEL0=0) is output for the 16-bit interface (ATM8=0). The DRCA[4:1] outputs can be used to support Utopia Direct Access mode.
PHY_ADR[2] PHY_ADR[1] PHY_ADR[0]	Input	K18 L20 L19	Device Identification Address (PHY_ADR[2:0]). The PHY_ADR[2:0] inputs are the most-significant bits of the address space which this S/UNI-QJET occupies. When the PHY_ADR[2:0] inputs match the TADR[4:2] or RADR[4:2] inputs, then one of the four quadrants (as determined by the TADR[1:0] or RADR[1:0] inputs) in this S/UNI-QJET is selected for transmit or receive ATM access. Note that the null-PHY address 1FH is an invalid address and will not be identified to any port on the S/UNI-QJET.

Pin Name	Type	Pin No.	Function
CSB	Input	C9	Active low Chip Select (CSB). This signal must be low to enable S/UNI-QJET register accesses. If CSB is not used, (RDB and WRB determine register reads and writes) then it should be tied to an inverted version of RSTB.
WRB	Input	B8	Active low Write Strobe (WRB). This signal is pulsed low to enable a S/UNI-QJET register write access. The D[7:0] bus is clocked into the addressed register on the rising edge of WRB while CSB is low.
RDB	Input	D9	Active low Read Enable (RDB). This signal is pulsed low to enable a S/UNI-QJET register read access. The S/UNI-QJET drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are both low.
D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	I/O	D12 C13 A14 B14 D13 C14 A15 B15	Bi-directional Data Bus (D[7:0]). The bi-directional data bus D[7:0] is used during S/UNI-QJET register read and write accesses.

Pin Name	Type	Pin No.	Function
A[10] A[9] A[8] A[7] A[6] A[5] A[4] A[3] A[2] A[1] A[0]	Input	B9 B10 C10 A11 B11 C11 D11 A12 B12 C12 B13	Address Bus (A[10:0]). The address bus A[10:0] selects specific registers during S/UNI-QJET register accesses.
RSTB	Input	C8	Active low Reset (RSTB). This signal is set low to asynchronously reset the S/UNI-QJET. RSTB is a Schmitt-trigger input with an integral pull-up resistor.
ALE	Input	A8	Address Latch Enable (ALE). The address latch enable (ALE) is active-high and latches the address bus A[10:0] when low. When ALE is high, the internal address latches are transparent. It allows the S/UNI-QJET to interface to a multiplexed address/data bus. ALE has an integral pull-up resistor.
INTB	Output	A7	Active low Open-Drain Interrupt (INTB). This signal goes low when an unmasked interrupt event is detected on any of the internal interrupt sources. Note that INTB will remain low until all active, unmasked interrupt sources are acknowledged at their source.
TCK	Input	B6	Test Clock (TCK). This signal provides timing for test operations that can be carried out using the IEEE P1149.1 test access port.

Pin Name	Type	Pin No.	Function
TMS	Input	C7	Test Mode Select (TMS). This signal controls the test operations that can be carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull up resistor.
TDI	Input	D8	Test Data Input (TDI). This signal carries test data into the S/UNI-QJET via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull up resistor.
TDO	Output	B7	Test Data Output (TDO). This signal carries test data out of the S/UNI-QJET via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output which is inactive except when scanning of data is in progress.
TRSTB	Input	A6	Active low Test Reset (TRSTB). This signal provides an asynchronous S/UNI-QJET test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmitt triggered input with an integral pull up resistor. TRSTB must be asserted during the power up sequence. Note that if not used, TRSTB must be connected to the RSTB input.
BIAS	Input	H20 U17 D4 U4	+5V Bias (BIAS). When tied to +5V, the BIAS input is used to bias the wells in the input and I/O pads so that the pads can tolerate 5V on their inputs without forward biasing internal ESD protection devices. When tied to VDD, the inputs and bi-directional inputs will only tolerate input levels up to VDD.

Pin Name	Type	Pin No.	Function
VDD[1]	Power	B2	DC Power. The DC Power pins should be connected to a well-decoupled +3.3V DC supply.
VDD[2]		B3	
VDD[3]		B18	
VDD[4]		B19	
VDD[5]		C2	
VDD[6]		C3	
VDD[7]		C18	
VDD[8]		C19	
VDD[9]		D7	
VDD[10]		D10	
VDD[11]		D14	
VDD[12]		G4	
VDD[13]		G17	
VDD[14]		K17	
VDD[15]		L4	
VDD[16]		P4	
VDD[17]		P17	
VDD[18]		U7	
VDD[19]		U11	
VDD[20]		U14	
VDD[21]		V2	
VDD[22]		V3	
VDD[23]		V18	
VDD[24]		V19	
VDD[25]		W2	
VDD[26]		W3	
VDD[27]		W18	
VDD[28]		W19	

Pin Name	Type	Pin No.	Function
VSS[1]	Ground	A1	DC Ground. The DC Ground pins should be connected to GND.
VSS[2]		A2	
VSS[3]		A3	
VSS[4]		A9	
VSS[5]		A10	
VSS[6]		A13	
VSS[7]		A18	
VSS[8]		A19	
VSS[9]		A20	
VSS[10]		B1	
VSS[11]		B20	
VSS[12]		C1	
VSS[13]		C20	
VSS[14]		H1	
VSS[15]		J20	
VSS[16]		K20	
VSS[17]		L1	
VSS[18]		M1	
VSS[19]		N20	
VSS[20]		V1	
VSS[21]		V20	
VSS[22]		W1	
VSS[23]		W20	
VSS[24]		Y1	
VSS[25]		Y2	
VSS[26]		Y3	
VSS[27]		Y8	
VSS[28]		Y11	
VSS[29]		Y12	

Pin Name	Type	Pin No.	Function
VSS[30] VSS[31] VSS[32]	Ground	Y18 Y19 Y20	DC Ground. The DC Ground pins should be connected to GND.

Notes on Pin Description:

1. All S/UNI-QJET inputs and bi-directionals present minimum capacitive loading and operate at TTL logic levels.

2. All S/UNI-QJET outputs and bi-directionals have at least 3 mA drive capability. The data bus outputs, D[7:0], have 3 mA drive capability. The FIFO interface outputs, RDAT[15:0], RPRTY, RCA, DRCA[4:1], RSOC, TCA, and DTCA[4:1], have 12 mA drive capability. The outputs TCLK[4:1], TPOS/TDATO[4:1], TNEG/TOHM[4:1], TPOHFP/TFPO/TMFPO/TGAPCLK[4:1], LCD/RDATO[4:1], RPOH/ROVRHD[4:1], RPOHCLK/RSCLK/RGAPCLK[4:1], and REF8KO/RPOHFP/RFPO/RMFPO[4:1] have 6 mA drive capability. All other outputs have 3 mA drive capability.

3. Inputs RSTB, ALE, TMS, TDI and TRSTB have internal pull-up resistors.

4. RSTB, TRSTB, TMS, TDI, TCK, REF8KI, TFCLK, RFCLK, TICLK[4:1], and RCLK[4:1] are schmitt trigger input pads.

5. RFCLK and TFCLK are 3.3 V only input pins – they are **not** 5 V tolerant. Connecting a 5 V signal to these inputs may result in damage to the part.

6. The VSS [32:1] ground pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the S/UNI-QJET.

7. The VDD[28:1] power pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the device. These power supply connections must all be utilized and must all connect to a common +3.3 V or ground rail, as appropriate.

8. During power-up and power-down, the voltage on the BIAS pin must be kept equal to or greater than the voltage on the VDD [28:1] pins, to avoid damage to the device.

9 FUNCTIONAL DESCRIPTION

9.1 DS3 Framer

The DS3 Framer (T3-FRMR) Block integrates circuitry required for decoding a B3ZS-encoded signal and framing to the resulting DS3 bit stream. The T3-FRMR is directly compatible with the M23 and C-bit parity DS3 applications.

The T3-FRMR decodes a B3ZS-encoded signal and provides indications of line code violations. The B3ZS decoding algorithm and the LCV definition can be independently chosen through software. A loss of signal (LOS) defect is also detected for B3ZS encoded streams. LOS is declared when inputs RPOS and RNEG contain zeros for 175 consecutive RCLK cycles. LOS is removed when the ones density on RPOS and/or RNEG is greater than 33% for 175 ±1 RCLK cycles.

The framing algorithm examines five F-bit candidates simultaneously. When at least one discrepancy has occurred in each candidate, the algorithm examines the next set of five candidates. When a single F-bit candidate remains in a set, the first bit in the supposed M-subframe is examined for the M-frame alignment signal (i.e., the M-bits, M1, M2, and M3 are following the 010 pattern). Framing is declared, and out-of-frame is removed, if the M-bits are correct for three consecutive M-frames while no discrepancies have occurred in the F-bits. During the examination of the M-bits, the X-bits and P-bits are ignored. The algorithm gives a maximum average reframe time of 1.5 ms.

While the T3-FRMR is synchronized to the DS3 M-frame, the F-bit and M-bit positions in the DS3 stream are examined. An out-of-frame defect is detected when 3 F-bit errors out of 8 or 16 consecutive F-bits are observed (as selected by the M3O8 bit in the DS3 FRMR Configuration Register), or when one or more M-bit errors are detected in 3 out of 4 consecutive M-frames. The M-bit error criteria for OOF can be disabled by the MBDIS bit in the DS3 Framer Configuration register. The 3 out of 8 consecutive F-bits out-of-frame ratio provides more robust operation, in the presence of a high bit error rate, than the 3 out of 16 consecutive F-bits ratio. Either out-of-frame criteria allows an out-of-frame defect to be detected quickly when the M-subframe alignment patterns or, optionally, when the M-frame alignment pattern is lost.

Also while in-frame, line code violations, M-bit or F-bit framing bit errors, and P-bit parity errors are indicated. When C-bit parity mode is enabled, both C-bit parity errors and far end block errors are indicated. These error indications, as well as the line code violation and excessive zeros indication, are accumulated

over 1 second intervals with the Performance Monitor (PMON). Note that the framer is an off-line framer, indicating both OOF and COFA events. Even if an OOF is indicated, the framer will continue indicating performance monitoring information based on the previous frame alignment.

Three DS3 maintenance signals (a RED alarm condition, the alarm indication signal, and the idle signal) are detected by the T3-FRMR. The maintenance detection algorithm employs a simple integrator with a 1:1 slope that is based on the occurrence of "valid" M-frame intervals. For the RED alarm, an M-frame is said to be a "valid" interval if it contains a RED defect, defined as an occurrence of an OOF or LOS event during that M-frame. For AIS and IDLE, an M-frame interval is "valid" if it contains AIS or IDLE, defined as the occurrence of less than 15 discrepancies in the expected signal pattern (1010... for AIS, 1100... for IDLE) while valid frame alignment is maintained. This discrepancy threshold ensures the detection algorithms operate in the presence of a 10^{-3} bit error rate. For AIS, the expected pattern may be selected to be: the framed "1010" signal; the framed arbitrary DS3 signal and the C-bits all zero; the framed "1010" signal and the C-bits all zero; the framed all-ones signal (with overhead bits ignored); or the unframed all-ones signal (with overhead bits equal to ones). Each "valid" M-frame causes an associated integration counter to increment; "invalid" M-frames cause a decrement. With the "slow" detection option, RED, AIS, or IDLE are declared when the respective counter saturates at 127, which results in a detection time of 13.5 ms. With the "fast" detection option, RED, AIS, or IDLE are declared when the respective counter saturates at 21, which results in a detection time of 2.23 ms (i.e., 1.5 times the maximum average reframe time). RED, AIS, or IDLE are removed when the respective counter decrements to 0. DS3 Loss of Frame detection is provided as recommended by ITU-T G.783 with programmable integration periods of 1ms, 2ms, or 3ms. While integrating up to assert LOF, the counter will integrate up when the framer asserts an Out of Frame condition and integrates down when the framer de-asserts the Out of Frame condition. Once an LOF is asserted, the framer must not assert OOF for the entire integration period before LOF is de-asserted.

Valid X-bits are extracted by the T3-FRMR to provide indication of far end receive failure (FERF). A FERF defect is detected if the extracted X-bits are equal and are logic 0 (X1=X2=0); the defect is removed if the extracted X-bits are equal and are logic 1 (X1=X2=1). If the X-bits are not equal, the FERF status remains in its previous state. The extracted FERF status is buffered for 2 M-frames before being reported within the DS3 FRMR Status register. This buffer ensures a better than 99.99% chance of freezing the FERF status on a correct value during the occurrence of an out of frame.

When the C-bit parity application is enabled, both the far end alarm and control (FEAC) channel and the path maintenance data link are extracted. Codes in the FEAC channel are detected by the Bit Oriented Code Detector (RBOC). HDLC messages in the Path Maintenance Data Link are received by the Data Link Receiver (RDLC).

The T3-FRMR can be enabled to automatically assert the RAI indication in the outgoing transmit stream upon detection of any combination of LOS, OOF or RED, or AIS. The T3-FRMR can also be enabled to automatically insert C-bit Parity FEBE upon detection of receive C-bit parity error.

The T3-FRMR extracts the entire DS3 overhead (56 bits per M-frame) using the ROH output, along with the ROHCLK, and ROHFP outputs.

The T3-FRMR may be configured to generate interrupts on error events or status changes. All sources of interrupts can be masked or acknowledged via internal registers. Internal registers are also used to configure the T3-FRMR. Access to these registers is via a generic microprocessor bus.

9.2 E3 Framer

The E3 Framer (E3-FRMR) Block integrates circuitry required for decoding an HDB3-encoded signal and framing to the resulting E3 bit stream. The E3-FRMR is directly compatible with the G.751 and G.832 E3 applications.

The E3-FRMR searches for frame alignment in the incoming serial stream based on either the G.751 or G.832 formats. For the G.751 format, the E3-FRMR expects to see the selected framing pattern error-free for three consecutive frames before declaring INFRAME. For the G.832 format, the E3-FRMR expects to see the selected framing pattern error-free for two consecutive frames before declaring INFRAME. Once the frame alignment is established, the incoming data is continuously monitored for framing bit errors and byte interleaved parity errors (in G.832 format).

While in-frame, the E3-FRMR also extracts various overhead bytes and processes them according to the framing format selected:

In G.832 E3 format, the E3-FRMR extracts:

- the Trail Trace bytes and outputs them as a serial stream for further processing by the Trail Trace Buffer (TTB) block;

- the FERF bit and indicates an alarm when the FERF bit is a logic 1 for 3 or 5 consecutive frames. The FERF indication is removed when the FERF bit is a logic 0 for 3 or 5 consecutive frames;

- the FEBE bit and outputs it for accumulation in PMON;

- the Payload Type bits and buffers them so that they can be read by the microprocessor;

- the Timing Marker bit and asserts the Timing Marker indication when the value of the extracted bit has been in the same state for 3 or 5 consecutive frames;

- the Network Operator byte and presents it as a serial stream for further processing by the RDLC block when the RNETOP bit in the S/UNI-QJET Data Link and FERF Control register is logic 1. The byte is also brought out on the ROH[x] output with an associated clock on ROHCLK[x]. All 8 bits of the Network Operator byte are extracted and presented on the overhead output and, optionally, presented to the RDLC.

- the General Purpose Communication Channel byte and presents it to the RDLC when the RNETOP bit in the S/UNI-QJET Data Link and FERF Control register is logic 0 The byte is also brought out on the ROH[x] output with an associated clock on ROHCLK[x].

In G.751 E3 mode, the E3-FRMR extracts:

- the Remote Alarm Indication bit (bit 11 of the frame) and indicates a Remote Alarm when the RAI bit is a logic 1 for 3 or 5 consecutive frames. Similarly, the Remote Alarm is removed when the RAI bit is logic 0 for 3 or 5 consecutive frames;

- the National Use reserved bit (bit 12 of the frame) and presents it as a serial stream for further processing in the RDLC when the RNETOP bit in the S/UNI-QJET Data Link and FERF Control register is logic 0. The bit is also brought out on the ROH[x] output with an associated clock on ROHCLK[x]. Optionally, an interrupt can be generated when the National Use bit changes state.

Further, while in-frame, the E3-FRMR indicates the position of all the overhead bits in the incoming digital stream to the ATMF/SPLR block. For G.751 mode, the tributary justification bits can optionally be identified as either overhead or payload for payload mappings that take advantage of the full bandwidth.

The E3-FRMR declares out of frame alignment if the framing pattern is in error for four consecutive frames. The E3-FRMR is an "off-line" framer, where all frame alignment indications, all overhead bit indications, and all overhead bit processing continue based on the previous alignment. Once the framer has determined the new frame alignment, the out-of-frame indication is removed and a COFA indication is declared if the new alignment differs from the previous alignment.

The E3-FRMR detects the presence of AIS in the incoming data stream when less than 8 zeros in a frame are detected while the framer is OOF in G.832 mode, or when less than 5 zeros in a frame are detected while OOF in G.751 mode. This algorithm provides a probability of detecting AIS in the presence of a 10^{-3} BER as 92.9% in G.832 and 98.0% in G.751.

Loss of signal is LOS is declared when no marks have been received for 32 consecutive bit periods. Loss of signal is de-asserted after 32 bit periods during which there is no sequence of four consecutive zeros.

E3 Loss of Frame detection is provided as recommended by ITU-T G.783 with programmable integration periods of 1ms, 2ms, or 3ms. While integrating up to assert LOF, the counter will integrate up when the framer asserts an Out of Frame condition and integrates down when the framer de-asserts the Out of Frame condition. Once an LOF is asserted, the framer must not assert OOF for the entire integration period before LOF is de-asserted.

The E3-FRMR can also be enabled to automatically assert the RAI/FERF indication in the outgoing transmit stream upon detection of any combination of LOS, OOF or AIS. The E3-FRMR can also be enabled to automatically insert G.832 FEBE upon detection of receive BIP-8 errors.

9.3 J2 Framer

The J2-FRMR integrates circuitry to decode a unipolar or B8ZS encoded signal and frame to the resulting 6312 kbps J2 bit stream. Having found frame, the J2-FRMR extracts a variety of overhead and datalink information from the J2 bit stream.

The J2 format consists of 789-bit frames, each 125µs long, consisting of 96 bytes of payload, 2 reserved bytes, and 5 F-bits. The frames are grouped into 4-frame multiframes. The multiframe format is as follows:

Bit #	1-8	...	761-768	769-776	777-784	785	786	787	788	789
Frm. 1	TS1[1:8]	...	TS96[1:8]	TS97[1:8]	TS98[1:8]	1	1	0	0	m
Frm. 2	TS1[1:8]	...	TS96[1:8]	TS97[1:8]	TS98[1:8]	1	0	1	0	0
Frm. 3	TS1[1:8]	...	TS96[1:8]	TS97[1:8]	TS98[1:8]	x1	x2	x3	a	m
Frm. 4	TS1[1:8]	...	TS96[1:8]	TS97[1:8]	TS98[1:8]	e1	e2	e3	e4	e5

TS1 .. TS96 : Byte interleaved payload

TS97, TS98: Reserved channels for signaling

Frame Alignment Signal: represented as binary ones and zeroes

m : 4-kHz datalink

x1, x2, x3: Spare bits, usually logic 1

a : Remote Loss of Frame alarm bit, active high

e1..e5: CRC-5 check sequence. The entire 3156-bit multiframe, including

the CRC-5 check sequence, should have a remainder of 0 when

divided by $x^5 + x^4 + x^2 + 1$

The J2-FRMR frames to a J2 signal with an average reframe time of 5.07 ms. An alternate framing algorithm that uses the CRC-5 check to detect static mimic patterns is available. Once in frame, the J2-FRMR provides indications of frame and multiframe boundaries, and marks overhead bits, x-bits, m-bits, and reserved channels (TS97 and TS98). Indications of loss of signal, bipolar violations, excessive zeroes, change of frame alignment, framing errors, and CRC errors are provided, and may be accumulated by the PMON (with the exception of change of frame alignment); maskable interrupts are available to alert the microprocessor to the occurrence of any of these events. In addition to marking x-bit values, J2-FRMR provides microprocessor access to the x-bits, and will optionally generate an interrupt when any of the x-bits changes state. The m-bits and the associated clock are can either be extracted through the RDLC or through the ROH[x] and ROHCLK[x] output pins of the S/UNI-QJET. The m-bits are also presented to the RBOC for detection of any generic bit-oriented codes.

Status signals such as Physical AIS, Payload AIS, Remote Alarm Indication in

m-bits, and Remote Loss of Frame (a-bit) are detected by the J2-FRMR. In addition to providing indication signals of these states, the J2-FRMR will optionally generate an interrupt when any of these status signals changes.

J2 LOS is declared when no marks have been received for one of 15, 31, 63, or 255 consecutive bit periods. J2 LOS is cleared when either 15, 31, 63, or 255 consecutive bit periods have passed without an excessive zeros (8 or more consecutive zeros) detection as required by ITU-T G.775.

J2 LOF is declared when 7 or more consecutive multiframes with errored framing patterns are received. The J2 LOF is cleared when 3 or more consecutive multiframes with correct framing patterns are received. A framing algorithm which takes into account the CRC calculation is also available. The framing algorithms are described in the following text.

J2 Physical Layer AIS is declared when 2 or less zeros are detected in a sequence of 3156 bits. It is cleared when 3 or more zeros is detected in a sequence of 3156 bits as required by ITU-T G.775.

J2 Payload AIS is detected when the incoming J2 payload has 2 or less zeros in a sequence of 3072 bits. It is cleared when 3 or more zeros are detected in a sequence of 3072 bits.

The J2-FRMR may be forced to re-frame by microprocessor control. Similarly, the microprocessor may disable the J2-FRMR from reframing due to framing bit errors.

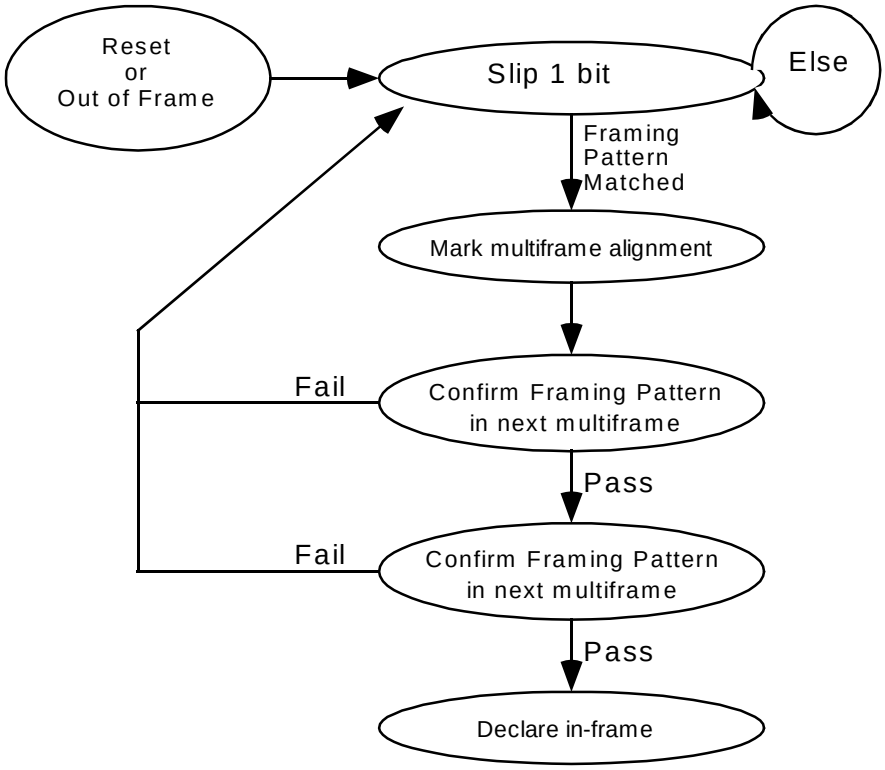
The J2-FRMR may be configured, and all sources of interrupts may be masked or acknowledged, via internal registers. These internal registers are accessed via a generic microprocessor bus.

9.3.1 J2 Frame Find Algorithms

The J2-FRMR searches for frame alignment using one of two algorithms, as selected by the CRC_REFR bit in the J2-FRMR Configuration Register.

When the CRC_REFR bit is set to logic 0, the J2-FRMR uses only the frame alignment sequence to find frame, searching for three consecutive correct frame alignment sequences. The frame find block searches for the entire 9-bit sequence (spread over two multiframes) at the same time, greatly reducing the time required to find frame alignment. The framing process with CRC-REFR cleared is illustrated in Figure 8.

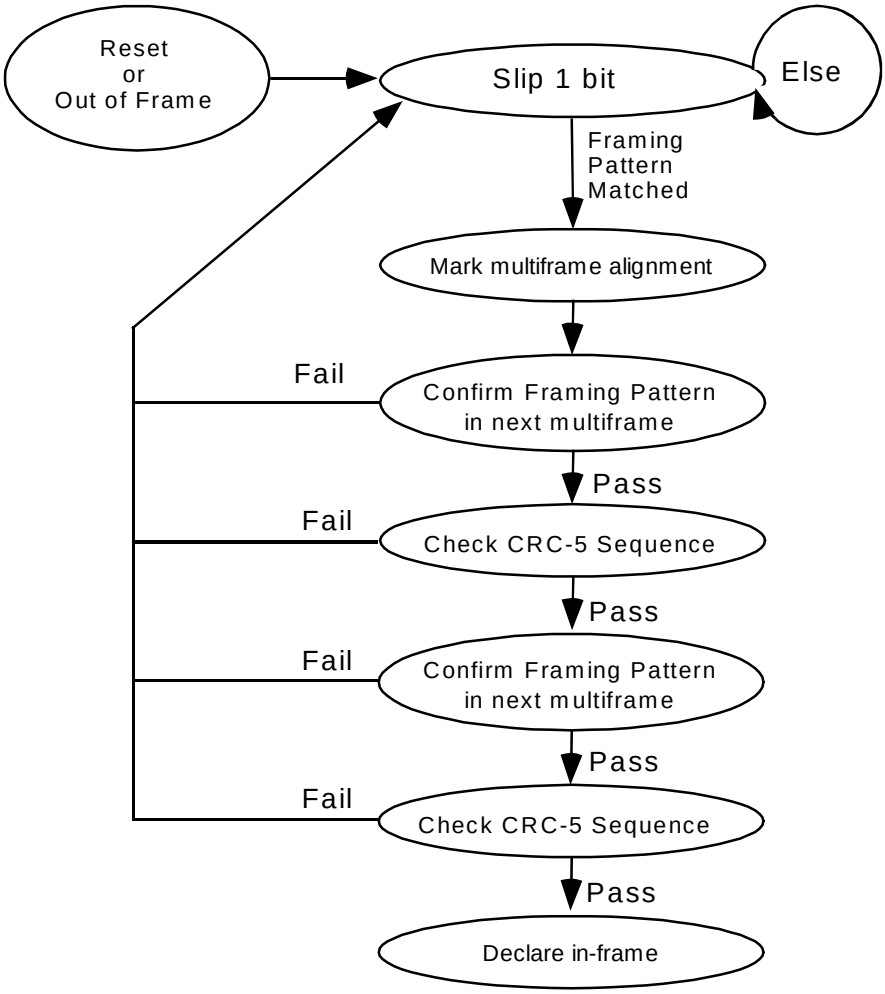
Figure 8 - Framing algorithm (CRC_REFR = 0)



Using this algorithm, the J2-FRMR will on average find frame in 5.07ms when starting the search in the worst possible position, given a 10^{-4} error rate and no static mimic patterns.

When the CRC_REFR bit is set to logic 1, in addition to requiring three consecutive correct framing patterns, the J2-FRMR requires that the first two CRC-5 checks be correct, or a reframe is initiated. To speed the process, the CRC-5 and frame alignment checks are run concurrently, as illustrated in Figure 9.

Figure 9 - Framing Algorithm (CRC_REFR = 1)



Using this algorithm, the J2-FRMR will find frame in 10.22ms, on average when starting the search in the worst possible position, given a 10^{-4} error rate and no static mimic patterns. The algorithm will reject 99.90% of mimic patterns. Further protection against mimic patterns is available by monitoring the rate of CRC-5 errors.

Once frame alignment is found, the block sets the LOF indication low, indicates a change of frame alignment (if it occurred). The block declares loss of frame alignment if 7 consecutive FASs have been received in error. In the presence of a random 10^{-3} bit error rate the frame loss criteria provides a mean time to falsely lose frame alignment of 1.65 years. The Frame Find Block can be forced to initiate a frame search at any time when the REFRAME bit in the J2-FRMR Configuration. Conversely, when the FLOCK bit is set to logic 1, the J2-FRMR

will never declare Loss of Frame or search for a new frame alignment due to excess framing bit errors.

J2 extended Loss of Frame detection is provided as recommended by ITU-T G.783 with programmable integration periods of 1ms, 2ms, or 3ms. While integrating up to assert LOF, the counter will integrate up when the framer asserts an Out of Frame condition and integrates down when the framer de-asserts the Out of Frame condition. Once an LOF is asserted, the framer must not assert OOF for the entire integration period before LOF is de-asserted.

9.4 PMON Performance Monitor Accumulator

The Performance Monitor (PMON) Block interfaces directly with either the DS3 Framer (T3-FRMR) to accumulate line code violation (LCV) events, parity error (PERR) events, path parity error (CPERR) events, far end block error (FEBE) events, excess zeros (EXZS), and framing bit error (FERR) events using saturating counters; the E3 Framer (E3-FRMR) to accumulate LCV, PERR (in G.832 mode), FEBE and FERR events; or the J2 Framer (J2-FRMR) to accumulate LCVs, CRC errors (in the PERR counter), Framing bit errors (FERR), and excess zeros (EXZS). The PMON stops accumulating error signal from the E3, DS3, or J2 Framers once frame synchronization is lost.

When an accumulation interval is signaled by a write to the PMON register address space or a write to the S/UNI-QJET Identification, Master Reset, and Global Monitor Update register, the PMON transfers the current counter values into microprocessor accessible holding registers and resets the counters to begin accumulating error events for the next interval. The counters are reset in such a manner that error events occurring during the reset period are not missed.

When counter data is transferred into the holding registers, an interrupt is generated, providing the interrupt is enabled. If the holding registers have not been read since the last interrupt, an overrun status bit is set. In addition, a register is provided to indicate changes in the PMON counters since the last accumulation interval.

9.5 RBOC Bit-Oriented Code Detector

The Bit-Oriented Code Detector is only used in DS3 C-bit Parity or J2 mode.

The Bit-Oriented Code Detector (RBOC) Block detects the presence of 63 of the 64 possible bit-oriented codes (BOCs) contained in the DS3 C-bit parity far-end alarm and control (FEAC) channel or in the J2 datalink signal stream. The 64th code ("111111") is similar to the HDLC flag sequence and is ignored.

Bit-oriented codes (BOCs) are received on the FEAC channel as 16-bit sequences each consisting of 8 ones, a zero, 6 code bits, and a trailing zero ("111111110xxxxxx0"). BOCs are validated when repeated at least 10 times. The RBOC can be enabled to declare a code valid if it has been observed for 8 out of 10 times or for 4 out of 5 times, as specified by the AVC bit in the RBOC Configuration/Interrupt Enable Register. The RBOC declares that the code is removed if two code sequences containing code values different from the detected code are received in a moving window of ten code periods.

Valid BOCs are indicated through the RBOC Interrupt Status Register. The BOC bits are set to all ones ("111111") when no valid code is detected. The RBOC can be programmed to generate an interrupt when a detected code has been validated and when the code is removed.

9.6 RDLC Facility Data Link Receiver

The RDLC is a microprocessor peripheral used to receive LAPD/HDLC frames on any serial HDLC bit stream that provides data and clock information such as the DS3 C-bit parity Path Maintenance Data Link, the E3 G.832 Network Requirement byte or the General Purpose data link (selectable using the RNETOP bit in the S/UNI-QJET Data Link and FERF/RAI Control register), the E3 G.751 Network Use bit, or the J2 m-bit Data Link.

The RDLC detects the change from flag characters to the first byte of data, removes stuffed zeros on the incoming data stream, receives packet data, and calculates the CRC-CCITT frame check sequence (FCS).

In the address matching mode, only those packets whose first data byte matches one of two programmable bytes or the universal address (all ones) are stored in the FIFO. The two least significant bits of the address comparison can be masked for LAPD SAPI matching.

Received data is placed into a 128-level FIFO buffer. An interrupt is generated when a programmable number of bytes are stored in the FIFO buffer. Other sources of interrupt are detection of the terminating flag sequence, abort sequence, or FIFO buffer overrun.

The Status Register contains bits which indicate the overrun or empty FIFO status, the interrupt status, and the occurrence of first flag or end of message bytes written into the FIFO. The Status Register also indicates the abort, flag, and end of message status of the data just read from the FIFO. On end of message, the Status Register indicates the FCS status and if the packet contained a non-integer number of bytes.

9.7 SPLR PLCP Layer Receiver

The PLCP Layer Receiver (SPLR) Block integrates circuitry to support DS1, DS3, E1, and G.751 E3 PLCP frame processing. The SPLR provides framing for PLCP based transmission formats.

The SPLR frames to DS1, DS3, E1, and G.751 E3 based PLCP frames with maximum average reframe times of 635 µs, 22 µs, 483 µs, and 32 µs respectively. Framing is declared (out of frame is removed) upon finding 2 valid, consecutive sets of framing (A1 and A2) octets and 2 valid and sequential path overhead identifier (POHID) octets. While framed, the A1, A2, and POHID octets are examined. OOF is declared when an error is detected in both the A1 and A2 octets or when 2 consecutive POHID octets are found in error. LOF is declared when an OOF state persists for more than 25 ms, 1 ms, 20 ms, or 1 ms for DS1, DS3, E1, or G.751 E3 PLCP formats respectively. If the OOF events are intermittent, the LOF counter is decremented at a rate 1/12 (DS3 PLCP), 1/10 (E1, DS1 PLCP) or 1/9(G.751 E3 PLCP) of the incrementing rate. LOF is thus removed when an in-frame state persists for more than 250 ms for a DS1 signal, 12 ms for a DS3 signal, 200 ms for an E1 signal, or 9 ms for a G.751 E3 signal. When LOF is declared, PLCP reframe is initiated.

When in frame, the SPLR extracts the path overhead octets and outputs them bit serially on output RPOH, along with the RPOHCLK and RPOHFP outputs. Framing octet errors and path overhead identifier octet errors are indicated as frame errors. Bit interleaved parity errors and far end block errors are indicated. The yellow signal bit is extracted and accumulated to indicate yellow alarms. Yellow alarm is declared when 10 consecutive yellow signal bits are set to logical 1; it is removed when 10 consecutive received yellow signal bits are set to logical 0. The C1 octet is examined to maintain nibble alignment with the incoming transmission system sublayer bit stream.

9.8 ATMF ATM Cell Delineator

The ATM Cell Delineator (ATMF) Block integrates circuitry to support HCS-based cell delineation for non-PLCP based transmission formats. The ATMF block accepts a bit serial cell stream from an upstream transmission system sublayer entity (such as the T3-FRMR, E3-FRMR, or J2-FRMR Block) and performs cell delineation to locate the cell boundaries. For PLCP applications, ATM cell positions are fixed relative to the PLCP frame, but the ATMF still performs cell delineation to locate the cell boundaries.

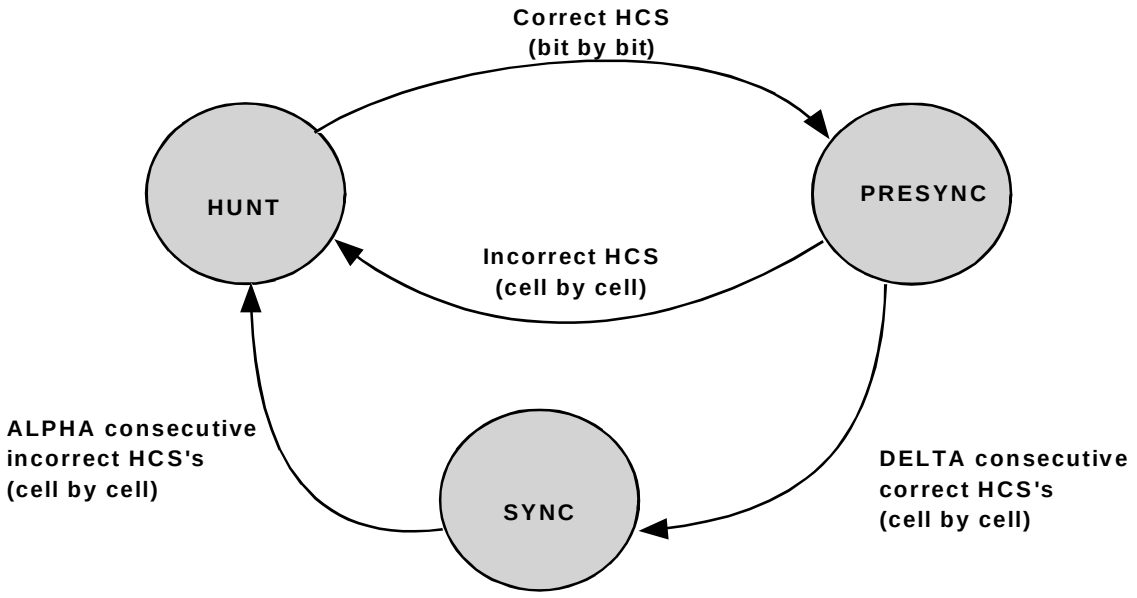
Cell delineation is the process of framing to ATM cell boundaries using the header check sequence (HCS) field found in the ATM cell header. The HCS is a

CRC-8 calculation over the first 4 octets of the ATM cell header. When performing delineation, correct HCS calculations are assumed to indicate cell boundaries.

The ATMF performs a sequential bit-by-bit, a nibble-by-nibble (DS-3 direct mapped), or a byte-by-byte (J2 and E3 direct-mapped) hunt for a correct HCS sequence. This state is referred to as the HUNT state. When receiving a bit serial cell stream from an upstream transmission system sublayer entity, the bit, nibble, or byte boundaries are determined from the location of the overhead.

When a correct HCS is found, the ATMF locks on the particular cell boundary and assumes the PRESYNC state. This state verifies that the previously detected HCS pattern was not a false indication. If the HCS pattern was a false indication then an incorrect HCS should be received within the next DELTA cells. At that point a transition back to the HUNT state is executed. If an incorrect HCS is not found in this PRESYNC period then a transition to the SYNC state is made. In this state synchronization is not relinquished until ALPHA consecutive incorrect HCS patterns are found. In such an event a transition is made back to the HUNT state. The state diagram of the cell delineation process is shown in Figure 10.

Figure 10 - Cell delineation State Diagram



The values of ALPHA and DELTA determine the robustness of the delineation method. ALPHA determines the robustness against false misalignments due to bit errors. DELTA determines the robustness against false delineation in the

synchronization process. ALPHA is chosen to be 7 and DELTA is chosen to be 6 as recommended in ITU-T Recommendation I.432. These values result in a maximum average time to frame of 127 µs for a DS3 stream carrying ATM cells directly mapped into the DS3 information payload.

Loss of cell delineation (LCD) is detected by counting the number of incorrect cells while in the HUNT state. The counter value is stored in the RXCP-50 LCD Count Threshold register. The threshold has a default value of 360 which results in a DS3 application detection time of 3.5 ms, an E3 G.832 application detection time of 4.5 ms, and E3 G.751 application detection time of 5.0 ms, a J2 application time of 24.8ms, an E1 application detection time of 77 ms, and a DS1 application detection time of 100 ms. If the counter value is set to zero, the LCD output signal is asserted for every incorrect cell.

9.9 RXCP-50 Receive Cell Processor

The Receive Cell Processor (RXCP-50) Block integrates circuitry to support scrambled or unscrambled cell payloads, scrambled or unscrambled cell headers, header check sequence (HCS) verification, idle cell filtering, and performance monitoring.

The RXCP-50 operates upon a delineated cell stream. For PLCP based transmissions systems, cell delineation is performed by the SPLR. For non-PLCP based transmission systems, cell delineation is performed by the ATMF. Framing status indications from these blocks ensure that cells are not written to the RXFF while the SPLR is in the loss of frame state, or cells are not written to the RXFF while the ATMF is in the HUNT or PRESYNC states.

The RXCP-50 descrambles the cell payload field using the self synchronizing descrambler with a polynomial of $x^{43} + 1$. The header portion of the cells can optionally be descrambled also. Note that cell payload scrambling is enabled by default in the S/UNI-QJET as required by ITU-T Recommendation I.432, but may be disabled to ensure backwards compatibility with older equipment.

The HCS is a CRC-8 calculation over the first 4 octets of the ATM cell header. The RXCP-50 verifies the received HCS using the accumulation polynomial, $x^8 + x^2 + x + 1$. The coset polynomial $x^6 + x^4 + x^2 + 1$ is added (modulo 2) to the received HCS octet before comparison with the calculated result as required by the ATM Forum UNI specification, and ITU-T Recommendation I.432.

The RXCP-50 can be programmed to drop all cells containing an HCS error or to filter cells based on the HCS and the cell header. Filtering according to a particular HCS and the GFC, PTI, and CLP bits of the ATM cell header (the VCI and VPI bits must be all logic 0) is programmable through the RXCP-50 registers.

More precisely, filtering is performed when filtering is enabled or when HCS errors are found when HCS checking is enabled. Otherwise, all cells are passed on regardless of any error conditions. Cells can be blocked if the HCS pattern is invalid or if the filtering 'Match Pattern' and 'Match Mask' registers are programmed with a certain blocking pattern. ATM Idle cells are filtered by default. For ATM cells, Null cells (Idle cells) are identified by the standardized header pattern of 'H00, 'H00, 'H00 and 'H01 in the first 4 octets followed by the valid HCS octet.

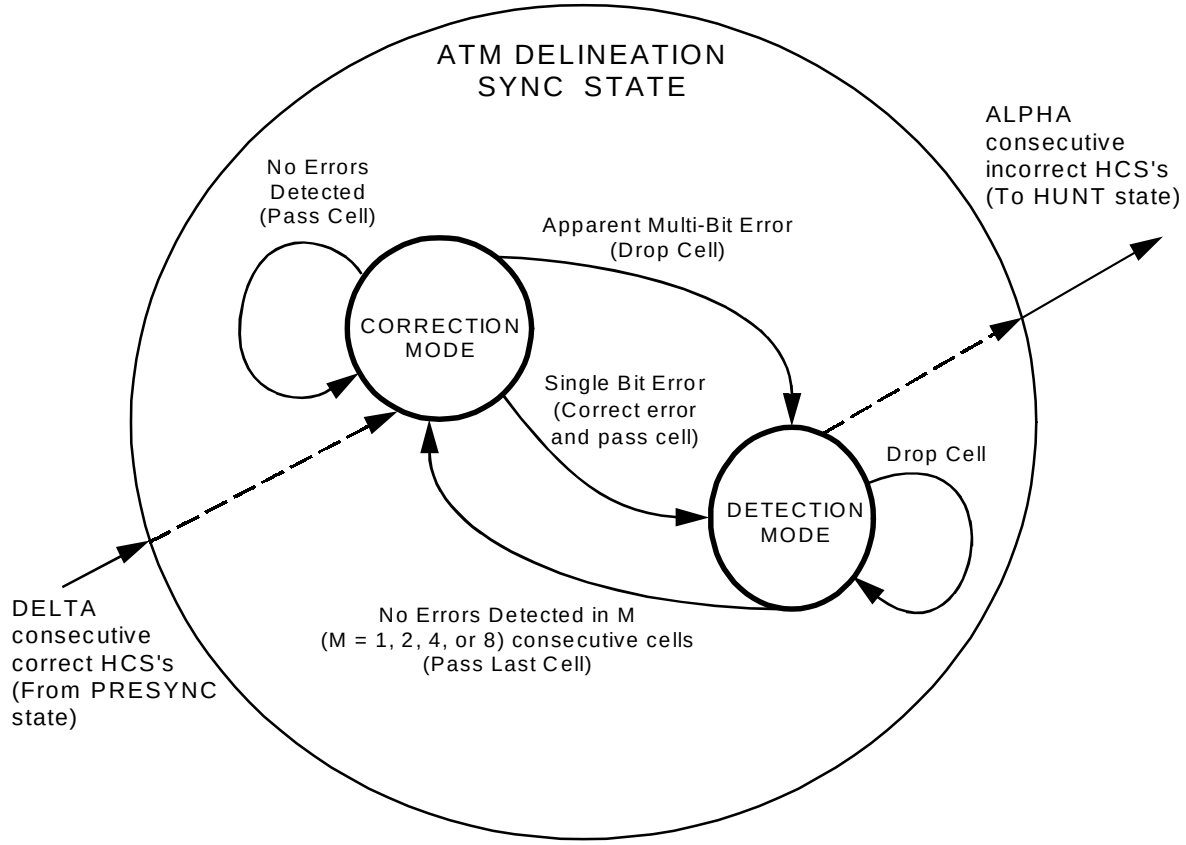
While the cell delineation state machine is in the SYNC state, the HCS verification circuit implements the state machine shown in Figure 11.

In normal operation, the HCS verification state machine remains in the 'Correction' state. Incoming cells containing no HCS errors are passed to the receive FIFO. Incoming single-bit errors are corrected, and the resulting cell is passed to the FIFO. Upon detection of a single-bit error or a multi-bit error, the state machine transitions to the 'Detection' state.

A programmable hysteresis is provided when dropping cells based on HCS errors. When a cell with an HCS error is detected, the RXCP-50 can be programmed to continue to discard cells until m (where m = 1, 2, 4, 8) cells are received with a correct HCS. The mth cell is not discarded (see Figure 11). Note that the dropping of cells due to HCS errors only occurs while the ATMF is in the SYNC state.

Cell delineation can optionally be disabled, allowing the RXCP-50 to pass all data bytes it receives.

Figure 11 - HCS Verification State Diagram



9.10 RXFF Receive FIFO

The Receive FIFO (RXFF) provides FIFO management and the S/UNI-QJET receive cell interface. The receive FIFO contains four cells. The FIFO provides the cell rate decoupling function between the transmission system physical layer and the ATM layer.

In general, the management functions include filling the receive FIFO, indicating when the receive FIFO contains cells, maintaining the receive FIFO read and write pointers, and detecting FIFO overrun and underrun conditions.

The FIFO interface is “UTOPIA Level 2" compliant and accepts a read clock (RFCLK) and read enable signal (RENB). The receive FIFO output bus (RDAT[15:0]) is tri-stated when RENB is logic 1 or if the PHY device address (RADR[4:0]) selected does not match this device's address. The interface indicates the start of a cell (RSOC) and the receive cell available status (RCA and DRCA[4:1]) when data is read from the receive FIFO (using the rising edges

of RFCLK). The RCA (and DRCA[x]) status changes from available to unavailable when the FIFO is either empty (RCALEVEL0=1) or near empty (RCALEVEL0 is logic 0). This interface also indicates FIFO overruns via a maskable interrupt and register bits. Read accesses while RCA (or DRCA[x]) is a logic 0 will output invalid data.

9.11 CPPM Cell and PLCP Performance Monitor

The Cell and PLCP Performance Monitor (CPPM) Block interfaces directly to the SPLR to accumulate bit interleaved parity error events, framing octet error events, and far end block error events in saturating counters. When the PLCP framer (SPLR) declares loss of frame, bit interleaved parity error events, framing octet error events, far end block error events, header check sequence error events are not counted.

When an accumulation interval is signaled by a write to the CPPM register address space or to the S/UNI-QJET Identification, Master Reset, and Global Monitor Update register, the CPPM transfers the current counter values into holding registers and resets the counters to begin accumulating error events for the next interval. The counters are reset in such a manner that error events occurring during the reset period are not missed.

9.12 PRGD Pseudo-Random Sequence Generator/Detector

The Pseudo-Random Sequence Generator/Detector (PRGD) block is a software programmable test pattern generator, receiver, and analyzer. Two types of test patterns (pseudo-random and repetitive) conform to ITU-T O.151.

The PRGD can be programmed to generate any pseudo-random pattern with length up to 2^{32}-1 bits or any user programmable bit pattern from 1 to 32 bits in length. In addition, the PRGD can insert single bit errors or a bit error rate between 10^{-1} to 10^{-7}.

The PRGD can be programmed to check for the presence of the generated pseudo-random pattern. The PRGD can perform an auto-synchronization to the expected pattern, and generate interrupts on detection and loss of the specified pattern. The PRGD can accumulate the total number of bits received and the total number of bit errors in two saturating 32-bit counters. The counters accumulate over an interval defined by writes to the S/UNI-QJET Identification/Master Reset, and Global Monitor Update register (register 006H) or by writes to any PRGD accumulation register. When an accumulation is forced by either method, then the holding registers are updated, and the counters reset to begin accumulating for the next interval. The counters are reset in such a way

that no events are missed. The data is then available in the holding registers until the next accumulation. In addition to the two counters, a record of the 32 bits received immediately prior to the accumulation is available.

The PRGD may also be programmed to check for repetitive sequences. When configured to detect a pattern of length N bits, the PRGD will load N bits from the detected stream, and determine whether the received pattern repeats itself every N subsequent bits. Should it fail to find such a pattern, it will continue loading and checking until it finds a repetitive pattern. All the features (error counting, auto-synchronization, etc.) available for pseudo-random sequences are also available for repetitive sequences. Whenever a PRGD accumulation is forced, the PRGD stores a snapshot of the 32 bits received immediately prior to the accumulation. This snapshot may be examined in order to determine the exact nature of the repetitive pattern received by PRGD.

The pseudo-random or repetitive pattern can be inserted/extracted in the PLCP payload (if PLCP framing is enabled) or in the DS3, E3, J2, or Arbitrary framing format payload (if PLCP framing is disabled). It cannot be inserted into the ATM cell payload.

9.13 DS3 Transmitter

The DS3 Transmitter (T3-TRAN) Block integrates circuitry required to insert the overhead bits into a DS3 bit stream and produce a B3ZS-encoded signal. The T3-TRAN is directly compatible with the M23 and C-bit parity DS3 formats.

Status signals such as far end receive failure (FERF), the alarm indication signal, and the idle signal can be inserted when their transmission is enabled by internal register bits. FERF can also be automatically inserted on detection of any combination of LOS, OOF or RED, or AIS by the T3-FRMR.

A valid pair of P-bits is automatically calculated and inserted by the T3-TRAN. When C-bit parity mode is selected, the path parity bits, and far end block error (FEBE) indications are automatically inserted.

When enabled for C-bit parity operation, the FEAC channel is sourced by the XBOC bit-oriented code transmitter. The path maintenance data link messages are sourced by the TDPR data link transmitter. These overhead signals can also be overwritten by using the TOH[x] and TOHINS[x] inputs.

When enabled for M23 operation, the C-bits are forced to logic 1 with the exception of the C-bit Parity ID bit (first C-bit of the first M-subframe), which is forced to toggle every M-frame.

The T3-TRAN supports diagnostic modes in which it inserts parity or path parity errors, F-bit framing errors, M-bit framing errors, invalid X or P-bits, line code violations, or all-zeros.

User control of each of the overhead bits in the DS3 frame is provided. Overhead bits may be inserted on a bit-by-bit basis from a user supplied data stream. An overhead clock (at 526 kHz) and a DS3 overhead alignment output are provided to allow for control of the user provided stream.

9.14 E3 Transmitter

The E3 Transmitter (E3-TRAN) Block integrates circuitry required to insert the overhead bits into an E3 bit stream and produce an HDB3-encoded signal. The E3-TRAN is directly compatible with the G.751 and G.832 framing formats.

The E3-TRAN generates the frame alignment signal and inserts it into the incoming serial stream based on either the G.751 or G.832 formats and an alignment pulse applied to it by the SPLT block. All overhead and status bits in each frame format can be individually controlled by register bits or by the transmit overhead stream. While in certain framing format modes, the E3-TRAN generates various overhead bytes according to the following:

In G.832 E3 format, the E3-TRAN:

- inserts the BIP-8 byte calculated over the preceding frame;
- inserts the Trail Trace bytes through the Trail Trace Buffer (TTB) block;
- inserts the FERF bit via a register bit or, optionally, when the E3-FRMR declares OOF, or when the loss of cell delineation (LCD) defect is declared;
- inserts the FEBE bit, which is set to logic 1 when one or more BIP-8 errors are detected by the receive framer. If there are no BIP-8 errors indicated by the E3-FRMR, the E3-TRAN sets the FEBE bit to logic 0;
- inserts the Payload Type bits based on the register value set by the microprocessor;
- inserts the Tributary Unit multiframe indicator bits either via the TOH overhead stream or by register bit values set by the microprocessor;
- inserts the Timing Marker bit via a register bit;

- inserts the Network Operator (NR) byte from the TDPR block when the TNETOP bit in the S/UNI-QJET Data Link and FERF Control register is logic 1; otherwise, the NR byte is set to all ones. The NR byte can be overwritten by using the TOH[x] and TOHINS[x] input pins. All 8 bits of the Network Operator byte are available for use as a datalink;

- inserts the General Purpose Communication Channel (GC) byte from the TDPR block when the TNETOP bit in the S/UNI-QJET Data Link and FERF Control register is logic 0; otherwise, the byte is set to all ones. The GC byte can be overwritten by using the TOH[x] and TOHINS[x] input pins.

In G.751 E3 mode, the E3-TRAN :

- inserts the Remote Alarm Indication bit (bit 11 of the frame) either via a register bit or, optionally, when the E3-FRMR declares OOF;

- inserts the National Use reserved bit (bit 12 of the frame) either as a fixed value through a register bit or from the TDPR block as configured by the TNETOP bit in the S/UNI-QJET Data Link and FERF Control register and the NATUSE bit in the E3 TRAN Configuration register;

- optionally identifies the tributary justification bits and stuff opportunity bits as either overhead or payload to SPLT for payload mappings that take advantage of the full bandwidth.

Further, the E3-TRAN can provide insertion of bit errors in the framing pattern or in the parity bits, and insertion of single line code violations for diagnostic purposes. Most of the overhead bits can be overwritten by using the TOH[x] and TOHINS[x] input pins.

9.15 J2 Transmitter

The J2 Transmitter (J2-TRAN) Block integrates circuitry required to insert the overhead bits into an J2 bit stream and produce a B8ZS-encoded signal. The J2-TRAN is directly compatible with the framing format specified in G.704 and NTT Technical Reference for High-Speed Digital Leased Circuit Services.

The J2-TRAN generates the frame alignment signal and inserts it into the incoming serial stream. All overhead and status bits in each frame format can be individually controlled by either register bits or by the transmit overhead stream.

The J2-TRAN:

- inserts the CRC-5 bits calculated over the preceding multiframe;
- inserts the x-bits through microprocessor programmable register bits;
- inserts the a-bit through a microprocessor programmable register bit;
- inserts the m-bit data link through the TDPR block;
- inserts payload AIS or physical layer AIS through microprocessor programmable register bits;
- inserts RAI over the m-bits, overwriting HDLC frames, by using the XBOC block or through automatic activation upon detection of certain remote alarm conditions.

The J2-TRAN allows overwriting of any of the overhead bits by using the TOH[x], TOHINS[x], TOHFP[x], and TOHCLK[x] overhead signals. Further, the J2-TRAN can provide insertion of single bit errors in the framing pattern or in the CRC-5 bits, and insertion of single line code violations for diagnostic purposes.

9.16 XBOC Bit Oriented Code Generator

The Bit Oriented Code Generator (XBOC) Block transmits 63 of the possible 64 bit oriented codes (BOC) in the C-bit parity Far End Alarm and Control (FEAC) channel. A BOC is a 16-bit sequence consisting of 8 ones, a zero, 6 code bits, and a trailing zero (111111110xxxxxx0) which is repeated as long as the code is not 111111. The code to be transmitted is programmed by writing the XBOC Code Register. The 64th code (111111) is similar to the HDLC idle sequence and is used to disable the transmission of any bit oriented codes. When transmission is disabled, the FEAC channel is set to all ones.

9.17 TDPR Facility Data Link Transmitter

The Facility Data Link Transmitter (TDPR) provides a serial data link for the C-bit parity path maintenance data link in DS3, the serial Network Operator byte or the General Purpose datalink in G.832 E3, the National Use bit datalink in G.751 E3, or the m-bit datalink in J2. The TDPR is used under microprocessor control to transmit HDLC data frames. It performs all of the data serialization, CRC generation, zero-bit stuffing, as well as flag, and abort sequence insertion. Upon completion of the message, a CRC-CCITT frame check sequence (FCS) can be

appended, followed by flags. If the TDPR transmit data FIFO underflows, an abort sequence is automatically transmitted.

When enabled, the TDPR continuously transmits flags (01111110) until data is ready to be transmitted. Data bytes to be transmitted are written into the TDPR Transmit Data Register. The TDPR automatically begins transmission of data once at least one complete packet is written into its FIFO. All complete packets of data will be transmitted if no error condition occurs. After the last data byte of a packet, the CRC FCS (if CRC insertion has been enabled) and a flag, or just a flag (if CRC insertion has not been enabled) is transmitted. The TDPR then returns to the transmission of flag characters until the next packet is available for transmission. The TDPR will also force transmission of the FIFO data once the FIFO depth has surpassed the programmable upper limit threshold. Transmission commences regardless of whether or not a packet has been completely written into the FIFO. The user must be careful to avoid overfilling the FIFO. Underruns can only occur if the packet length is greater than the programmed upper limit threshold because, in such a case, transmission will begin before a complete packet is stored in the FIFO.

An interrupt can be generated once the FIFO depth has fallen below a user configured lower threshold as an indicator for the user to write more data. Interrupts can also be generated if the FIFO underflows while transmitting a packet, when the FIFO is full, or if the FIFO is overrun.

If there are more than five consecutive ones in the raw transmit data or in the CRC data, a zero is stuffed into the serial data output. This prevents the unintentional transmission of flag or abort sequences.

Abort sequences (01111111 sequence where the 0 is transmitted first) can be continuously transmitted at any time by setting a control bit. During packet transmission, an underrun situation can occur if data is not written to the TDPR Transmit Data register before the previous byte has been depleted. In this case, an abort sequence is transmitted, and the controlling processor is notified via the UDR register bit. An abort sequence will also be transmitted if the user overflows the FIFO with a packet of length greater than 128 bytes. Overflows where other complete packets are still stored in the FIFO will not generate an abort. Only the packet which caused the overflow is corrupted and an interrupt is generated to the user via the OVR register bit. The other packets remain unaffected.

When the TDPR is disabled, a logical 1 (Idle) is inserted in the path maintenance data link.

9.18 SPLT SMDS PLCP Layer Transmitter

The SMDS PLCP Layer Transmitter (SPLT) Block integrates circuitry to support DS1, DS3, E1, and G.751 E3 based PLCP frame insertion.

The SPLT automatically inserts the framing (A1, A2) and path overhead identification (POHID) octets and provides registers or automatic generation of the F1, B1, G1, M2, M1 and C1 octets.

Registers are provided for the path user channel octet (F1) and the path status octet (G1). The bit interleaved parity octet (B1) and the FEBE subfield are automatically inserted.

The DQDB management information octets, M1 and M2 are generated. The type 0 and type 1 patterns described in TA-TSY-000772 are automatically inserted. The type 1 page counter may be reset using a register bit in the SPLT Configuration register. Note that this feature is not required for the ATM Forum compliant DS3 UNI. For this application, the M1 and M2 octets must be set to all zeros.

The PLCP transmit frame C1 cycle/stuff counter octet and the transmit stuffing pattern can be referenced to the REF8KI input pin. Alternately, a fixed stuffing pattern may be inserted into the C1 cycle/stuff counter octet. A looped timing operating mode is provided where the transmit PLCP timing is derived from the received timing. In this mode, the C1 stuffing is generated based on the received stuffing pattern as determined by the SPLR block. When DS1 or E1 PLCP format is enabled, the pattern 00H is inserted.

When DS3 PLCP format is enabled, the C1 octet indicates the phase of the 375 µs nibble stuffing opportunity cycle. During frame one of the three frame cycle, the pattern FFH is inserted in the C1 octet, indicating a 13 nibble trailer length. During frame two, the pattern 00H is inserted, indicating a 14 nibble trailer length. During frame three, the pattern 66H or 99H is inserted, indicating a 13 or 14 nibble trailer length respectively.

When configured for G.751 E3 PLCP frame format, the C1 octet is used to indicate the number of octets stuffed in the trailer. The following table shows the C1 octet pattern for each of the possible octet stuff lengths:

Stuff Length	C1(Hex)
17	3B

Stuff Length	C1(Hex)
18	4F
19	75
20	9D
21	A7

The SPLT block generates a stuff length pattern of 18, 19 or 20 octets determined by the phase alignment of the start of the G.751 E3 frame and the start of the E3 PLCP frame. The REF8KI input is provisioned to loop time the PLCP transmit frame to an externally applied 8 kHz reference.

The Zn, growth octets are set to 00H. The Zn octets may be inserted from an external device via the path overhead stream input, TPOH.

9.19 TXCP-50 Transmit Cell Processor

The Transmit Cell Processor (TXCP-50) Block integrates circuitry to support ATM cell payload scrambling, header check sequence (HCS) generation, and idle/unassigned cell generation.

The TXCP-50 scrambles the cell payload field using the self synchronizing scrambler with polynomial $x^{43} + 1$. The header portion of the cells may optionally also be scrambled. Note that cell payload scrambling may be disabled in the S/UNI-QJET, though it is required by ITU-T Recommendation I.432. The ATM Forum DS3 UNI specification requires that cell payloads are scrambled for the DS3 physical layer interface. However, to ensure backwards compatibility with older equipment, the payload scrambling may be disabled.

The HCS is generated using the polynomial, $x^8 + x^2 + x + 1$. The coset polynomial $x^6 + x^4 + x^2 + 1$ is added (modulo 2) to the calculated HCS octet as required by the ATM Forum UNI specification, and ITU-T Recommendation I.432. The resultant octet optionally overwrites the HCS octet in the transmit cell. When the transmit FIFO is empty, the TXCP-50 inserts idle/unassigned cells. The idle/unassigned cell header is fully programmable using five internal registers. Similarly, the 48 octet information field is programmed with an 8 bit repeating pattern using an internal register.

9.20 TXFF Transmit FIFO

The Transmit FIFO (TXFF) provides FIFO management and the S/UNI-QJET transmit cell interface. The transmit FIFO contains four cells. The FIFO depth may be programmed to four, three, two, or one cells. The FIFO provides the cell rate decoupling function between the transmission system physical layer and the ATM layer.

In general, the management functions include emptying cells from the transmit FIFO, indicating when the transmit FIFO is full, maintaining the transmit FIFO read and write pointers and detecting a FIFO overrun condition.

The FIFO interface is “UTOPIA Level 2” compliant and accepts a write clock (TFCLK), a write enable signal (TENB), the start of a cell (TSOC) indication, and the parity bit (TPRTY), and the ATM device address (TADR[4:0]) when data is written to the transmit FIFO (using the rising edges of TFCLK). The interface provides the transmit cell available status (TCA and DTCA[4:1]) which can transition from "available" to "unavailable" when the transmit FIFO is near full (when TCALEVEL0 is logic 0) or when the FIFO is full (when TCALEVEL0 is logic 1) and can accept no more writes. To reduce FIFO latency, the FIFO depth at which TCA and DTCA[x] indicates "full" can be set to one, two, three or four cells by the FIFODP[1:0] bits of TXCP-50 Configuration 2 register. If the programmed depth is less than four, more than one cell may be written after TCA or DTCA[x] is asserted as the TXCP-50 still allows four cells to be stored in its FIFO. This interface also indicates FIFO overruns via a maskable interrupt and register bit, but write accesses while TCA or DTCA[x] is logic 0 are not processed. The TXFF automatically transmits idle cells until a full cell is available to be transmitted.

9.21 TTB Trail Trace Buffer

The Trail Trace Buffer (TTB) extracts and sources the trail trace message carried in the TR byte of the G.832 E3 stream. The message is used by the OS to prevent delivery of traffic from the wrong source and is 16 bytes in length. The 16-byte message is framed by the PTI Multiframe Alignment Signal (TMFAS = 'b10000000 00000000). One bit of the TMFAS is placed in the most significant bit of each message byte. In the receive direction, the trail trace message is extracted from the serial overhead stream output by the E3-FRMR. The extracted message is stored in the internal RAM for review by an external microprocessor. By default, the TTB will write the byte of a 16-byte message with its most significant bit set high to the first location in the RAM. The extracted trail trace message is checked for consistency between consecutive multiframes. A message received unchanged three or five times (programmable) is accepted for

comparison with the copy previously written into the internal RAM by the external microprocessor. Alarms are raised to indicate reception of unstable and mismatched messages. In the transmit direction, the TTB sources the trail trace message from the internal RAM for insertion into the TR byte by the E3-TRAN.

The TTB also extracts the Payload Type label carried in the MA byte of the G.832 E3 stream. The label is used to ensure that the adaptation function at the trail termination sink is compatible with the adaptation function at the trail termination source. The Payload Type label is check for consistency between consecutive multiframes. A Payload Type label received unchanged for five frames is accepted for comparison with the copy previously written into the TTB by the external microprocessor. Alarms are raised to indicate reception of unstable and mismatched Payload Type label bits.

9.22 JTAG Test Access Port

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The S/UNI-QJET identification code is 073460CD hexadecimal.

9.23 Microprocessor Interface

The microprocessor interface block provides normal and test mode registers, and the logic required to connect to the microprocessor interface. The normal mode registers are required for normal operation, and test mode registers are used to enhance the testability of the S/UNI-QJET. The register set is accessed as follows:

Table 2 - Register Memory Map

Address				Register
000H	100H	200H	300H	S/UNI-QJET Configuration 1
001H	101H	201H	301H	S/UNI-QJET Configuration 2
002H	102H	202H	302H	S/UNI-QJET Transmit Configuration
003H	103H	203H	303H	S/UNI-QJET Receive Configuration
004H	104H	204H	304H	S/UNI-QJET Data Link and FERF/RAI Control
005H	105H	205H	305H	S/UNI-QJET Interrupt Status

Address				Register
006H				S/UNI-QJET Identification, Master Reset, and Global Monitor Update
	106H	206H	306H	S/UNI-QJET Reserved
007H	107H	207H	307H	S/UNI-QJET Clock Activity Monitor and Interrupt Identification
008H	108H	208H	308H	SPLR Configuration
009H	109H	209H	309H	SPLR Interrupt Enable
00AH	10AH	20AH	30AH	SPLR Interrupt Status
00BH	10BH	20BH	30BH	SPLR Status
00CH	10CH	20CH	30CH	SPLT Configuration
00DH	10DH	20DH	30DH	SPLT Control
00EH	10EH	20EH	30EH	SPLT Diagnostics and G1 Octet
00FH	10FH	20FH	30FH	SPLT F1 Octet
010H	110H	210H	310H	PMON Change of PMON Performance Meters
011H	111H	211H	311H	PMON Interrupt Enable/Status
012H-013H	112H-113H	212H-213H	312H-313H	PMON Reserved
014H	114H	214H	314H	PMON Line Code Violation Event Count LSB
015H	115H	215H	315H	PMON Line Code Violation Event Count MSB
016H	116H	216H	316H	PMON Framing Bit Error Event Count LSB
017H	117H	217H	317H	PMON Framing Bit Error Event Count MSB
018H	118H	218H	318H	PMON Excessive Zeros Count LSB
019H	119H	219H	319H	PMON Excessive Zeros Count MSB
01AH	11AH	21AH	31AH	PMON Parity Error Event Count LSB
01BH	11BH	21BH	31BH	PMON Parity Error Event Count MSB

Address				Register
01CH	11CH	21CH	31CH	PMON Path Parity Error Event Count LSB
01DH	11DH	21DH	31DH	PMON Path Parity Error Event Count MSB
01EH	11EH	21EH	31EH	PMON FEBE/J2-EXZS Event Count LSB
01FH	11FH	21FH	31FH	PMON FEBE/J2-EXZS Event Count MSB
020H	120H	220H	320H	CPPM Reserved
021H	121H	221H	321H	CPPM Change of CPPM Performance Meter
022H	122H	222H	322H	CPPM BIP Error Count LSB
023H	123H	223H	323H	CPPM BIP Error Count MSB
024H	124H	224H	324H	CPPM PLCP Framing Error Event Count LSB
025H	125H	225H	325H	CPPM PLCP Framing Error Event Count MSB
026H	126H	226H	326H	CPPM PLCP FEBE Count LSB
027H	127H	227H	327H	CPPM PLCP FEBE Count MSB
028H-02FH	128H-12FH	228H-22FH	328H-32FH	CPPM Reserved
030H	130H	230H	330H	DS3 FRMR Configuration
031H	131H	231H	331H	DS3 FRMR Interrupt Enable
032H	132H	232H	332H	DS3 FRMR Interrupt Status
033H	133H	233H	333H	DS3 FRMR Status
034H	134H	234H	334H	DS3 TRAN Configuration
035H	135H	235H	335H	DS3 TRAN Diagnostics
036H-037H	136H-137H	236H-237H	336H-337H	DS3 TRAN Reserved
038H	138H	238H	338H	E3 FRMR Framing Options
039H	139H	239H	339H	E3 FRMR Maintenance Options

Address				Register
03AH	13AH	23AH	33AH	E3 FRMR Framing Interrupt Enable
03BH	13BH	23BH	33BH	E3 FRMR Framing Interrupt Indication and Status
03CH	13CH	23CH	33CH	E3 FRMR Maintenance Event Interrupt Enable
03DH	13DH	23DH	33DH	E3 FRMR Maintenance Event Interrupt Indication
03EH	13EH	23EH	33EH	E3 FRMR Maintenance Event Status
03FH	13FH	23FH	33FH	E3 FRMR Reserved
040H	140H	240H	340H	E3 TRAN Framing Options
041H	141H	241H	341H	E3 TRAN Status and Diagnostic Options
042H	142H	242H	342H	E3 TRAN BIP-8 Error Mask
043H	143H	243H	343H	E3 TRAN Maintenance and Adaptation Options
044H	144H	244H	344H	J2 FRMR Configuration
045H	145H	245H	345H	J2 FRMR Status
046H	146H	246H	346H	J2 FRMR Alarm Interrupt Enable
047H	147H	247H	347H	J2 FRMR Alarm Interrupt Status
048H	148H	248H	348H	J2 FRMR Error/X-bit Interrupt Enable
049H	149H	249H	349H	J2 FRMR Error/X-bit Interrupt Status
04AH-04BH	14AH-14BH	24AH-24BH	34AH-34BH	J2 FRMR Reserved
04CH	14CH	24CH	34CH	J2 TRAN Configuration
04DH	14DH	24DH	34DH	J2 TRAN Diagnostics
04EH	14EH	24EH	34EH	J2 TRAN TS97 Signaling
04FH	14FH	24FH	34FH	J2 TRAN TS98 Signaling
050H	150H	250H	350H	RDLC Configuration
051H	151H	251H	351H	RDLC Interrupt Control
052H	152H	252H	352H	RDLC Status

Address				Register
053H	153H	253H	353H	RDLC Data
054H	154H	254H	354H	RDLC Primary Address Match
055H	155H	255H	355H	RDLC Secondary Address Match
056H	156H	256H	356H	RDLC Reserved
057H	157H	257H	357H	RDLC Reserved
058H	158H	258H	358H	TDPR Configuration
059H	159H	259H	359H	TDPR Upper Transmit Threshold
05AH	15AH	25AH	35AH	TDPR Lower Interrupt Threshold
05BH	15BH	25BH	35BH	TDPR Interrupt Enable
05CH	15CH	25CH	35CH	TDPR Interrupt Status/UDR Clear
05DH	15DH	25DH	35DH	TDPR Transmit Data
05EH-05FH	15EH-15FH	25EH-25FH	35EH-35FH	TDPR Reserved
060H	160H	260H	360H	RXCP-50 Configuration 1
061H	161H	261H	361H	RXCP-50 Configuration 2
062H	162H	262H	362H	RXCP-50 FIFO/UTOPIA Control & Config
063H	163H	263H	363H	RXCP-50 Interrupt Enables and Counter Status
064H	164H	264H	364H	RXCP-50 Status/Interrupt Status
065H	165H	265H	365H	RXCP-50 LCD Count Threshold (MSB)
066H	166H	266H	366H	RXCP-50 LCD Count Threshold (LSB)
067H	167H	267H	367H	RXCP-50 Idle Cell Header Pattern
068H	168H	268H	368H	RXCP-50 Idle Cell Header Mask
069H	169H	269H	369H	RXCP-50 Corrected HCS Error Count
06AH	16AH	26AH	36AH	RXCP-50 Uncorrected HCS Error Count
06BH	16BH	26BH	36BH	RXCP-50 Received Cell Count LSB
06CH	16CH	26CH	36CH	RXCP-50 Received Cell Count
06DH	16DH	26DH	36DH	RXCP-50 Received Cell Count MSB

Address				Register
06EH	16EH	26EH	36EH	RXCP-50 Idle Cell Count LSB
06FH	16FH	26FH	36FH	RXCP-50 Idle Cell Count
070H	170H	270H	370H	RXCP-50 Idle Cell Count MSB
071H-07FH	171H-17FH	271H-27FH	371H-37FH	RXCP-50 Reserved
080H	180H	280H	380H	TXCP-50 Configuration 1
081H	181H	281H	381H	TXCP-50 Configuration 2
082H	182H	282H	382H	TXCP-50 Transmit Cell Status
083H	183H	283H	383H	TXCP-50 Interrupt Enable/Status
084H	184H	284H	384H	TXCP-50 Idle Cell Header Control
085H	185H	285H	385H	TXCP-50 Idle Cell Payload Control
086H	186H	286H	386H	TXCP-50 Transmit Cell Counter LSB
087H	187H	287H	387H	TXCP-50 Transmit Cell Counter
088H	188H	288H	388H	TXCP-50 Transmit Cell Counter MSB
089H-08FH	189H-18FH	289H-28FH	389H-38FH	TXCP-50 Reserved
090H	180H	290H	390H	TTB Control Register
091H	181H	291H	391H	TTB Trail Trace Identifier Status
092H	182H	292H	392H	TTB Indirect Address Register
093H	183H	293H	393H	TTB Indirect Data Register
094H	184H	294H	394H	TTB Expected Payload Type Label Register
095H	195H	295H	395H	TTB Payload Type Label Control/Status
096H-097H	196H-197H	296H-297H	396H-397H	TTB Reserved
098H	198H	298H	398H	RBOC Configuration/Interrupt Enable
099H	199H	299H	399H	RBOC Status
09AH	19AH	29AH	39AH	XBOC Code
09BH	19BH	29BH	39BH	S/UNI-QJET Misc.

Address				Register
09CH	19CH	29CH	39CH	S/UNI-QJET FRMR LOF Status.
0A0H	1A0H	2A0H	3A0H	PRGD Control
0A1H	1A1H	2A1H	3A1H	PRGD Interrupt Enable/Status
0A2H	1A2H	2A2H	3A2H	PRGD Length
0A3H	1A3H	2A3H	3A3H	PRGD Tap
0A4H	1A4H	2A4H	3A4H	PRGD Error Insertion
0A5H-0A7H	1A5H-1A7H	2A5H-2A7H	3A5H-3A7H	PRGD Reserved
0A8H	1A8H	2A8H	3A8H	PRGD Pattern Insertion Register #1
0A9H	1A9H	2A9H	3A9H	PRGD Pattern Insertion Register #2
0AAH	1AAH	2AAH	3AAH	PRGD Pattern Insertion Register #3
0ABH	1ABH	2ABH	3ABH	PRGD Pattern Insertion Register #4
0ACH	1ACH	2ACH	3ACH	PRGD Pattern Detector Register #1
0ADH	1ADH	2ADH	3ADH	PRGD Pattern Detector Register #2
0AEH	1AEH	2AEH	3AEH	PRGD Pattern Detector Register #3
0AFH	1AFH	2AFH	3AFH	PRGD Pattern Detector Register #4
0B0H-0FFH	1B0H-1FFH	2B0H-2FFH	3B0H-3FFH	S/UNI-QJET Reserved
400H				S/UNI-QJET Master Test Register
401H - 7FFH				Reserved for S/UNI-QJET Test

For all register accesses, CSB must be low.

10 NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the S/UNI-QJET. Normal mode registers (as opposed to test mode registers) are selected when A[10] is low.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the S/UNI-QJET to determine the programming state of the block.

3. Writable normal mode register bits are cleared to logic zero upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect S/UNI-QJET operation unless otherwise noted.

5. Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the S/UNI-QJET operates as intended, reserved register bits must only be written with the suggested logic levels. Similarly, writing to reserved registers should be avoided.

6. The S/UNI-QJET requires a software initialization sequence in order to guarantee proper device operation and long term reliability. Please refer to Section 12.1 of this document for the details on how to program this sequence.

Register 000H, 100H, 200H, 300H: S/UNI-QJET Configuration 1

Bit	Type	Function	Default
Bit 7	R/W	8KREFO	1
Bit 6	R/W	DS27_53	1
Bit 5	R/W	TOCTA	0
Bit 4	R/W	FRMRONLY	0
Bit 3	R/W	LOOPT	0
Bit 2	R/W	LLOOP	0
Bit 1	R/W	DLOOP	0
Bit 0	R/W	PLOOP	0

PLOOP:

The PLOOP bit controls the DS3, E3, or J2 payload loopback. When a logic 0 is written to PLOOP, DS3, E3, or J2 payload loopback is disabled. When a logic 1 is written to PLOOP, the DS3, E3, or J2 overhead bits are regenerated and inserted into the received DS3, E3, or J2 stream and the resulting stream is transmitted. Setting the PLOOP bit disables the effect of the TICLK bit in the S/UNI-QJET Transmit Configuration register, thereby forcing flow-through timing. The TFRM[1:0] and RFRM[1:0] bits in the S/UNI-QJET Transmit Configuration and Receive Configuration registers, respectively, must be set to the same value for PLOOP to work properly.

DLOOP:

The DLOOP bit controls the diagnostic loopback. When a logic 0 is written to DLOOP, diagnostic loopback is disabled. When a logic 1 is written to DLOOP, the transmit data stream is looped in the receive direction. The TFRM[1:0] and RFRM[1:0] bits in the S/UNI-QJET Transmit Configuration and Receive Configuration registers, respectively, must be set to the same value for DLOOP to work properly. The DLOOP should not be set to a logic 1 when either the PLOOP, LLOOP, or LOOPT bit is a logic 1. When in DS3, E3, or J2 modes, the TUNI register bit in the S/UNI-QJET Transmit Configuration register should be set to the same value as the UNI bit in the DS3, E3, or J2 FRMR registers.

LLOOP:

The LLOOP bit controls the line loopback. When a logic 0 is written to LLOOP, line loopback is disabled. When a logic 1 is written to LLOOP, the stream received on RPOS/RDATI and RNEG/RLCV/ROHM is looped to the TPOS/TDATO and TNEG/TOHM outputs. Note that the TPOS, TNEG, and TCLK outputs are referenced to RCLK when LLOOP is logic 1.

LOOPT:

The LOOPT bit selects the transmit timing source. When a logic 1 is written to LOOPT, the transmitter is loop-timed to the receiver. When loop timing is enabled, the receive clock (RCLK) is used as the transmit timing source. The transmit nibble stuffing is derived from the nibble stuffing in the receive PLCP frame (for DS3 or E3 PLCP frame transmission). The FIXSTUFF bit must be set to logic 0 if the LOOPT bit is set to logic 1. When a logic 0 is written to LOOPT, the transmit clock (TICLK) is used as the transmit timing source. The nibble stuffing is derived from the REF8KI input, or is fixed internally (as determined by the FIXSTUFF bit in the SPLT Configuration Register (for DS3 or E3 PLCP frame transmission only). Setting the LOOPT bit disables the effect of the TICLK and TXREF bits in the S/UNI-QJET Transmit Configuration and S/UNI-QJET Configuration 2 registers respectively, thereby forcing flow-through timing.

FRMRONLY:

The FRMRONLY bit controls whether the S/UNI-QJET is operating solely as a DS3, E3, or J2 framer/transmitter. If FRMRONLY is set to logic 1, the PLCP, and ATM blocks are disabled and the RDATO, REF8KO/RFPO/RMFPO, RSCLK, ROVRHD, TFPO/TMFPO, TFPI/TMFPI, and TDATI I/O pins are enabled. The ATM interface inputs are ignored and the outputs are tri-stated. If FRMRONLY is set to logic 0, the PLCP and ATM blocks are enabled and the LCD, RPOH, RPOHCLK, RPOHFP, TPOH, TIOHM, and TPOHFP I/O pins are enabled and the ATM interface inputs and outputs are enabled.

TOCTA:

The TOCTA bit enables octet-alignment or nibble-alignment of the transmit cell stream to the transmission overhead when the arbitrary transmission format is chosen (TFRM[1:0] = 11 binary and SPLT Configuration register bit EXT = 1). This bit has no effect when DS3, G.751 E3, G.832 E3, J2, T1, or E1 formats are selected since octet or nibble alignment is specified for these formats. When the arbitrary transmission format is chosen and TOCTA is set to logic 1, the ATM cell nibbles or octets are aligned to the arbitrary transmission format overhead boundaries (as set by the TIOHM input). Nibble alignment is chosen if the FORM[1:0] bits in the SPLT Configuration

are set to 00. Byte alignment is chosen if these FORM[1:0] bits are set to any other value. The number of TICLK periods between transmission format overhead bit positions must be divisible by 4 (for nibble alignment) or 8 (for byte alignment). When TOCTA is set to logic 0, no octet alignment is performed , and there is no restriction on the number of TICLK periods between transmission format overhead bit positions.

DS27_53:

The DS27_53 bit is used to select between the long data structure (27 words in 16-bit mode and 53 bytes in 8-bit mode) and the short data structure (26 words in 16-bit mode and 52 bytes in 8-bit mode) on the ATM interface. When DS27_53 is set to logic one, the RXCP-50 and TXCP-50 blocks are configured to operate with the long data structure; when DS27_53 is set to logic zero, the RXCP-50 and TXCP-50 are configured to operate with the short data structure.

8KREFO:

The 8KREFO bit is used, in conjunction with the PLCPEN bit in the SPLR Configuration Register to select the function of the REF8KO/RPOHFP/RFPO/RMFPO[x] output pin. When PLCPEN is logic 1, the RPOHFP function will be selected and 8KREFO has no effect (note that RPOHFP is inherently an 8kHz reference). If PLCPEN is logic 0, then if 8KREFO is logic 1, then an 8kHz reference will be derived from the RCLK[x] signal and output on REF8KO. If 8KREFO and PLCPEN are both logic 0, then the RXMFPO register bit in the S/UNI-QJET Configuration 2 register will select either the RFPO or RMFPO function.

Register 001H, 101H, 201H, 301H: S/UNI-QJET Configuration 2

Bit	Type	Function	Default
Bit 7	R/W	STATSEL[2]	0
Bit 6	R/W	STATSEL[1]	0
Bit 5	R/W	STATSEL[0]	0
Bit 4	R/W	TXMFPI	0
Bit 3	R/W	TXGAPEN	0
Bit 2	R/W	RXGAPEN	0
Bit 1	R/W	TXMFPO	0
Bit 0	R/W	RXMFPO	0

RXMFPO:

The RXMFPO bit controls which of the outputs RMFPO[4:1] or RFPO[4:1] is valid. If RXMFPO is a logic 1, then RMFPO[4:1] will be available. If RXMFPO is a logic 0, then RFPO[4:1] will be available. This bit has effect only if the FRMRONLY bit in the S/UNI-QJET Configuration 1 register is a logic 1.

TXMFPO:

The TXMFPO bit controls which of the outputs TMFPO[4:1] or TFPO[4:1] is valid. If TXMFPO is a logic 1, then TMFPO[4:1] will be available. If TXMFPO is a logic 0, then TFPO[4:1] will be available. This bit has effect only if the FRMRONLY bit in the S/UNI-QJET Configuration 1 register is a logic 1. The TXGAPEN bit takes precedence over the TXMFPO bit.

RXGAPEN:

The RXGAPEN bit configures the S/UNI-QJET to enable the RGAPCLK[x] outputs. When RXGAPEN is a logic 1, then the RGAPCLK[x] output is enabled. When RXGAPEN is a logic 0, then the RSCLK[x] output is enabled. The FRMRONLY register bit must be a logic 1 for RXGAPEN to have effect.

TXGAPEN:

The TXGAPEN bit configures the S/UNI-QJET to enable the TGAPCLK[x] outputs. When TXGAPEN is a logic 1, the TGAPCLK[x] output is enabled. When TXGAPEN is a logic 0, then either the TFPO[x] or TMFPO[x] output is enabled, depending on the setting of the TXMFPO register bit. The FRMRONLY register bit must be a logic 1 for TXGAPEN to have effect.

TXMFPI:

The TXMFPI bit controls which of the inputs TMFPI[4:1] or TFPI[4:1] is valid. If TXMFPI is a logic 1, then TMFPI[4:1] will be expected. If TXMFPI is a logic 0, then TFPI[4:1] will be expected. This bit has effect only if the FRMRONLY bit in the S/UNI-QJET Configuration 1 register is a logic 1.

STATSEL[2:0]:

The STATSEL[2:0] bits are used to select the function of the FRMSTAT[4:1] output. The selection is shown in the following table:

Table 3 - STATSEL[2:0] Options

STATSEL[2:0]	FRMSTAT output pin indication function
000	E3/DS3 Loss of Frame or J2 extended Loss of Frame (integration periods are selected by the LOFINT[1:0] register bits in the S/UNI-QJET Receive Configuration Register)
001	PLCP Loss of Frame
010	E3/DS3 Out of Frame or J2 Loss of Frame
011	PLCP Out of Frame
100	Alarm Indication Signal (AIS)
101	Loss of Signal
110	DS3 Idle
111	Reserved

Register 002H, 102H, 202H, 302H: S/UNI-QJET Transmit Configuration

Bit	Type	Function	Default
Bit 7	R/W	TFRM[1]	0
Bit 6	R/W	TFRM[0]	0
Bit 5	R/W	TXREF	0
Bit 4	R/W	TICLK	0
Bit 3	R/W	TUNI	0
Bit 2	R/W	TCLKINV	0
Bit 1	R/W	TPOSINV	0
Bit 0	R/W	TNEGINV	0

TNEGINV:

The TNEGINV bit provides polarity control for outputs TNEG/TOHM. When a logic 0 is written to TNEGINV, the TNEG/TOHM output is not inverted. When a logic 1 is written to TNEGINV, the TNEG/TOHM output is inverted. The TNEGINV bit setting does not affect the loopback data in diagnostic loopback.

TPOSINV:

The TPOSINV bit provides polarity control for outputs TPOS/TDATO. When a logic 0 is written to TPOSINV , the TPOS/TDATO output is not inverted. When a logic 1 is written to TPOSINV , the TPOS/TDATO output is inverted. The TPOSINV bit setting does not affect the loopback data in diagnostic loopback.

TCLKINV:

The TCLKINV bit provides polarity control for output TCLK. When a logic 0 is written to TCLKINV, TCLK is not inverted and outputs TPOS/TDATO and TNEG/TOHM are updated on the falling edge of TCLK. When a logic 1 is written to TCLKINV, TCLK is inverted and outputs TPOS/TDATO and TNEG/TOHM are updated on the rising edge of TCLK.

TUNI:

The TUNI bit enables the S/UNI-QJET to transmit unipolar or bipolar DS3, E3, or J2 data streams. When a logic 1 is written to TUNI, the S/UNI-QJET transmits unipolar DS3, E3, or J2 data on TDATO. When TUNI is logic 1, the TOHM output indicates the start of the DS3 M-Frame (the X1 bit), the start of the E3 frame (bit 1 of the frame), or the first framing bit of the J2 multiframe.

When a logic 0 is written to TUNI, the S/UNI-QJET transmits B3ZS-encoded DS3 data, HDB3-encoded E3 data, or B8ZS-encoded J2 data on TPOS and TNEG. The TUNI bit has no effect if TFRM[1:0] is set to 11 binary as the output data is automatically configured for unipolar format.

TICLK:

The TICLK bit selects the transmit clock used to update the TPOS/TDATO and TNEG/TOHM outputs. When a logic 0 is written to TICLK, the buffered version of the input transmit clock, TCLK, is used to update TPOS/TDATO and TNEG/TOHM on the edge selected by the TCLKINV bit. When a logic 1 is written to TICLK, TPOS/TDATO and TNEG/TOHM are updated on the rising edge of TICLK, eliminating the flow-through TCLK signal. The TICLK bit has no effect if the LOOPT, LLOOP, or PLOOP bit is a logic 1.

TXREF:

The TXREF register bit determines if TICLK[1] and TIOHM/TFPI/TMFPI[1] should be used as the reference transmit clock and overhead/frame pulse, respectively, instead of TICLK[X] and TIOHM/TFPI/TMFPI[X]. If TXREF is set to a logic 1, then TICLK[1] and TIOHM/TFPI/TMFPI[1] will be used as the reference transmit clock and overhead/frame pulse, respectively. If TXREF is set to a logic 0, then TICLK[X] and TIOHM/TFPI/TMFPI[X] will be used as the reference transmit clock and overhead/frame pulse, respectively, for quadrant X. If loop-timing is enabled (LOOPT = 1), the TXREF bit has no effect on the corresponding quadrant. Note that when TXREF is set to logic 1, the unused TICLK[x] and TIOHM/TFPI/TMFPI[x] should be tied to power or ground, not left floating.

TFRM[1:0]:

The TFRM[1:0] bits determine the frame structure of the transmitted signal according to the following table:

Table 4 - TFRM[1:0] Transmit Frame Structure Configurations

TFRM[1:0]	Transmit Frame Structure
00	DS3 (C-bit parity or M23 depending on the setting of the CBIT bit in the DS3 TRAN Configuration register)
01	E3 (G.751 or G.832 depending on the setting of the FORMAT[1:0] bits in the E3 TRAN Framing Options register)
10	J2 (G.704 and NTT compliant framing format)

TFRM[1:0]	Transmit Frame Structure
11	DS1/E1/Arbitrary framing format - If the EXT bit in the SPLT Configuration register is a logic 0, then DS1 or E1 direct-mapped or PLCP framing is selected (via the PLCPEN and FORM[1:0] bits in the SPLT Configuration register) and TIOHM[x] should be tied low. If EXT is a logic 1, then the arbitrary framing format is selected and overhead positions are indicated by the TIOHM[x] input pin.

Register 003H, 103H, 203H, 303H: S/UNI-QJET Receive Configuration

Bit	Type	Function	Default
Bit 7	R/W	RFRM[1]	0
Bit 6	R/W	RFRM[0]	0
Bit 5	R/W	LOFINT[1]	0
Bit 4	R/W	LOFINT[0]	0
Bit 3	R/W	RSCLKR	0
Bit 2	R/W	RCLKINV	0
Bit 1	R/W	RPOSINV	0
Bit 0	R/W	RNEGINV	0

RNEGINV:

The RNEGINV bit provides polarity control for input RNEG/RLCV/ROHM. When a logic 0 is written to RNEGINV, the input RNEG/RLCV/ROHM is not inverted. When a logic 1 is written to RNEGINV, the input RNEG/RLCV/ROHM is inverted. The RNEGINV bit setting does not affect the loopback data in diagnostic loopback.

RPOSINV:

The RPOSINV bit provides polarity control for input RPOS/RDATI. When a logic 0 is written to RPOSINV , the input RPOS/RDATI is not inverted. When a logic 1 is written to RPOSINV , the input RPOS/RDATI is inverted. The RPOSINV bit setting does not affect the loopback data in diagnostic loopback.

RCLKINV:

The RCLKINV bit provides polarity control for input RCLK. When a logic 0 is written to RCLKINV, RCLK is not inverted and inputs RPOS/RDATI and RNEG/RLCV/ROHM are sampled on the rising edge of RCLK. When a logic 1 is written to RCLKINV, RCLK is inverted and inputs RPOS/RDATI and RNEG/RLCV/ROHM are sampled on the falling edge of RCLK.

RSCLKR:

The RSCLKR bit has effect only when the FRMRONLY bit in the S/UNI-QJET Configuration 1 register is set to logic 1. When RSCLKR is a logic 1, the RDATO, RFPO/RMFPO, and ROVRHD outputs are updated on the rising

edge of RSCLK. When RSCLKR is a logic 0, the RDATO, RFPO/RMFPO, and ROVRHD outputs are updated on the falling edge of RSCLK. If the RXGAPEN bit is a logic 1, then RSCLKR affects RGAPCLK in the same manner as it affects RSCLK.

LOFINT[1:0]

The LOFINT[1:0] bits determine the integration period used for asserting and de-asserting E3 and DS3 Loss of Frame or J2 extended Loss of Frame on the FRMLOF register bit of the S/UNI-QJET FRMR LOF Status register (x9CH) and on the FRMSTAT[4:1] output pins (if this function is enabled by the STATSEL[2:0] register bits of the S/UNI-QJET Configuration 2 Register). The integration times are selected as follows:

Table 5 - LOF[1:0] Integration Period Configuration

LOFINT[1:0]	Integration Period
00	3ms
01	2ms
10	1ms
11	Reserved

RFRM[1:0]:

The RFRM[1:0] bits determine the expected frame structure of the received signal according to the following table:

Table 6 - RFRM[1:0] Receive Frame Structure Configurations

RFRM[1:0]	Expected Receive Frame Structure
00	DS3 (C-bit parity or M23 depending on the setting of the CBE bit in the DS3 FRMR Configuration register)
01	E3 (G.751 or G.832 depending on the setting of the FORMAT[1:0] bits in the E3 FRMR Framing Options register)
10	J2 (G.704 and NTT compliant framing format)

RFRM[1:0]	Expected Receive Frame Structure
11	DS1/E1/Arbitrary framing format - when EXT in the SPLR Configuration register is a logic 0, then DS1 or E1 direct-mapped or PLCP framing is selected (via the PLCPEN and FORM[1:0] bits in the SPLR Configuration register) and the frame alignment is indicated by the ROHM[x] input pin. When EXT is a logic 1, then the arbitrary framing format is selected and overhead bit positions are indicated by the ROHM[x] input pin.

Register 004H, 104H, 204H, 304H: S/UNI-QJET Data Link and FERF/RAI Control

Bit	Type	Function	Default
Bit 7	R/W	LCDEN	1
Bit 6	R/W	AISEN	1
Bit 5	R/W	RBLEN	1
Bit 4	R/W	OOFEN	1
Bit 3	R/W	LOSEN	1
Bit 2	R/W	TNETOP	0
Bit 1	R/W	RNETOP	0
Bit 0	R/W	DLINV	0

DLINV:

The DLINV bit provides polarity control for the DS3 C-bit Parity path maintenance data link which is located in the 3 C-bits of M-subframe 5. When a logic 1 is written to DLINV, the path maintenance data link is inverted before being processed. The rationale behind this bit is as follows: currently ANSI standard T1.107 specifies that the C-bits (which carry the path maintenance data link) be set to all zeros while the AIS maintenance signal is transmitted. The data link is obviously inactive during AIS transmission, and ideally the HDLC idle sequence (all ones) should be transmitted. By inverting the data link, the all zeros C-bit pattern becomes an idle sequence and the data link is terminated gracefully. Although this inversion is currently not specified in ANSI T1.107a, this bit is provided to safe-guard the S/UNI-QJET in case the inversion is required in the future.

RNETOP:

The RNETOP bit enables the Network Operator Byte (NR) extracted from the G.832 E3 stream to be terminated by the internal HDLC receiver, RDLC. When RNETOP is logic 1, the NR byte is extracted from the G.832 stream and terminated by RDLC. When RNETOP is logic 0, the GC byte is extracted from the G.832 stream and terminated by RDLC. Both the NR byte and the GC byte are extracted and output on the ROH pin for external processing.

TNETOP:

The TNETOP bit enables the Network Operator Byte (NR) inserted in the G.832 E3 stream to be sourced by the internal HDLC transmitter, TDPR. When TNETOP is logic 1, the NR byte is inserted into the G.832 stream through the TDPR block; the GC byte of the G.832 E3 stream is sourced by through the TOH[x] and TOHINS[x] pins. If TOH[x] and TOHINS[x] are not active, then an all ones signal will be inserted into the GC byte. When TNETOP is logic 0, the GC byte is inserted into the G.832 stream through the TDPR block; the NR byte of the G.832 E3 stream is sourced by the TOH[x] and TOHINS[x] pins. If TOH[x] and TOHINS[x] are not active, then an all ones signal will be inserted into the NR byte.

For G.751 E3 streams, the National Use bit is sourced by the TDPR block if TNETOP and the NATUSE bit (from the E3 TRAN Configuration Register x41H) are both logic 0. If either TNETOP or NATUSE is logic 1, the National Use bit will be sourced from the NATUSE register bit in register x41H.

If the S/UNI-QJET is configured for DS3 or J2 operation, TNETOP has no effect. The DS3 C-bit Parity and J2 datalink is inserted into the DS3 or J2 stream through the internal HDLC transmitter TDPR.

The TOH[x] and TOHINS[x] input pins can be used to overwrite the values of these overhead bits in the transmit stream.

LOSEN:

The LOSEN bit enables the receive loss of signal indication to automatically generate a FERF indication in the transmit stream. This bit operates regardless of framer selected (DS3, E3, or J2). When LOSEN is logic 1, assertion of the LOS indication by the framer causes a FERF (RAI in G.751 or J2 mode) to be transmitted by TRAN for the duration of the LOS assertion. When LOSEN is logic 0, assertion of the LOS indication does not cause transmission of a FERF/RAI.
Note that for the RAI to be automatically transmitted when in J2 format, the FEAC[5:0] bits in the XBOC Code register must all be set to logic 1. If the XBOC FEAC code is to be transmitted in J2 mode, LOSEN, OOFEN, AISEN, and LCDEN should all be set to logic 0.

OOFEN:

The OOFEN bit enables the receive out of frame indication to automatically generate a FERF indication (RAI in G.751 or J2 mode) in the transmit stream. This bit operates when the E3 or J2 framer is selected or when the DS3 framer is selected and the RBLEN bit is logic 0. When OOFEN is logic 1, assertion of the OOF indication by the framer causes a FERF/RAI to be transmitted by TRAN for the duration of the OOF assertion. When OOFEN is

logic 0, assertion of the OOF indication does not cause transmission of a FERF/RAI.
Note that for the RAI to be automatically transmitted when in J2 format, the FEAC[5:0] bits in the XBOC Code register must all be set to logic 1. If the XBOC FEAC code is to be transmitted in J2 mode, LOSEN, OOFEN, AISEN, and LCDEN should all be set to logic 0.

RBLEN:

The RBLEN bit enables the receive **R**ED alarm (persistent out of frame) indication to automatically generate a FERF indication in the DS3 transmit stream, or a **B**IP8 error detection in the E3 G.832 Framer to generate a FEBE indication in the E3 G.832 transmit stream, or an **L**OF to generate a RLOF indication (A-bit) in the J2 transmit stream. When the E3 G.751 framer is selected, this bit has no effect. When RBLEN is logic 1 and TFRM[1:0] is 00 binary and RFRM[1:0] is 00 binary, assertion of the RED indication by the framer causes a FERF to be transmitted by DS3_TRAN for the duration of the RED assertion. Also, for DS3 frame format, the OOFEN bit is internally forced to logic 0 when RBLEN is logic 1. When RBLEN is logic 0, assertion of the RED indication does not cause transmission of a FERF. When RBLEN is logic 1 and TFRM[1:0] is 01 binary and RFRM[1:0] is 01 binary, any BIP8 error indication by the E3 G.832 framer causes a FEBE to be generated by the E3 G.832 TRAN. When RBLEN is logic 0, BIP8 errors detected by the E3 framer do not cause FEBEs to be generated by the E3_TRAN. When RBLEN is logic 1 and TFRM[1:0] is 10 binary and RFRM[1:0] is 10 binary, any LOF error indication by the J2 framer causes the RLOF bit (also known as the A bit) to be set in the J2 transmit stream. When RBLEN is logic 0, LOF errors detected by the J2 framer do not cause the RLOF bit to be set in the transmit stream.

AISEN:

The AISEN bit enables the receive alarm indication signal to automatically generate a FERF indication (RAI in G.751 or J2 mode) in the transmit stream. This bit operates regardless of framer selected (DS3, E3, or J2). When AISEN is logic 1, assertion of the AIS indication (physical AIS for J2) by the framer causes a FERF/RAI to be transmitted by TRAN for the duration of the AIS assertion. When AISEN is logic 0, assertion of the AIS indication does not cause transmission of a FERF/RAI.
Note that for the RAI to be automatically transmitted when in J2 format, the FEAC[5:0] bits in the XBOC Code register must all be set to logic 1. If the XBOC FEAC code is to be transmitted in J2 mode, LOSEN, OOFEN, AISEN, and LCDEN should all be set to logic 0.

LCDEN:

The LCDEN bit enables the receive out of cell delineation indication to automatically generate a FERF indication (RAI in G.751 or J2 mode) in the transmit stream. This bit operates regardless of framer selected (DS3, E3, or J2) but only in ATM mode. When LCDEN is logic 1, assertion of the LCD indication by the receive FIFO causes a FERF/RAI to be transmitted by the transmitter for the duration of the LCD assertion. When LCDEN is logic 0, assertion of the LCD indication does not cause transmission of a FERF/RAI. Note that for the RAI to be automatically transmitted when in J2 format, the FEAC[5:0] bits in the XBOC Code register must all be set to logic 1. If the XBOC FEAC code is to be transmitted in J2 mode, LOSEN, OOFEN, AISEN, and LCDEN should all be set to logic 0.

Register 005H, 105H, 205H, 305H: S/UNI-QJET Interrupt Status

Bit	Type	Function	Default
Bit 7	R	SPLRI/TTBI	X
Bit 6	R	TXCP50I	X
Bit 5	R	RXCP50I	X
Bit 4	R	RBOCI/PRGDI	X
Bit 3	R	FRMRI/LOFI	X
Bit 2	R	PMONI	X
Bit 1	R	TDPRI	X
Bit 0	R	RDLCI	X

SPLRI/TTBI, TXCP50I, RXCP50I, RBOCI/PRGDI, FRMRI/LOFI, PMONI, TDPRI, RDLCI:

These bits are interrupt status indicators. These bits identify the block that is the source of a pending interrupt. The SPLRI/TTBI bit will be logic 1 if either the SPLR or the TTB block has produced the interrupt. The RBOCI/PRGDI bit will be logic 1 if either the RBOC or PRGD block has produced the interrupt. The FRMRI/LOFI will be logic 1 if either the FRMR (J2, E3, or T3 - whichever one is enabled) or the E3, T3, or J2 Extended Loss of Frame signal (FRMLOFI from register x9CH) is the source of the interrupt. This register is typically used by interrupt service routines to determine the source of a S/UNI-QJET interrupt.

Register 006H: S/UNI-QJET Identification, Master Reset, and Global Monitor Update

Bit	Type	Function	Default
Bit 7	R/W	RESET	0
Bit 6	R	TYPE[3]	1
Bit 5	R	TYPE[2]	0
Bit 4	R	TYPE[1]	0
Bit 3	R	TYPE[0]	0
Bit 2	R	TIP	X
Bit 1	R	ID[1]	1
Bit 0	R	ID[0]	0

This register is used for global performance monitor updates, global software resets, and for device identification. Writing any value except 80H into this register initiates latching of all performance monitor counts in the PMON, RXCP-50, and TXCP-50 blocks in all four quadrants of the S/UNI-QJET. The TIP register bit is used to signal when the latching is complete.

The CPPM counter registers are **not** latched by writing to register 006H. Counters in the CPPM can only be updated by writing to CPPM register addresses (x22H – x2FH).

RESET:

The RESET bit allows software to asynchronously reset the S/UNI-QJET. The software reset is equivalent to setting the RSTB input pin low, except that the S/UNI-QJET Master Test Register is not affected. When a logic 1 is written to RESET, the S/UNI-QJET is reset. When a logic 0 is written to RESET, the reset is removed. The RESET bit must be explicitly set and cleared by writing the corresponding logic value to this register.

TYPE[3:0]:

The TYPE[3:0] bits allow software to identify this device as the S/UNI-QJET member of the S/UNI family of products.

TIP:

The TIP bit is set to a logic one when any value is written to this register. Such a write initiates an accumulation interval transfer and loads all the

performance meter registers in the PMON, RXCP-50, and TXCP-50 blocks in all four quadrants of the S/UNI-QJET. TIP remains high while the transfer is in progress, and is set to a logic zero when the transfer is complete. TIP can be polled by a microprocessor to determine when the accumulation interval transfer is complete. Note that all the transmit and receive line side clocks must be toggling for TIP to be cleared.

ID[1:0]:

The ID[1:0] bits allows software to identify the version level of the S/UNI-QJET.

Register 007H, 107H, 207H, 307H: S/UNI-QJET Clock Activity Monitor and Interrupt Identification

Bit	Type	Function	Default
Bit 7	R	INT[4]	X
Bit 6	R	INT[3]	X
Bit 5	R	INT[2]	X
Bit 4	R	INT[1]	X
Bit 3	R	RCLKA	X
Bit 2	R	TICLKA	X
Bit 1	R	TFCLKA	X
Bit 0	R	RFCLKA	X

RFCLKA:

The RFCLKA bit monitors for low to high transitions on the RFCLK input. RFCLKA is set high on a rising edge of RFCLK, and is set low when this register is read.

TFCLKA:

The TFCLKA bit monitors for low to high transitions on the TFCLK input. TFCLKA is set high on a rising edge of TFCLK, and is set low when this register is read.

TICLKA:

The TICLKA bit monitors for low to high transitions on the TICLK[x] input. TICLKA is set high on a rising edge of TICLK[x], and is set low when this register is read.

RCLKA:

The RCLKA bit monitors for low to high transitions on the RCLK[x] input. RCLKA is set high on a rising edge of RCLK[x], and is set low when this register is read.

INT[4:1]:

The INT[4:1] bits identify which of the four quadrants of the S/UNI-QJET have generated the current interrupt. When the INT[x] bit is set to logic 1, then the Xth quadrant has generated the interrupt. The particular block(s) within that

quadrant which generated the interrupt can be identified by reading the corresponding quadrant's S/UNI-QJET Interrupt Status Register. When the INT[x] bit is set to logic 0, then the Xth quadrant has not generated an interrupt. Note that the INT[4:1] bits are valid only in register address 007H.

Register 008H, 108H, 208H, 308H: SPLR Configuration

Bit	Type	Function	Default
Bit 7	R/W	FORM[1]	0
Bit 6	R/W	FORM[0]	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	REFRAME	0
Bit 2	R/W	PLCPEN	0
Bit 1		Unused	X
Bit 0	R/W	EXT	0

EXT:

The EXT bit disables the internal transmission system sublayer timeslot counter from identifying DS1, DS3, E1, J2, E3 G.751, or E3 G.832 overhead bits. The EXT bit allows transmission formats that are unsupported by the internal timeslot counter to be supported using the ROHM[x] input. When a logic 0 is written to EXT, input transmission system overhead (for DS1, DS3, E1, J2, E3 G.751, and E3 G.832 formats) is indicated using the internal timeslot counter. This counter is synchronized to the transmission system frame alignment using the ROHM[x] (for DS1 or E1 ATM direct-mapped formats), or by the integral framer block (for the DS3, J2, E3 G.751, or E3 G.832 formats).

When a logic 1 is written to EXT, indications on ROHM[x] identify each transmission system overhead bit.

PLCPEN:

The PLCPEN bit enables PLCP framing. When a logic 1 is written to PLCPEN, PLCP framing is enabled. The PLCP format is specified by the FORM[1:0] bits in this register. When a logic 0 is written to PLCPEN, PLCP related functions in the SPLR block are disabled. PLCPEN must be programmed to logic 0 for E3 G.832, J2, and arbitrary framing formats.

REFRAME:

The REFRAME bit is used to trigger reframing. When a logic 1 is written to REFRAME, the S/UNI-QJET is forced out of PLCP frame and a new search

for frame alignment is initiated. Note that only a logic 0 to logic 1 transition of the REFRAME bit triggers reframing; multiple write operations are required to ensure such a transition.

FORM[1:0]:

The FORM[1:0] bits select the PLCP frame format as shown below. These bits must be set to “11” if E1 direct mapped mode is being used (PLCPEN=0 and EXT=1).

Table 7 - SPLR FORM[1:0] Configurations

FORM[1]	FORM[0]	PLCP Framing Format
0	0	DS3
0	1	E3 G.751
1	0	DS1
1	1	E1

Register 009H, 109H, 209H, 309H: SPLR Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	FEBEE	0
Bit 5	R/W	COLSSE	0
Bit 4	R/W	BIPEE	0
Bit 3	R/W	FEE	0
Bit 2	R/W	YELE	0
Bit 1	R/W	LOFE	0
Bit 0	R/W	OOFE	0

OOFE:

The OOFE bit enables interrupt generation when a PLCP out of frame defect is declared or removed. The interrupt is enabled when a logic 1 is written.

LOFE:

The LOFE bit enables interrupt generation when a PLCP loss of frame defect is declared or removed. The interrupt is enabled when a logic 1 is written.

YELE:

The YELE bit enables interrupt generation when a PLCP yellow alarm defect is declared or removed. The interrupt is enabled when a logic 1 is written.

FEE:

The FEE bit enables interrupt generation when the S/UNI-QJET detects a PLCP framing octet error. The interrupt is enabled when a logic 1 is written.

BIPEE:

The BIPEE bit enables interrupt generation when the S/UNI-QJET detects a PLCP bit interleaved parity error. The interrupt is enabled when a logic 1 is written.

COLSSE:

The COLSSE bit enables interrupt generation when the S/UNI-QJET detects a change of PLCP link status. The interrupt is enabled when a logic 1 is written.

FEBEE:

The FEBEE bit enables interrupt generation when the S/UNI-QJET detects a PLCP far end block error. The interrupt is enabled when a logic 1 is written.

Register 00AH, 10AH, 20AH, 30AH: SPLR Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	FEBEI	X
Bit 5	R	COLSSI	X
Bit 4	R	BIPEI	X
Bit 3	R	FEI	X
Bit 2	R	YELI	X
Bit 1	R	LOFI	X
Bit 0	R	OOFI	X

OOFI:

The OOFI bit is set to logic 1 when a PLCP out of frame defect is detected or removed. The OOF defect state is contained in the SPLR Status Register. The OOFI bit position is set to logic 0 when this register is read.

LOFI:

The LOFI bit is set to logic 1 when a PLCP loss of frame defect is detected or removed. The LOF defect state is contained in the SPLR Status Register. The LOFI bit position is set to logic 0 when this register is read.

YELI:

The YELI bit is set to logic 1 when a PLCP yellow alarm defect is detected or removed. The yellow alarm defect state is contained in the SPLR Status Register. The YELI bit position is set to logic 0 when this register is read.

FEI:

The FEI bit is set to logic 1 when a PLCP framing octet error is detected. A framing octet error is generated when one or more errors are detected in the framing alignment octets (A1, and A2), or the path overhead identification octets. The FEI bit position is set to logic 0 when this register is read.

BIPEI:

The BIPEI bit is set to logic 1 when a PLCP bit interleaved parity (BIP) error is detected. BIP errors are detected using the B1 byte in the PLCP path overhead. The BIPEI bit position is set to logic 0 when this register is read.

COLSSI:

The COLSSI bit is set to logic 1 when a PLCP change of link status signal code is detected. The link status signal code is contained in the path status octet (G1). Link status signal codes are required in systems implementing the IEEE-802.6 DQDB protocol. A change of link status event occurs when two consecutive and identical link status codes are received that differ from the current code. The COLSSI bit position is set to logic 0 when this register is read.

FEBEI:

The FEBEI bit is set to logic 1 when a PLCP far end block error (FEBE) is detected. FEBE errors are indicated in the PLCP path status octet (G1). The FEBEI bit position is set to logic 0 when this register is read.

Register 00BH, 10BH, 20BH, 30BH: SPLR Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	LSS[2]	X
Bit 5	R	LSS[1]	X
Bit 4	R	LSS[0]	X
Bit 3		Unused	X
Bit 2	R	YELV	X
Bit 1	R	LOFV	X
Bit 0	R	OOFV	X

OOFV:

The OOFV bit indicates the current PLCP out of frame defect state. When an error is detected in both the A1 and A2 octets or when an error is detected in two consecutive path overhead identifier octets, OOFV is set to logic 1. When the S/UNI-QJET has found two valid, consecutive sets of A1 and A2 octets with two valid and sequential path overhead identifier octets, the OOFV bit is set to logic 0.

LOFV:

The LOFV bit indicates the current PLCP loss of frame defect state. The loss of frame defect state is an integrated version of the out of frame defect state. The declaration/removal times for the loss of frame defect state depends on the selected PLCP format, and are summarized in the table below:

Table 8 - PLCP LOF Declaration/Removal Times

PLCP Format	Declaration (ms)	Removal (ms)
DS3	1	12
E3 G.751	1.12	10
DS1	25	250
E1	20	200

If the OOF defect state is transient, the LOF counter is decremented at a rate 1/12 (DS3 PLCP) or 1/10 (DS1 or E1 PLCP) or 1/9 (G.751 E3 PLCP) of the incrementing rate.

YELV:

The YELV bit indicates the current PLCP yellow alarm defect state. YELV is set to a logic 1 when ten or more consecutive frames are received with the yellow bit (contained in the path status octet) set to a logic 1. YELV is set to a logic 0 when ten or more consecutive frames are received with the yellow bit (contained in the path status octet) set to a logic 0.

LSS[2:0]:

The LSS[2:0] bits contain the current link status signal code. Link status signal codes are required in systems implementing the IEEE-802.6 DQDB protocol. LSS[2:0] is updated when two consecutive and identical link status signal codes are received.

Register 00CH, 10CH, 20CH, 30CH: SPLT Configuration

Bit	Type	Function	Default
Bit 7	R/W	FORM[1]	0
Bit 6	R/W	FORM[0]	0
Bit 5	R/W	M1TYPE	0
Bit 4	R/W	M2TYPE	0
Bit 3	R/W	FIXSTUFF	0
Bit 2	R/W	PLCPEN	0
Bit 1		Unused	X
Bit 0	R/W	EXT	0

EXT:

The EXT bit disables the internal transmission system sublayer timeslot counter from identifying DS1, DS3, E1, J2, E3 G.751, or E3 G.832 overhead bits. The EXT bit allows transmission formats that are unsupported by the internal timeslot counter and must be supported using the TIOHM[x] input. When a logic 0 is written to EXT, input transmission system overhead (for DS1, DS3, E1, J2, E3 G.751, and E3 G.832 formats) is indicated using the internal timeslot counter. This counter flywheels to create the appropriate transmission system alignment. This alignment is indicated on the TOHM[x] output. When a logic 1 is written to EXT, indications on TIOHM[x] identify each transmission system overhead bit. These indications flow through the S/UNI-QJET and appear on the TOHM[x] output where they mark the transmission system overhead placeholder positions in the TDATO[x] stream. EXT should only be set to logic 1 if the TFRM[1:0] bits in the S/UNI-QJET Transmit Configuration register are both set to logic 1 and the arbitrary framing format is desired.

PLCPEN:

The PLCPEN bit enables PLCP frame insertion. When a logic 1 is written to PLCPEN, DS3, E3 G.751, DS1, or E1 PLCP framing is inserted. The PLCP format is specified by the FORM[1:0] bits in this register. When a logic 0 is written to PLCPEN, PLCP related functions in the SPLT block are disabled. The PLCPEN bit must be set to logic 0 for G.832 E3, J2, and arbitrary framing formats.

FIXSTUFF:

The FIXSTUFF bit controls the transmit PLCP frame octet/nibble stuffing used for DS3 and G.751 E3 PLCP frame formats. When a logic 0 is written to FIXSTUFF, stuffing is determined by the REF8KI input. When a logic 1 is written to FIXSTUFF and the DS3 PLCP frame format is enabled, a nibble is stuffed into the 13 nibble trailer twice every three stuff opportunities (i.e. 13, 14, 14 nibbles). This stuff ratio provides for a nominal PLCP frame rate of 125.0002366 µs (an error of 1.9 ppm). When the G.751 E3 PLCP frame format is enabled, 18, 19 or 20 octets are stuffed into the trailer depending on the alignment of the G.751 E3 frame, and the G.751 E3 PLCP frame. This yields a nominal PLCP frame rate of 125 µs.

M2TYPE:

The M2TYPE bit selects the type of code transmitted in the M2 octet. These codes are required in systems implementing the IEEE-802.6 DQDB protocol. When a logic 0 is written to M2TYPE, the fixed pattern type 0 code is transmitted in the M2 octet. When a logic 1 is written to M2TYPE, the 1023 cyclic code pattern (starting with B6 hexadecimal and ending with 8D hexadecimal) is transmitted in the M2 octet. Please refer to TA-TSY-000772, Issue 3 and Supplement 1, for details on the codes.

M1TYPE:

The M1TYPE bit selects the type of code transmitted in the M1 octet. These codes are required in systems implementing the IEEE-802.6 DQDB protocol. When a logic 0 is written to M1TYPE, the fixed pattern type 0 code is transmitted in the M1 octet. When a logic 1 is written to M1TYPE, the 1023 cyclic code pattern (starting with B6 hexadecimal and ending with 8D hexadecimal) is transmitted in the M1 octet. Please refer to TA-TSY-000772, Issue 3 and Supplement 1, for details on the codes.

FORM[1:0]:

When EXT = 0 and PLCPEN = 0, the FORM[1:0] bits and the TFRM[1:0] bits in the S/UNI-QJET Transmit Configuration register select the ATM direct-mapped transmission frame format as shown below. When EXT = 0 and PLCPEN = 1, the FORM[1:0] bits along with the TFRM[1:0] bits select the transmission and PLCP frame format as shown below. When EXT = 1 and TOCTA = 1, then the FORM[1:0] bits control the cell alignment with respect to the transmission overhead given on TIOHM[x] as shown below. The FORM bits have no effect if EXT = 1 and TOCTA = 0.

Table 9 - SPLT FORM[1:0] Configurations

FORM[1]	FORM[0]	PLCP or ATM direct-mapped Framing Format / Cell alignment
0	0	DS3 / nibble
0	1	E3 or J2 / byte
1	0	DS1 / byte
1	1	E1 / byte

Register 00DH, 10DH, 20DH, 30DH: SPLT Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	SRCZN	0
Bit 5	R/W	SRCF1	0
Bit 4	R/W	SRCB1	0
Bit 3	R/W	SRCG1	0
Bit 2	R/W	SRCM1	0
Bit 1	R/W	SRCM2	0
Bit 0	R/W	SRCC1	0

SRCC1:

The SRCC1 bit value ORed with input TPOHINS selects the source for the C1 octet on a bit by bit basis. If the OR results in a logic 0, the C1 bit position is derived internally as specified by the FIXSTUFF bit in the SPLT Configuration Register. If the OR results in a logic 1, the C1 bit position is inserted with the value sampled on TPOH.

SRCM2:

The SRCM2 bit value ORed with input TPOHINS selects the source for the M2 octet on a bit by bit basis. If the OR results in a logic 0, the M2 bit position is derived internally as specified by the M2TYPE bit in the SPLT Configuration Register. If the OR results in a logic 1, the M2 bit position is inserted with the value sampled on TPOH. The M2 octet is set to logic 0 (as required by the ATM Forum User Network Interface specification) by writing this bit position with a logic 1, and connecting the TPOH input to VSS.

SRCM1:

The SRCM1 bit value ORed with input TPOHINS selects the source for the M1 octet on a bit by bit basis. If the OR results in a logic 0, the M1 bit position is derived internally as specified by the M1TYPE bit in the SPLT Configuration Register. If the OR results in a logic 1, the M1 bit position is inserted with the value sampled on TPOH. The M1 octet is set to logic 0 (as required by the ATM Forum User Network Interface specification) by writing this bit position with a logic 1, and connecting the TPOH input to VSS.

SRCG1:

The SRCG1 bit value ORed with input TPOHINS selects the source for the G1 octet on a bit by bit basis. If the OR results in a logic 0, the G1 bit position is derived internally as required. If the OR results in a logic 1, the G1 bit position is inserted with the value sampled on TPOH.

SRCB1:

The SRCB1 bit value ORed with input TPOHINS selects the source for the B1 octet on a bit by bit basis. If the OR results in a logic 0, the internally calculated bit interleaved parity value is inserted in the B1 bit position. If the OR results in a logic 1, the B1 bit position is inserted with the value sampled on TPOH.

SRCF1:

The SRCF1 bit value ORed with input TPOHINS selects the source for the F1 octet on a bit by bit basis. If the OR results in a logic 0, the F1 bit position is determined by the SPLT F1 Octet Register. If the OR results in a logic 1, the F1 bit position is inserted with the value sampled on TPOH.

SRCZN:

The SRCZN bit value ORed with input TPOHINS selects the source for the Zn octets (where n=1 to 4 for the DS1 or E1 PLCP frame formats, n=1 to 6 for the DS3 PLCP frame format, and n=1 to 3 for the G.751 E3 PLCP frame format) on a bit by bit basis. If the OR results in a logic 0, the Zn bit position is forced to a logic 0. If the OR results in a logic 1, the Zn bit position is inserted with the value sampled on TPOH.

Register 00EH, 10EH, 20EH, 30EH: SPLT Diagnostics and G1 Octet

Bit	Type	Function	Default
Bit 7	R/W	DPFRM	0
Bit 6	R/W	DAFRM	0
Bit 5	R/W	DB1	0
Bit 4	R/W	DFEBE	0
Bit 3	R/W	YEL	0
Bit 2	R/W	LSS[2]	0
Bit 1	R/W	LSS[1]	0
Bit 0	R/W	LSS[0]	0

LSS[2:0]:

The LSS[2:0] bits control the value inserted in the link status signal code bit positions of the path status octet (G1). These bits should be written with logic 0 when implementing an ATM Forum UNI-compliant DS3 interface.

YEL:

The YEL bit controls the yellow signal bit position in the path status octet (G1). When a logic 1 is written to YEL, the PLCP yellow alarm signal is transmitted.

DFEBE:

The DFEBE bit controls the insertion of far end block errors in the PLCP frame. When DFEBE is written with a logic 1, a single FEBE is inserted each PLCP frame. When DFEBE is written with a logic 0, FEBEs are indicated based on receive PLCP bit interleaved parity errors.

DB1:

The DB1 bit controls the insertion of bit interleaved parity (BIP) errors in the PLCP frame. When DB1 is written with a logic 1, a single BIP error is inserted in each PLCP frame. When DB1 is written with a logic 0, the bit interleaved parity is calculated and inserted normally.

DAFRM:

The DAFRM bit controls the insertion of frame alignment pattern errors. When DAFRM is written with a logic 1, a single bit error is inserted in each A1

octet, and in each A2 octet. When DAFRM is written with a logic 0, the frame alignment pattern octets are inserted normally.

DPFRM:

The DPFRM bit controls the insertion of parity errors in the path overhead identification (POHID) octets. When DPFRM is written with a logic 1, a parity error is inserted in each POHID octet. When DPFRM is written with a logic 0, the POHID octets are inserted normally.

Register 00FH, 10FH, 20FH, 30FH: SPLT F1 Octet

Bit	Type	Function	Default
Bit 7	R/W	F1[7]	0
Bit 6	R/W	F1[6]	0
Bit 5	R/W	F1[5]	0
Bit 4	R/W	F1[4]	0
Bit 3	R/W	F1[3]	0
Bit 2	R/W	F1[2]	0
Bit 1	R/W	F1[1]	0
Bit 0	R/W	F1[0]	0

F1[7:0]:

The F1[7:0] bits contain the value inserted in the path user channel octet (F1). F1[7] is the most significant bit, and is transmitted first. F1[0] is the least significant bit and is the last bit transmitted in the octet.

Register 010H, 110H, 210H, 310H: Change of PMON Performance Meters

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	LCVCH	X
Bit 4	R	FERRCH	X
Bit 3	R	EXZS	X
Bit 2	R	PERRCH	X
Bit 1	R	CPERRCH	X
Bit 0	R	FEBECH	X

FEBECH:

The FEBECH bit is set to logic 1 if one or more FEBE events (or J2 EXZS events when the J2 framing format is selected) have occurred during the latest PMON accumulation interval.

CPERRCH:

The CPERRCH bit is set to logic 1 if one or more path parity error events have occurred during the latest PMON accumulation interval.

PERRCH:

The PERRCH bit is set to logic 1 if one or more parity error events (or J2 CRC-5 errors) have occurred during the latest PMON accumulation interval.

EXZS:

The EXZS bit is set to logic 1 if one or more summed line code violation events in DS3 mode have occurred during the latest PMON accumulation interval.

FERRCH:

The FERRCH bit is set to logic 1 if one or more F-bit or M-bit error events have occurred during the latest PMON accumulation interval.

LCVCH:

The LCVCH bit is set to logic 1 if one or more line code violation events have occurred during the latest PMON accumulation interval.

Register 011H, 111H, 211H, 311H: PMON Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	INTE	0
Bit 1	R	INTR	X
Bit 0	R	OVR	X

OVR:

The OVR bit indicates the overrun status of the PMON holding registers. A logic 1 in this bit position indicates that a previous interrupt has not been cleared before the end of the next accumulation interval, and that the contents of the holding registers have been overwritten. A logic 0 indicates that no overrun has occurred. This bit is reset to logic 0 when this register is read.

INTR:

The INTR bit indicates the current status of the interrupt signal. A logic 1 in this bit position indicates that a transfer of counter values to the holding registers has occurred; a logic 0 indicates that no transfer has occurred. The INTR bit is set to logic 0 when this register is read.

INTE:

The INTE bit enables the generation of an interrupt when the PMON counter values are transferred to the holding registers. When a logic 1 is written to INTE, the interrupt generation is enabled.

Register 014H, 114H, 214H, 314H: PMON Line Code Violation Event Count LSB

Bit	Type	Function	Default
Bit 7	R	LCV[7]	X
Bit 6	R	LCV[6]	X
Bit 5	R	LCV[5]	X
Bit 4	R	LCV[4]	X
Bit 3	R	LCV[3]	X
Bit 2	R	LCV[2]	X
Bit 1	R	LCV[1]	X
Bit 0	R	LCV[0]	X

Register 015H, 115H, 215H, 315H: PMON Line Code Violation Event Count MSB

Bit	Type	Function	Default
Bit 7	R	LCV[15]	X
Bit 6	R	LCV[14]	X
Bit 5	R	LCV[13]	X
Bit 4	R	LCV[12]	X
Bit 3	R	LCV[11]	X
Bit 2	R	LCV[10]	X
Bit 1	R	LCV[9]	X
Bit 0	R	LCV[8]	X

LCV[15:0]:

LCV[15:0] represents the number of DS3, E3, or J2 line code violation errors that have been detected since the last time the LCV counter was polled.

The counter (and all other counters in the PMON) is polled by writing to any of the PMON register addresses (x14H to x1FH) or to the S/UNI-QJET Identification, Master Reset, and Global Monitor Update register (006H). Such a write transfers the internally accumulated count to the LCV Error Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost. The transfer takes 3 RCLK[x] cycles to complete.

Register 016H, 116H, 216H, 316H: PMON Framing Bit Error Event Count LSB

Bit	Type	Function	Default
Bit 7	R	FERR[7]	X
Bit 6	R	FERR[6]	X
Bit 5	R	FERR[5]	X
Bit 4	R	FERR[4]	X
Bit 3	R	FERR[3]	X
Bit 2	R	FERR[2]	X
Bit 1	R	FERR[1]	X
Bit 0	R	FERR[0]	X

Register 017H, 117H, 217H, 317H: PMON Framing Bit Error Event Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	FERR[9]	X
Bit 0	R	FERR[8]	X

FERR[9:0]:

FERR[9:0] represents the number of DS3 F-bit and M-bit errors, or E3 or J2 framing pattern errors, that have been detected since the last time the framing error counter was polled.

The counter (and all other counters in the PMON) is polled by writing to any of the PMON register addresses (x14H to x1FH) or to the S/UNI-QJET Identification, Master Reset, and Global Monitor Update register (006H). Such a write transfers the internally accumulated count to the FERR Error Event Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost. The transfer takes 255 RCLK[x] cycles to complete in DS3 mode and 3 RCLK[x] cycles to complete in E3 and J2 mode.

This counter is paused when the corresponding framer has lost frame alignment.

Register 018H, 118H, 218H, 318H: PMON Excessive Zero Count LSB

Bit	Type	Function	Default
Bit 7	R	EXZS[7]	X
Bit 6	R	EXZS[6]	X
Bit 5	R	EXZS[5]	X
Bit 4	R	EXZS[4]	X
Bit 3	R	EXZS[3]	X
Bit 2	R	EXZS[2]	X
Bit 1	R	EXZS[1]	X
Bit 0	R	EXZS[0]	X

Register 019H, 119H, 219H, 319H: PMON Excessive Zero Count MSB

Bit	Type	Function	Default
Bit 7	R	EXZS[15]	X
Bit 6	R	EXZS[14]	X
Bit 5	R	EXZS[13]	X
Bit 4	R	EXZS[12]	X
Bit 3	R	EXZS[11]	X
Bit 2	R	EXZS[10]	X
Bit 1	R	EXZS[9]	X
Bit 0	R	EXZS[8]	X

EXZS[15:0]:

In DS3 mode, EXZS[15:0] represents the number of summed Excessive Zeros (EXZS) that occurred during the previous accumulation interval. One or more excessive zeros occurrences within an 85 bit DS3 information block is counted as one summed excessive zero. Excessive zeros are accumulated by this register only when the EXZSO and EXZDET are logic 1 in the DS3 FRMR Additional Configuration Register. This register accumulates summed line code violations when the EXZSO is logic 0. The count of summed line code violations is defined as the number of DS3 information blocks (85 bits) that contain one or more line code violations since the last time the summed LCV counter was polled.

The counter (and all other counters in the PMON) is polled by writing to any of the PMON register addresses (x14H to x1FH) or to the S/UNI-QJET Identification, Master Reset, and Global Monitor Update register (006H). Such a write transfers the internally accumulated count to the EXZS Event Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost. The transfer takes 255 RCLK[x] cycles to complete in DS3 mode and a maximum of 500 RCLK[x] cycles to complete in G.832 E3 mode.

Register 01AH, 11AH, 21AH, 31AH: PMON Parity Error Event Count LSB

Bit	Type	Function	Default
Bit 7	R	PERR[7]	X
Bit 6	R	PERR[6]	X
Bit 5	R	PERR[5]	X
Bit 4	R	PERR[4]	X
Bit 3	R	PERR[3]	X
Bit 2	R	PERR[2]	X
Bit 1	R	PERR[1]	X
Bit 0	R	PERR[0]	X

Register 01BH, 11BH, 21BH, 31BH: PMON Parity Error Event Count MSB

Bit	Type	Function	Default
Bit 7	R	PERR[15]	X
Bit 6	R	PERR[14]	X
Bit 5	R	PERR[13]	X
Bit 4	R	PERR[12]	X
Bit 3	R	PERR[11]	X
Bit 2	R	PERR[10]	X
Bit 1	R	PERR[9]	X
Bit 0	R	PERR[8]	X

PERR[15:0]:

PERR[15:0] represents the number of DS3 P-bit errors, the number of E3 G.832 BIP-8 errors or the number of J2 CRC-5 errors that have been detected since the last time the parity error counter was polled.

The counter (and all other counters in the PMON) is polled by writing to any of the PMON register addresses (x14H to x1FH) or to the S/UNI-QJET Identification, Master Reset, and Global Monitor Update register (006H). Such a write transfers the internally accumulated count to the PERR Error Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost. The transfer takes 255 RCLK[x] cycles to complete in DS3 mode and 3 RCLK[x] cycles to complete in E3 and J2 mode.

This counter is paused when the corresponding framer has lost frame alignment.

Register 01CH, 11CH, 21CH, 31CH: PMON Path Parity Error Event Count LSB

Bit	Type	Function	Default
Bit 7	R	CPERR[7]	X
Bit 6	R	CPERR[6]	X
Bit 5	R	CPERR[5]	X
Bit 4	R	CPERR[4]	X
Bit 3	R	CPERR[3]	X
Bit 2	R	CPERR[2]	X
Bit 1	R	CPERR[1]	X
Bit 0	R	CPERR[0]	X

Register 01DH, 11DH, 21DH, 31DH: PMON Path Parity Error Event Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	CPERR[13]	X
Bit 4	R	CPERR[12]	X
Bit 3	R	CPERR[11]	X
Bit 2	R	CPERR[10]	X
Bit 1	R	CPERR[9]	X
Bit 0	R	CPERR[8]	X

CPERR[13:0]:

When configured for DS3 applications, CPERR[13:0] represents the number of DS3 path parity errors that have been detected since the last time the DS3 path parity error counter was polled.

This counter is forced to zero when the S/UNI-QJET is configured for either J2 and E3 applications.

The counter (and all other counters in the PMON) is polled by writing to any of the PMON register addresses (x14H to x1FH) or to the S/UNI-QJET Identification, Master Reset, and Global Monitor Update register (006H). Such a write transfers the internally accumulated count to the CPERR Error Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost. The transfer takes 255 RCLK[x] cycles to complete.

This counter is paused when the corresponding framer has lost frame alignment.

Register 01EH, 11EH, 21EH, 31EH: PMON FEBE/J2-EXZS Event Count LSB

Bit	Type	Function	Default
Bit 7	R	FEBE/J2-EXZS[7]	X
Bit 6	R	FEBE/J2-EXZS[6]	X
Bit 5	R	FEBE/J2-EXZS[5]	X
Bit 4	R	FEBE/J2-EXZS[4]	X
Bit 3	R	FEBE/J2-EXZS[3]	X
Bit 2	R	FEBE/J2-EXZS[2]	X
Bit 1	R	FEBE/J2-EXZS[1]	X
Bit 0	R	FEBE/J2-EXZS[0]	X

Register 01FH, 11FH, 21FH, 31FH: PMON FEBE/J2-EXZS Event Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	FEBE/J2-EXZS[13]	X
Bit 4	R	FEBE/J2-EXZS[12]	X
Bit 3	R	FEBE/J2-EXZS[11]	X
Bit 2	R	FEBE/J2-EXZS[10]	X
Bit 1	R	FEBE/J2-EXZS[9]	X
Bit 0	R	FEBE/J2-EXZS[8]	X

FEBE/J2-EXZS[13:0]:

FEBE/J2-EXZS[13:0] represents the number of DS3 or E3 G.832 far end block errors that have been detected since the last time the FEBE error counter was polled.

In J2 mode, FEBE/J2-EXZS[13:0] represents the number of Excessive Zeros (EXZS is a string of 8 or more consecutive zeros) that have occurred during the previous accumulation interval.

The counter (and all other counters in the PMON) is polled by writing to any of the PMON register addresses (x14H to x1FH) or to the S/UNI-QJET Identification, Master Reset, and Global Monitor Update register (006H). Such a write transfers the internally accumulated count to the FEBE Event Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost. The transfer takes 255 RCLK[x] cycles to complete in DS3 mode and 3 RCLK[x] cycles to complete in E3 and J2 mode.

This counter is paused when the corresponding framer has lost frame alignment.

Register 021H, 121H, 221H, 321H: CPPM Change of CPPM Performance Meters

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	FEBECH	X
Bit 1	R	FECH	X
Bit 0	R	BIPECH	X

BIPECH:

The BIPECH bit is set to logic 1 if one or more PLCP bit interleaved parity error events have occurred since the last CPPM accumulation interval.

FECH:

The FECH bit is set to logic 1 if one or more PLCP frame alignment pattern octet errors, or path overhead identification octet errors have occurred since the last CPPM accumulation interval.

FEBECH:

The FEBECH bit is set to logic 1 if one or more PLCP far end block error events have occurred since the last CPPM accumulation interval.

Register 022H, 122H, 222H, 322H: CPPM B1 Error Count LSB

Bit	Type	Function	Default
Bit 7	R	B1E[7]	X
Bit 6	R	B1E[6]	X
Bit 5	R	B1E[5]	X
Bit 4	R	B1E[4]	X
Bit 3	R	B1E[3]	X
Bit 2	R	B1E[2]	X
Bit 1	R	B1E[1]	X
Bit 0	R	B1E[0]	X

Register 023H, 123H, 223H, 323H: CPPM B1 Error Count MSB

Bit	Type	Function	Default
Bit 7	R	B1E[15]	X
Bit 6	R	B1E[14]	X
Bit 5	R	B1E[13]	X
Bit 4	R	B1E[12]	X
Bit 3	R	B1E[11]	X
Bit 2	R	B1E[10]	X
Bit 1	R	B1E[9]	X
Bit 0	R	B1E[8]	X

B1E[15:0]:

B1E[15:0] represents the number of PLCP bit interleaved parity (BIP) errors that have been detected since the last time the B1 error counter was polled. The counter (and all other counters in the CPPM) is polled by writing to any of the CPPM register addresses (x22H - x2FH). Such a write transfers the internally accumulated count to the B1 Error Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer occurs within 67 RCLK periods (1.5 µs for the DS3 bit rate; 1.95µs for the E3 bit rate) of the write. The transfer and reset is carried out in a manner that coincident events are not lost. B1 errors are not accumulated when the S/UNI-QJET has declared a PLCP loss of frame defect state.

Register 024H, 124H, 224H, 324H: CPPM Framing Error Event Count LSB

Bit	Type	Function	Default
Bit 7	R	FE[7]	X
Bit 6	R	FE[6]	X
Bit 5	R	FE[5]	X
Bit 4	R	FE[4]	X
Bit 3	R	FE[3]	X
Bit 2	R	FE[2]	X
Bit 1	R	FE[1]	X
Bit 0	R	FE[0]	X

Register 025H, 125H, 225H, 325H: CPPM Framing Error Event Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	FE[11]	X
Bit 2	R	FE[10]	X
Bit 1	R	FE[9]	X
Bit 0	R	FE[8]	X

FE[11:0]:

FE[11:0] represents the number of PLCP framing pattern octet errors and path overhead identification octet errors that have been detected since the last time the framing error event counter was polled. The counter (and all other counters in the CPPM) is polled by writing to any of the CPPM register addresses (x22H - x2FH). Such a write transfers the internally accumulated count to the Framing Error Event Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer occurs within 67 RCLK periods (1.5 µs for the DS3 bit rate; 1.95µs for the E3 bit rate) of the write. The transfer and reset is carried out in a manner that coincident events are not lost. Framing error errors are not accumulated when the S/UNI-QJET has declared a PLCP loss of frame defect state.

Register 026H, 126H, 226H, 326H: CPPM FEBE Count LSB

Bit	Type	Function	Default
Bit 7	R	FEBE[7]	X
Bit 6	R	FEBE[6]	X
Bit 5	R	FEBE[5]	X
Bit 4	R	FEBE[4]	X
Bit 3	R	FEBE[3]	X
Bit 2	R	FEBE[2]	X
Bit 1	R	FEBE[1]	X
Bit 0	R	FEBE[0]	X

Register 027H, 127H, 227H, 327H: CPPM FEBE Count MSB

Bit	Type	Function	Default
Bit 7	R	FEBE[15]	X
Bit 6	R	FEBE[14]	X
Bit 5	R	FEBE[13]	X
Bit 4	R	FEBE[12]	X
Bit 3	R	FEBE[11]	X
Bit 2	R	FEBE[10]	X
Bit 1	R	FEBE[9]	X
Bit 0	R	FEBE[8]	X

FEBE[15:0]:

FEBE[15:0] represents the number of PLCP far end block errors (FEBE) that have been detected since the last time the FEBE error counter was polled. The counter (and all other counters in the CPPM) is polled by writing to any of the CPPM register addresses (x22H - x2FH). Such a write transfers the internally accumulated count to the FEBE Error Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer occurs within 67 RCLK periods (1.5 µs for the DS3 bit rate; 1.95µs for the E3 bit rate) of the write. The transfer and reset is carried out in a manner that coincident events are not lost. FEBE errors are not accumulated when the S/UNI-QJET has declared a PLCP loss of frame defect state.

Register 030H, 130H, 230H, 330H: DS3 FRMR Configuration

Bit	Type	Function	Default
Bit 7	R/W	AISPAT	1
Bit 6	R/W	FDET	0
Bit 5	R/W	MBDIS	0
Bit 4	R/W	M3O8	0
Bit 3	R/W	UNI	0
Bit 2	R/W	REFR	0
Bit 1	R/W	AISC	0
Bit 0	R/W	CBE	0

CBE:

The CBE bit enables the DS3 C-bit parity application. When a logic 1 is written to CBE, C-bit parity mode is enabled. When a logic 0 is written to CBE, the DS3 M23 format is selected. While the C-bit parity application is enabled, C-bit parity error events, far end block errors are accumulated.

AISC:

The AISC bit controls the algorithm used to detect the alarm indication signal (AIS). When a logic 1 is written to AISC, the algorithm checks that a framed DS3 signal with all C-bits set to logic 0 is observed for a period of time before declaring AIS. The payload contents are checked to the pattern selected by the AISPAT bit. When a logic 0 is written to AISC, the AIS detection algorithm is determined solely by the settings of AISPAT and AISONES register bits (see bit mapping table in the Additional Configuration Register description).

REFR:

The REFR bit initiates a DS3 reframe. When a logic 1 is written to REFR, the S/UNI-QJET is forced out-of-frame, and a new search for frame alignment is initiated. Note that only a low to high transition of the REFR bit triggers reframing; multiple write operations are required to ensure such a transition.

UNI:

The UNI bit configures the S/UNI-QJET to accept either dual-rail or single-rail receive DS3 streams. When a logic 1 is written to UNI, the S/UNI-QJET accepts a single-rail DS3 stream on RDATI. The S/UNI-QJET accumulates

line code violations on the RLCV input. When a logic 0 is written to UNI, the S/UNI-QJET accepts B3ZS-encoded dual-rail data on RPOS and RNEG.

M3O8:

The M3O8 bit controls the DS3 out of frame decision criteria. When a logic 1 is written to M3O8, DS3 out of frame is declared when 3 of 8 framing bits (F-bits) are in error. When a logic 0 is written to M3O8, the 3 of 16 framing bits in error criteria is used, as recommended in ANSI T1.107

MBDIS:

The MBDIS bit disables the use of M-bit errors as a criteria for losing frame alignment. When MBDIS is set to logic 1, M-bit errors are disabled from causing an OOF; the loss of frame criteria is based solely on the number of F-bit errors selected by the M3O8 bit. When MBDIS is set to logic 0, errors in either M-bits or F-bits are enabled to cause an OOF. When MBDIS is logic 0, an OOF can occur when one or more M-bit errors occur in 3 out of 4 consecutive M-frames, or when the F-bit error ratio selected by the M3O8 bit is exceeded.

FDET:

The FDET bit selects the fast detection timing for AIS, IDLE and RED. When FDET is set to logic 1, the AIS, IDLE, and RED detection time is 2.23 ms; when FDET is set to logic 0, the detection time is 13.5 ms.

AISPAT:

The AISPAT bit controls the pattern used to detect the alarm indication signal (AIS). When a logic 1 is written to AISPAT, the AIS detection algorithm checks that a framed DS3 signal containing the repeating pattern 1010... is present. The C-bits are checked for the value specified by the AISC bit setting. When a logic 0 is written to AISPAT, the AIS detection algorithm is determined solely by the settings of AISC and AISONES register bits (see bit mapping table in the Additional Configuration Register description).

Register 031H, 131H, 231H, 331H: DS3 FRMR Interrupt Enable (ACE=0)

Bit	Type	Function	Default
Bit 7	R/W	COFAE	0
Bit 6	R/W	REDE	0
Bit 5	R/W	CBITE	0
Bit 4	R/W	FERFE	0
Bit 3	R/W	IDLE	0
Bit 2	R/W	AISE	0
Bit 1	R/W	OOFE	0
Bit 0	R/W	LOSE	0

LOSE:

The LOSE bit enables interrupt generation when a DS3 loss of signal defect is declared or removed. The interrupt is enabled when a logic 1 is written.

OOFE:

The OOFE bit enables interrupt generation when a DS3 out of frame defect is declared or removed. The interrupt is enabled when a logic 1 is written.

AISE:

The AISE bit enables interrupt generation when the DS3 AIS maintenance signal is detected or removed. The interrupt is enabled when a logic 1 is written.

IDLE:

The IDLE bit enables interrupt generation when the DS3 IDLE maintenance signal is detected or removed. The interrupt is enabled when a logic 1 is written.

FERFE:

The FERFE bit enables interrupt generation when a DS3 far end receive failure defect is declared or removed. The interrupt is enabled when a logic 1 is written.

CBITE:

The CBITE bit enables interrupt generation when the S/UNI-QJET detects a change of state in the DS3 application identification channel. The interrupt is enabled when a logic 1 is written.

REDE:

The REDE bit enables an interrupt to be generated when a change of state of the DS3 RED indication occurs. The DS3 RED indication is visible in the REDV bit location of the DS3 FRMR Status register. When REDE is set to logic 1, the interrupt output, INTB, is set low when the state of the RED indication changes.

COFAE:

The COFAE bit enables interrupt generation when the S/UNI-QJET detects a DS3 change of frame alignment. The interrupt is enabled when a logic 1 is written.

Register 031H, 131H, 231H, 331H: DS3 FRMR Additional Configuration Register (ACE=1)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	AISONES	0
Bit 4	R/W	BPVO	0
Bit 3	R/W	EXZSO	0
Bit 2	R/W	EXZDET	0
Bit 1	R/W	SALGO	0
Bit 0	R/W	DALGO	0

DALGO:

The DALGO bit determines the criteria used to decode a valid B3ZS signature. When DALGO is set to logic 1, a valid B3ZS signature is declared and 3 zeros substituted whenever a zero followed by a bipolar violation of the opposite polarity to the last observed BPV is seen. When the DALGO bit is set to logic 0, a valid B3ZS signature is declared and the 3 zeros are substituted whenever a zero followed by a bipolar violation is observed.

SALGO:

The SALGO bit determines the criteria used to establish a valid B3ZS signature used to map BPVs to line code violation indications. Any BPV that is not part of a valid B3ZS signature is indicated as an LCV. When the SALGO bit is set to logic 1, a valid B3ZS signature is declared whenever a zero followed by a bipolar violation is observed. When SALGO is set to logic 0, a valid B3ZS signature is declared whenever a zero followed by a bipolar violation of the opposite polarity to the last observed BPV is seen.

EXZDET:

The EXZDET bit determines the type of zero occurrences to be included in the LCV indication. When EXZDET is set to logic 1, the occurrence of an excessive zero generates a single pulse indication that is used to indicate an LCV. When EXZDET is set to logic 0, every occurrence of 3 consecutive zeros generates a pulse indication that is used to indicate an LCV. For example, if a sequence of 15 consecutive zeros were received, with

EXZDET=1 only a single LCV would be indicated for this string of excessive zeros; with EXZDET=0, five LCVs would be indicated for this string (i.e. one LCV for every 3 consecutive zeros).

EXZSO:

The EXZSO bit enables only summed zero occurrences to be accumulated in the PMON EXZS Count Registers. When EXZSO is set to logic 1, any excessive zeros occurrences over an 85 bit period increments the PMON EXZS counter by one. When EXZSO is set to logic 0, summed LCVs are accumulated in the PMON EXZS Count Registers. A summed LCV is defined as the occurrence of either BPVs not part of a valid B3ZS signature or 3 consecutive zeros (or excessive zeros if EXZDET=1) occurring over an 85 bit period; each summed LCV occurrence increment the PMON EXZS counter by one.

BPVO:

The BPVO bit enables only bipolar violations to indicate line code violations and be accumulated in the PMON LCV Count Registers. When BPVO is set to logic 1, only BPVs not part of a valid B3ZS signature generate an LCV indication and increment the PMON LCV counter. When BPVO is set to logic 0, both BPVs not part of a valid B3ZS signature, and either 3 consecutive zeros or excessive zeros generate an LCV indication and increment the PMON LCV counter.

Table 10 - DS3 FRMR EXZS/LCV count configurations

Register Bit			Counter Function	
EXZSO	**BPVO**	**EXZDET**	**PMON EXZ Count**	**PMON LCV Count**
0	0	0	Summed LCVs	BPVs & every 3 consecutive zeros
0	0	1	Summed LCVs	BPVs & every string of 3+ consecutive zeros
0	1	0	Reserved	Reserved
0	1	1	Reserved	Reserved
1	0	0	Summed excessive zeros	BPVs & every 3 consecutive zeros
1	0	1	Summed excessive zeros	BPVs & every string of 3+ consecutive zeros
1	1	0	Summed excessive zeros	Only BPVs
1	1	1	Summed excessive zeros	Only BPVs

AISONES:

The AISONES bit controls the pattern used to detect the alarm indication signal (AIS) when both AISPAT and AISC bits in DS3 FRMR Configuration register are logic 0; if either AISPAT or AISC are logic 1, the AISONES bit is ignored. When a logic 0 is written to AISONES, the algorithm checks that a framed all-ones payload pattern (1111...) signal is observed for a period of time before declaring AIS. Only the payload bits are observed to follow an all-ones pattern, the overhead bits (X, P, M, F, C) are ignored. When a logic 1 is written to AISONES, the algorithm checks that an unframed all-ones pattern (1111...) signal is observed for a period of time before declaring AIS. In this case all the bits, including the overhead, are observed to follow an all-ones pattern. The valid combinations of AISPAT, AISC, and AISONES bits are summarized below:

Table 11 - DS3 FRMR AIS Configurations

AISPAT	AISC	AISONES	AIS Detected
1	0	X	Framed DS3 stream containing repeating 1010… pattern; overhead bits ignored.
0	1	X	Framed DS3 stream containing C-bits all logic 0; payload bits ignored.
1	1	X	Framed DS3 stream containing repeating 1010… pattern in the payload, C-bits all logic 0, and X-bits=1. This can be detected by setting both AISPAT and AISC high, and declaring AIS only when AISV=1 and FERFV=0 (Register x33H).
0	0	0	Framed DS3 stream containing all-ones payload pattern; overhead bits ignored.
0	0	1	Unframed all-ones DS3 stream.

Register 032H, 132H, 232H, 332H: DS3 FRMR Interrupt Status

Bit	Type	Function	Default
Bit 7	R	COFAI	X
Bit 6	R	REDI	X
Bit 5	R	CBITI	X
Bit 4	R	FERFI	X
Bit 3	R	IDLI	X
Bit 2	R	AISI	X
Bit 1	R	OOFI	X
Bit 0	R	LOSI	X

LOSI:

The LOSI bit is set to logic 1 when a loss of signal defect is detected or removed. The LOSI bit position is set to logic 0 when this register is read.

OOFI:

The OOFI bit is set to logic 1 when an out of frame defect is detected or removed. The OOFI bit position is set to logic 0 when this register is read.

AISI:

The AISI bit is set to logic 1 when the DS3 AIS maintenance signal is detected or removed. The AISI bit position is set to logic 0 when this register is read.

IDLI:

The IDLI bit is set to logic 1 when the DS3 IDLE maintenance signal is detected or removed. The IDLI bit position is set to logic 0 when this register is read.

FERFI:

The FERFI bit is set to logic 1 when a FERF defect is detected or removed. The FERFI bit position is set to logic 0 when this register is read.

CBITI:

The CBITI bit is set to logic 1 when a change of state is detected in the DS3 application identification channel. The CBITI bit position is set to logic 0 when this register is read.

REDI:

The REDI bit indicates that a change of state of the DS3 RED indication has occurred. The DS3 RED indication is visible in the REDV bit location of the DS3 FRMR Status register. When the REDI bit is a logic 1, a change in the RED state has occurred. When the REDI bit is logic 0, no change in the RED state has occurred.

COFAI:

The COFAI bit is set to logic 1 when a change of frame alignment is detected. A COFA is generated when a new DS3 frame alignment is determined that differs from the last known frame alignment. The COFAI bit position is set to logic 0 when this register is read.

Register 033H, 133H, 233H, 333H: DS3 FRMR Status

Bit	Type	Function	Default
Bit 7	R/W	ACE	0
Bit 6	R	REDV	X
Bit 5	R	CBITV	X
Bit 4	R	FERFV	X
Bit 3	R	IDLV	X
Bit 2	R	AISV	X
Bit 1	R	OOFV	X
Bit 0	R	LOSV	X

LOSV:

The LOSV bit indicates the current loss of signal defect state. LOSV is a logic 1 when a sequence of 175 zeros is detected on the B3ZS encoded DS3 receive stream. LOSV is a logic 0 when a signal with a ones density greater than 33% for 175 ± 1 bit periods is detected.

OOFV:

The OOFV bit indicates the current DS3 out of frame defect state. When the S/UNI-QJET has lost frame alignment and is searching for the new alignment, OOFV is set to logic 1. When the S/UNI-QJET has found frame alignment, the OOFV bit is set to logic 0.

AISV:

The AISV bit indicates the alarm indication signal state. When the S/UNI-QJET detects the AIS maintenance signal, AISV is set to logic 1.

IDLV:

The IDLV bit indicates the IDLE signal state. When the S/UNI-QJET detects the IDLE maintenance signal, IDLV is set to logic 1.

FERFV:

The FERFV bit indicates the current far end receive failure defect state. When the S/UNI-QJET detects an M-frame with the X1 and X2 bits both set to zero, FERFV is set to logic 1. When the S/UNI-QJET detects an M-frame with the X1 and X2 bits both set to one, FERFV is set to logic 0.

CBITV:

The CBITV bit indicates the application identification channel (AIC) state. CBITV is set to logic 1 (indicating the presence of the C-bit parity application) when the AIC bit is set high for 63 consecutive M-frames. CBITV is set to logic 0 (indicating the presence of the M23 or SYNTRAN applications) when AIC is set low for 2 or more M-frames in the last 15.

REDV:

The REDV bit indicates the current state of the DS3 RED indication. When the REDV bit is a logic 1, the DS3 FRMR frame alignment acquisition circuitry has been out of frame for 2.23ms (or for 13.5ms when FDET is logic 0). When the REDV bit is logic 0, the frame alignment circuitry has found frame (i.e. OOFV=0) for 2.23ms (or 13.5ms if FDET=0).

ACE:

The ACE bit selects the Additional Configuration Register. This register is located at address x31H, and is only accessible when the ACE bit is set to logic 1. When ACE is set to logic 0, the Interrupt Enable register is accessible at address x31H.

Register 034H, 134H, 234H, 334H: DS3 TRAN Configuration

Bit	Type	Function	Default
Bit 7	R/W	CBTRAN	0
Bit 6	R/W	AIS	0
Bit 5	R/W	IDL	0
Bit 4	R/W	FERF	0
Bit 3	R/W	Reserved	0
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	CBIT	0

CBIT:

The CBIT bit enables the DS3 C-bit parity application. When CBIT is written with a logic 1, C-bit parity is enabled, and the S/UNI-QJET modifies the C-bits as required to include the path maintenance data link, the FEAC channel, the far end block error indication, and the path parity. When CBIT is written with a logic 0, the M23 application is selected, and each C-bit is set to logic 1 by the S/UNI-QJET except for the first C-bit of the frame, which is forced to toggle every frame. Note that the C-bits may be modified as required using the DS3 overhead access port (TOH) regardless of the setting of this bit.

FERF:

The FERF bit enables insertion of the far end receive failure maintenance signal in the DS3 stream. When FERF is written with a logic 1, the X1 and X2 overhead bit positions are set to logic 0. When FERF is written with a logic 0, the X1 and X2 overhead bit positions in the DS3 stream are set to logic 1.

IDL:

The IDL bit enables insertion of the idle maintenance signal in the DS3 stream. When IDL is written with a logic 1, the DS3 payload is overwritten with the repeating pattern 1100.... The DS3 overhead bit insertion (X, P, M F, and C) continues normally. When IDL is written with a logic 0, the idle signal is not inserted.

AIS:

The AIS bit enables insertion of the AIS maintenance signal in the DS3 stream. When AIS is written with a logic 1, the DS3 payload is overwritten with the repeating pattern 1010.... The DS3 overhead bit insertion (X, P, M and F) continues normally. The values inserted in the C-bits during AIS transmission are controlled by the CBTRAN bit in this register. When AIS is written with a logic 0, the AIS signal is not inserted.

CBTRAN:

The CBTRAN bit controls the C-bit values during AIS transmission. When CBTRAN is written with a logic 0, the C-bits are overwritten with zeros during AIS transmission as specified in ANSI T1.107. When CBTRAN is written with a logic 1, C-bit insertion continues normally (as controlled by the CBIT bit in this register) during AIS transmission.

Reserved:

The reserved bit must be programmed to logic 0 for proper operation.

Register 035H, 135H, 235H, 335H: DS3 TRAN Diagnostic

Bit	Type	Function	Default
Bit 7	R/W	DLOS	0
Bit 6	R/W	DLCV	0
Bit 5		Unused	X
Bit 4	R/W	DFERR	0
Bit 3	R/W	DMERR	0
Bit 2	R/W	DCPERR	0
Bit 1	R/W	DPERR	0
Bit 0	R/W	DFEBE	0

DFEBE:

The DFEBE bit controls the insertion of far end block errors in the DS3 stream. When DFEBE is written with a logic 1, and the C-bit parity application is enabled, the three C-bits in M-subframe 4 are set to a logic 0. When DFEBE is written with a logic 0, FEBEs are indicated based on receive framing bit errors and path parity errors.

DPERR:

The DPERR bit controls the insertion of parity errors (P-bit errors) in the DS3 stream. When DPERR is written with a logic 1, the P-bits are inverted before insertion. When DPERR is written with a logic 0, the parity is calculated and inserted normally.

DCPERR:

The DCPERR bit controls the insertion of path parity errors in the DS3 stream. When DCPERR is written with a logic 1 and the C-bit parity application is enabled, the three C-bits in M-subframe 3 are inverted before insertion. When DCPERR is written with a logic 0, the path parity is calculated and inserted normally.

DMERR:

The DMERR bit controls the insertion of M-bit framing errors in the DS3 stream. When DMERR is written with a logic 1, the M-bits are inverted before insertion. When DMERR is written with a logic 0, the M-bits are inserted normally.

DFERR:

The DFERR bit controls the insertion of F-bit framing errors in the DS3 stream. When DFERR is written with a logic 1, the F-bits are inverted before insertion. When DFERR is written with a logic 0, the F-bits are inserted normally.

DLCV:

The DLCV bit controls the insertion of a single line code violation in the DS3 stream. When DLCV is written with a logic 1, a line code violation is inserted by generating an incorrect polarity of violation in the next B3ZS signature. The data being transmitted must therefore contain periods of three consecutive zeros in order for the line code violation to be inserted. For example, line code violations may not be inserted when transmitting AIS, but may be inserted when transmitting the idle signal. DLCV is automatically cleared upon insertion of the line code violation.

DLOS:

The DLOS bit controls the insertion of loss of signal in the DS3 stream. When DLOS is written with a logic 1, the data on outputs TPOS/TDATO and TNEG/TOHM is forced to continuous zeros.

Register 038H, 138H, 238H, 338H: E3 FRMR Framing Options

Bit	Type	Function	Default
Bit 7	Unused	X	
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	UNI	0
Bit 3	R/W	FORMAT[1]	0
Bit 2	R/W	FORMAT[0]	0
Bit 1	R/W	REFRDIS	0
Bit 0	R/W	REFR	0

REFR:

A transition from logic 0 to logic 1 in the REFR bit position forces the E3 Framer to initiate a search for frame alignment. The bit must be cleared to logic 0, then set to logic 1 again to initiate subsequent searches for frame alignment.

REFRDIS:

The REFRDIS bit disables reframing under the consecutive framing bit error condition once frame alignment has been found, leaving reframing to be initiated only by software via the REFR bit. A logic 1 in the REFRDIS bit position causes the FRMR to remain "locked in frame" once initial frame alignment has been found. A logic 0 allows reframing to occur when four consecutive framing patterns are received in error.

FORMAT[1:0]:

The FORMAT[1:0] bits determine the framing mode used for pattern matching when finding frame alignment and for generating the output status signals. The FORMAT[1:0] bits select one of two framing formats:

Table 12 - E3 FRMR FORMAT[1:0] Configurations

FORMAT[1]	FORMAT[0]	Framing Format Selected
0	0	G.751 E3 format
0	1	G.832 E3 format
1	0	Reserved
1	1	Reserved

UNI:

The UNI bit selects the mode of the receive data interface. When UNI is logic 1, the E3-FRMR expects unipolar data on the RDATI input and accepts line code violation indications on the RLCV input. When UNI is logic 0, the E3-FRMR expects bipolar data on the RPOS and RNEG inputs and decodes the pulses according to the HDB3 line code.

Reserved:

The Reserved bit must be programmed to logic 0 for proper operation.

Register 039H, 139H, 239H, 339H: E3 FRMR Maintenance Options

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	WORDBIP	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	WORDERR	0
Bit 2	R/W	PYLD&JUST	0
Bit 1	R/W	FERFDET	0
Bit 0	R/W	TMARKDET	0

TMARKDET:

The TMARKDET bit determines the persistency check performed on the Timing Marker bit (bit 8 of the G.832 Maintenance and Adaptation byte). When TMARKDET is logic 1, the Timing Marker bit must be in the same state for 5 consecutive frames before the TIMEMK status is changed to that state. When TMARKDET is logic 0, the Timing Marker bit must be in the same state for 3 consecutive frames. When a framing mode other than G.832 is selected, the setting of the TMARKDET bit is ignored.

FERFDET:

The FERFDET bit determines the persistency check performed on the Far End Receive Failure (FERF) bit (bit 1 of the G.832 Maintenance and Adaptation byte) or on the Remote Alarm indication (RAI) bit (bit 11 of the frame in G.751 mode). When FERFDET is logic 1, the FERF, or RAI, bit must be in the same state for 5 consecutive frames before the FERF/RAI status is changed to that state. When FERFDET is logic 0, the FERF, or RAI, bit must be in the same state for 3 consecutive frames.

PYLD&JUST:

The PYLD&JUST bit selects whether the justification service bits and the tributary justification bits in framing mode G.751 is indicated as overhead or payload. When PYLD&JUST is logic 1, the justification service bits and the tributary justification bits are indicated as payload to the SPLR. When PYLD&JUST is logic 0, the justification service and tributary justification bits

are indicated as overhead to SPLR. For G.751 ATM applications, this bit must be set to logic 1 for correct cell mapping.

WORDERR:

The WORDERR bit selects whether the framing bit error indication pulses accumulated in PMON indicate all bit errors in the framing pattern or only one error for one or more errors in the framing pattern. When WORDERR is logic 1, the FERR indication to PMON pulses once per frame, accumulating one error for one or more framing bit errors occurred. When WORDERR is logic 0, the FERR indication to PMON pulses for each and every framing bit error that occurs; PMON accumulates all framing bit errors.

WORDBIP:

The WORDBIP bit selects whether the parity bit error indication pulses to the E3-TRAN block indicate all bit errors in the BIP-8 pattern or only one error for one or more errors in the BIP-8 pattern. When WORDBIP is logic 1, the parity error indication to the E3 TRAN block pulses once per frame, indicating that one or more parity bit errors occurred. When WORDBIP is logic 0, the parity error indication to the E3-TRAN block pulses for each and every parity bit error that occurs. For G.832 applications, this bit should be set to logic 1.

Register 03AH, 13AH, 23AH, 33AH: E3 FRMR Framing Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	CZDE	0
Bit 3	R/W	LOSE	0
Bit 2	R/W	LCVE	0
Bit 1	R/W	COFAE	0
Bit 0	R/W	OOFE	0

OOFE:

The OOFE bit is an interrupt enable. When OOFE is logic 1, a change of state of the OOF status generates an interrupt and sets the INTB output to logic 0. When OOFE is logic 0, changes of state of the OOF status are disabled from causing interrupts on the INTB output.

COFAE:

The COFAE bit is an interrupt enable. When COFAE is logic 1, a change of frame alignment generates an interrupt and sets the INTB output to logic 0. When COFAE is logic 0, changes of frame alignment are disabled from causing interrupts on the INTB output.

LCVE:

The LCVE bit is an interrupt enable. When LCVE is logic 1, detection of a line code violation generates an interrupt and sets the INTB output to logic 0. When LCVE is logic 0, occurrences of line code violations are disabled from causing interrupts on the INTB output.

LOSE:

The LOSE bit is an interrupt enable. When LOSE is logic 1, a change of state of the loss-of-signal generates an interrupt and sets the INTB output to logic 0. When LOSE is logic 0, occurrences of loss-of-signal are disabled from causing interrupts on the INTB output.

CZDE:

The CZDE bit is an interrupt enable. When CZDE is logic 1, detection of four consecutive zeros in the HDB3-encoded stream generates an interrupt and sets the INTB output to logic 0. When CZDE is logic 0, occurrences of consecutive zeros are disabled from causing interrupts on the INTB output.

Register 03BH, 13BH, 23BH, 33BH: E3 FRMR Framing Interrupt Indication and Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	CZDI	X
Bit 5	R	LOSI	X
Bit 4	R	LCVI	X
Bit 3	R	COFAI	X
Bit 2	R	OOFI	X
Bit 1	R	LOS	X
Bit 0	R	OOF	X

OOF:

The OOF bit indicates the current state of the E3-FRMR. When OOF is logic 1, the E3-FRMR is out of frame alignment and actively searching for the new alignment. While OOF is high all status indications and overhead extraction continue with the previous known alignment. When OOF is logic 0, the E3-FRMR has found a valid frame alignment and is operating in a maintenance mode, indicating framing bit errors, and extracting and processing overhead bits. During reset, OOF is set to logic 1, but the setting may change prior to the register being read.

LOS:

The LOS bit indicates the current state of the Loss-Of-Signal detector. When LOS is logic 1, the E3-FRMR has received 32 consecutive RCLK cycles with no occurrences of bipolar data on RPOS and RNEG. When LOS is logic 0, the FRMR is receiving valid bipolar data. When the E3-FRMR has declared loss of signal, the LOS indication is set to logic 0 (de-asserted) when the E3-FRMR has received 32 consecutive RCLK cycles containing no occurrences of 4 consecutive zeros. The LOS bit is forced to logic 0 if the UNI bit is logic 1. During reset, LOS is set to logic 0, but the setting may change prior to the register being read.

OOFI:

A logic 1 OOFI bit indicates a change in the OOF status. The OOFI bit is cleared to logic 0 upon the completion of the register read. When OOFI is

logic 0, it indicates that no OOF state change has occurred since the last time this register was read.

COFAI:

The COFAI bit indicates that a change of frame alignment between the previous alignment and the newly found alignment has occurred. When COFAI is logic 1, the last high-to-low transition on the OOF signal resulted in the new frame alignment differing from the previous one. The COFAI bit is cleared to logic 0 upon the completion of the register read. When COFAI is logic 0, it indicates that no change in frame alignment has occurred when OOF went low.

LCVI:

The LCVI bit indicates that a line code violation has occurred. When LCVI is logic 1, a line code violation on the RPOS and RNEG inputs was detected since the last time this register was read. The LCVI bit is cleared to logic 0 upon the completion of the register read. When LCVI is logic 0, it indicates that no line code violation was detected since the last register read. When the UNI bit in the Framing Options register is logic 1, the LCVI is forced to logic 0.

LOSI:

The LOSI bit indicates that a state transition occurred on the LOS status signal. When LOSI is logic 1, a high-to-low or low-to-high transition occurred on the LOS status signal since the last time this register was read. The LOSI bit is cleared to logic 0 upon the completion of the register read. When LOSI is logic 0, it indicates that no state change has occurred on LOS since the last time this register was read. When the UNI bit in the Framing Options register is logic 1, the LOSI is forced to logic 0.

CZDI:

The CZDI bit indicates that four consecutive zeros in the HDB3-encoded stream have been detected. CZDI is asserted to a logic 1, whenever the CZD signal is asserted. The CZDI bit is cleared to a logic 0 upon the completion of the register read. When CZDI is logic 0, it indicates that no occurrences of four consecutive zeros was detected since the last register read. When the UNI bit in the Framing Options register is logic 1, the CZDI indication is forced to logic 0.

The interrupt indications within this register work independently from the interrupt enable bits, allowing the microprocessor to poll the register to determine the state of the framer. The indication bits (bits 2,3,4,5,6 of this register) are cleared

to logic 0 after the register is read; the INTB output is also cleared to logic 1 if the interrupt was generated by any of these five events.

Register 03CH, 13CH, 23CH, 33CH: E3 FRMR Maintenance Event Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	FERRE	0
Bit 6	R/W	PERRE	0
Bit 5	R/W	AISDE	0
Bit 4	R/W	FERFE	0
Bit 3	R/W	FEBEE	0
Bit 2	R/W	PTYPEE	0
Bit 1	R/W	TIMEMKE	0
Bit 0	R/W	NATUSEE	0

NATUSEE:

The NATUSEE bit is an interrupt enable. When NATUSEE is logic 1, an interrupt is generated on the INTB output when the National Use bit (bit 12 of the frame in G.751 E3 mode) changes state. When NATUSEE is logic 0, changes in state of the National Use bit does not cause an interrupt on INTB.

TIMEMKE:

The TIMEMKE bit is an interrupt enable. When TIMEMKE is logic 1, an interrupt is generated on the INTB output when the Timing Marker bit (bit 8 of the G.832 Maintenance and Adaptation byte) changes state after the selected persistency check is applied. When TIMEMKE is logic 0, changes in state of the Timing Marker bit does not cause an interrupt on INTB.

PTYPEE:

The PTYPEE bit is an interrupt enable. When PTYPEE is logic 1, an interrupt is generated on the INTB output when the Payload Type bits (bits 3,4,5 of the G.832 Maintenance and Adaptation byte) change state. When PTYPEE is logic 0, changes in state of the Payload Type bits does not cause an interrupt on INTB.

FEBEE:

The FEBEE bit is an interrupt enable. When FEBEE is logic 1, an interrupt is generated on the INTB output when the Far End Block Error indication bit (bit 2 of the G.832 Maintenance and Adaptation byte) changes state. When

FEBEE is logic 0, changes in state of the FEBE bit does not cause an interrupt on INTB.

FERFE:

The FERFE bit is an interrupt enable. When FERFE is logic 1, an interrupt is generated on the INTB output when the Far End Receive Failure indication bit (bit 1 of the G.832 Maintenance and Adaptation byte), or when the Remote Alarm indication bit (bit 11 of the frame in G.751) changes state after the selected persistency check is applied. When FERFE is logic 0, changes in state of the FERF or RAI bit does not cause an interrupt on INTB.

AISDE:

The AISDE bit is an interrupt enable. When AISDE is logic 1, an interrupt is generated on the INTB output when the AISD indication changes state. When AISDE is logic 0, changes in state of the AISD signal does not cause an interrupt on INTB.

PERRE:

The PERRE bit is an interrupt enable. When PERRE is logic 1, an interrupt is generated on the INTB output when a BIP-8 error (in G.832 mode) is detected. When PERRE is logic 0, occurrences of BIP-8 errors do not cause an interrupt on INTB.

FERRE:

The FERRE bit is an interrupt enable. When FERRE is logic 1, an interrupt is generated on the INTB output when a framing bit error is detected. When FERRE is logic 0, occurrences of framing bit errors do not cause an interrupt on INTB.

Register 03DH, 13DH, 23DH, 33DH: E3 FRMR Maintenance Event Interrupt Indication

Bit	Type	Function	Default
Bit 7	R	FERRI	0
Bit 6	R	PERRI	0
Bit 5	R	AISDI	0
Bit 4	R	FERFI	0
Bit 3	R	FEBEI	0
Bit 2	R	PTYPEI	0
Bit 1	R	TIMEMKI	0
Bit 0	R	NATUSEI	0

NATUSEI:

The NATUSEI bit is a transition Indication. When NATUSEI is logic 1, a change of state of the National Use bit (bit 12 of the frame in G.751 E3 mode) has occurred. When NATUSEI is logic 0, no change of state of the National Use bit has occurred since the last time this register was read.

TIMEMKI:

The TIMEMKI bit is a transition indication. When TIMEMKI is logic 1, a change in state of the Timing Marker bit (bit 8 of the G.832 Maintenance and Adaptation byte) has occurred. When TIMEMKI is logic 0, no changes in the state of the Timing Marker bit occurred since the last time this register was read.

PTYPEI:

The PTYPEI bit is a transition indication. When PTYPEI is logic 1, a change of state of the Payload Type bits (bits 3,4,5 of the G.832 Maintenance and Adaptation byte) has occurred. When PTYPEI is logic 0, no changes in the state of the Payload Type bits has occurred since the last time this register was read.

FEBEI:

The FEBEI bit is a transition indication. When FEBEI is logic 1, a change of state of the Far End Block Error indication bit (bit 2 of the G.832 Maintenance and Adaptation byte) has occurred. When FEBEI is logic 0, no changes in

the state of the FEBE bit has occurred since the last time this register was read.

FERFI:

The FERFI bit is a transition indication. When FERFI is logic 1, a change of state of the Far End Receive Failure indication bit (bit 1 of the G.832 Maintenance and Adaptation byte), or when the Remote Alarm indication bit (bit 12 of the frame in G.751) has occurred. When FERFI is logic 0, no changes in the state of the FERF or RAI bit has occurred since the last time this register was read.

AISDI:

The AISDI bit is a transition indication. When AISDI is logic 1, a change in state of the AISD indication has occurred. When AISDI is logic 0, no changes in the state of the AISD signal has occurred since the last time this register was read.

PERRI:

The PERRI bit is an event indication. When PERRI is logic 1, the occurrence of one or more BIP-8 errors (in G.832 mode) has been detected. When PERRI is logic 0, no occurrences of BIP-8 errors have occurred since the last time this register was read.

FERRI:

The FERRI bit is an event indication. When FERRI is logic 1, the occurrence of one or more framing bit error has been detected. When FERRI is logic 0, no occurrences of framing bit errors have occurred since the last time this register was read.

The transition/event interrupt indications within this register work independently from the interrupt enable bits, allowing the microprocessor to poll the register to determine the activity of the maintenance events. The contents of this register are cleared to logic 0 after the register is read; the INTB output is also cleared to logic 1 if the interrupt was generated by any of the Maintenance Event outputs.

Register 03EH, 13EH, 23EH, 33EH: E3 FRMR Maintenance Event Status

Bit	Type	Function	Default
Bit 7	R	AISD	X
Bit 6	R	FERF/RAI	X
Bit 5	R	FEBE	X
Bit 4	R	PTYPE[2]	X
Bit 3	R	PTYPE[1]	X
Bit 2	R	PTYPE[0]	X
Bit 1	R	TIMEMK	X
Bit 0	R	NATUSE	X

NATUSE:

The NATUSE bit reflects the state of the extracted National Use bit (bit 12 of the frame in G.751 E3 mode).

TIMEMK:

The TIMEMK bit reflects the state of the Timing Marker bit (bit 8 of the G.832 Maintenance and Adaptation byte).

PTYPE[2:0]:

The PTYPE[2:0] bits reflect the state of the Payload Type bits (bits 3,4,5 of the G.832 Maintenance and Adaptation byte). These bits are not latched and should be read 2 or 3 times in rapid succession to ensure a coherent binary value.

FEBE:

The FEBE bit reflects the state of the Far End Block Error indication bit (bit 2 of the G.832 Maintenance and Adaptation byte).

FERF:

The FERF bit reflects the value of the Far End Receive Failure indication bit (bit 1 of the G.832 Maintenance and Adaptation byte), or the value of the Remote Alarm indication bit (bit 11 of the frame in G.751) when the value has been the same for either 3 or 5 consecutive frames.

AISD:

The AISD bit reflects the state of the AIS detection circuitry. When AISD is logic 1, less than 8 zeros (in G.832 mode), or less than 5 zeros (in G.751 mode), were detected during one complete frame period while the FRMR is out of frame alignment. When AISD is logic 0, 8 or more zeros (in G.832 mode), or 5 or more zeros (in G.751 mode), were detected during one complete frame period, or the FRMR has found frame alignment.

Register 040H, 140H, 240H, 340H: E3 TRAN Framing Options

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	FORMAT[1]	0
Bit 0	R/W	FORMAT[0]	0

FORMAT[1:0]:

The FORMAT[1:0] bits determine the framing mode used for framing pattern when generating the formatted output data stream. The FORMAT[1:0] bits select one of two framing formats:

Table 13 - E3 TRAN FORMAT[1:0] Configurations

FORMAT[1]	FORMAT[0]	Framing Format Selected
0	0	G.751 E3 format
0	1	G.832 E3 format
1	0	Reserved
1	1	Reserved

Reserved:

The Reserved bits must be programmed to logic 0 for correct operation.

Register 041H, 141H, 241H, 341H: E3 TRAN Status and Diagnostic Options

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	PYLD&JUST	0
Bit 5	R/W	CPERR	0
Bit 4	R/W	DFERR	0
Bit 3	R/W	DLCV	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	TAIS	0
Bit 0	R/W	NATUSE	1

NATUSE:

The NATUSE bit determines the default value of the National Use bit inserted into the G.751 E3 frame overhead. The value of the NATUSE bit is logically ORed with the bit collected once per frame from the internal HDLC transmitter (if TNETOP is set to logic 1). When TNETOP is logic 0, the NATUSE bit controls the value of the National Use bit. When NATUSE is logic 1, the National Use bit (bit 12 in G.751) is forced to logic 1 regardless of the bit input from the internal HDLC transmitter or the setting of TNETOP. When NATUSE is logic 0, the National Use bit is set to the value sampled from the internal HDLC transmitter if TNETOP is logic 0. Otherwise, the National Use bit will be set to logic 0. If the E3 TRAN is configured for G.832 mode, this bit is ignored.

TAIS:

The TAIS bit enables AIS signal transmission. When TAIS is logic 1, the all 1's AIS signal is transmitted. When TAIS is logic 0, the normal data is transmitted.

Reserved:

The Reserved bit must be programmed to logic 0 for proper operation.

DLCV:

The DLCV bit selects whether a line code violation is generated for diagnostic purposes. When DLCV changes from logic 0 to logic 1, single LCV is generated; in HDB3, the LCV is generated by causing a bipolar violation

pulse of the same polarity to the previous bipolar violation. To generate another LCV, the DLCV register bit must be first be written to logic 0 and then to logic 1 again.

DFERR:

The DFERR bit selects whether the framing pattern is corrupted for diagnostic purposes. When DFERR is logic 1, the framing pattern inserted into the output data stream is inverted. When DFERR is logic 0, the unaltered framing pattern inserted into the output data stream.

CPERR:

The CPERR bit enables continuous generation of BIP-8 errors for diagnostic purposes. When CPERR is logic 1, the calculated BIP-8 value is continuously inverted according to the error mask specified by the BIP-8 Error Mask register and inserted into the G.832 EM byte. When CPERR is logic 0, the calculated BIP-8 value is altered only once, according to the error mask specified by the BIP-8 Error Mask register, and inserted into the EM byte.

PYLD&JUST:

The PYLD&JUST bit selects whether the justification service bits and the tributary justification bits in framing modes G.751 is indicated as overhead or payload. When PYLD&JUST is logic 1, the justification service bits and the tributary justification bits are indicated as payload. When PYLD&JUST is logic 0, the justification service and tributary justification bits are indicated as overhead. For G.751 ATM applications, this bit must be set to logic 1 for correct cell mapping.

Register 042H, 142H, 242H, 342H: E3 TRAN BIP-8 Error Mask

Bit	Type	Function	Default
Bit 7	R/W	MBIP[7]	0
Bit 6	R/W	MBIP[6]	0
Bit 5	R/W	MBIP[5]	0
Bit 4	R/W	MBIP[4]	0
Bit 3	R/W	MBIP[3]	0
Bit 2	R/W	MBIP[2]	0
Bit 1	R/W	MBIP[1]	0
Bit 0	R/W	MBIP[0]	0

MBIP[7:0]:

The MBIP[7:0] bits act as an error mask to cause the transmitter to insert up to 8 BIP-8 errors. The contents of this register are XORed with the calculated BIP-8 byte and inserted into the G.832 EM byte of the frame. A logic 1 in any MBIP bit position causes that bit position in the EM byte to be inverted. Writing this register with a mask value causes that mask to be applied only once; if continuous BIP-8 errors are desired, the CPERR bit in the Status and Diagnostic Options register can be used.

Register 043H, 143H, 243H, 343H: E3 TRAN Maintenance and Adaptation Options

Bit	Type	Function	Default
Bit 7	R/W	FERF/RAI	0
Bit 6	R/W	FEBE	0
Bit 5	R/W	PTYPE[2]	0
Bit 4	R/W	PTYPE[1]	0
Bit 3	R/W	PTYPE[0]	0
Bit 2	R/W	TUMFRM[1]	0
Bit 1	R/W	TUMFRM[0]	0
Bit 0	R/W	TIMEMK	0

TIMEMK:

The TIMEMK bit determines the state of the Timing Marker bit (bit 8 of the G.832 Maintenance and Adaptation byte). When TIMEMK is set to logic 1, the Timing Marker bit in the MA byte is set to logic 1. When TIMEMK is set to logic 0, the Timing Marker bit in the MA byte is set to logic 0.

TUMFRM[1:0]:

The TUMFRM[1:0] bits reflect the value to be inserted in the Tributary Unit Multiframe bits (bits 6, and 7 of the G.832 Maintenance and Adaptation byte). These bits are logically ORed with the TUMFRM[1:0] overhead signals from the TOH input before being inserted in the MA byte.

PTYPE[2:0]:

The PTYPE[2:0] bits reflect the value to be inserted in the Payload Type bits (bits 3,4,5 of the G.832 Maintenance and Adaptation byte).

FEBE:

The FEBE bit reflects the value to be inserted in the Far End Block Error indication bit (bit 2 of the G.832 Maintenance and Adaptation byte). The FEBE bit value is logically ORed with the FEBE indications generated by the FRMR for any detected BIP-8 errors. When the FEBE bit is logic 1, bit 2 of the G.832 MA byte is set to logic 1; when the FEBE bit is logic 0, any BIP-8 error indications from the FRMR causes bit 2 of the MA byte to be set to logic 1.

FERF/RAI:

The FERF/RAI bit reflects the value to be inserted in the Far End Receive Failure indication bit (bit 1 of the G.832 Maintenance and Adaptation byte), or the value of the Remote Alarm indication bit (bit 11 of the frame in G.751). The FERF/RAI bit is logically ORed with the LOS, OOF, AIS, and LCD indications from the E3 FRMR and RXCP-50 when the LOSEN, OOFEN, AISEN, and LCDEN register bits (in the S/UNI-QJET Data Link and FERF/RAI Control register) are set to logic 1 respectively. When the OR of the two signals is logic 1, the FERF or RAI bit in the frame is set to logic 1; when neither signal is logic 1, the FERF or RAI bit is set to logic 0.

Register 044H, 144H, 244H, 344H: J2-FRMR Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	UNI	0
Bit 5	R/W	REFRAME	0
Bit 4	R/W	FLOCK	0
Bit 3	R/W	CRC_REFR	0
Bit 2	R/W	SFRME	0
Bit 1	R/W	LOSTHR[1]	1
Bit 0	R/W	LOSTHR[0]	1

UNI:

When the UNI bit is set to logic 0, the J2-FRMR expects unipolar data on the RDATI input and line code violation indications on the RLCV input. When UNI is logic 0, the J2-FRMR expects bipolar B8ZS encoded data on the RPOS and RNEG inputs. When UNI is set to logic 1, then the LOS, LOSI, and EXZI indications cannot be used.

REFRAME:

Writing the REFRAME bit logic 1 forces the J2-FRMR to declare loss of frame, and begin searching for a new alignment. In order to force another reframe, REFRAME must be written with logic 0, and then logic 1 again.

FLOCK:

When the FLOCK bit is set to logic 1, the J2-FRMR is prevented from declaring Loss of Frame and searching for a new frame alignment due to framing-pattern errors. In this case, the J2-FRMR will only search for frame alignment when the REFRAME register bit transitions from logic 0 to logic 1.

CRC_REFR

When the CRC Reframe Enable bit is set to logic 1, an alternate framing algorithm is enabled, which uses the CRC-5 check to detect framing to a mimic pattern in the payload or signaling bits. The framer, once it has seen at least one correct framing pattern, begins looking for correct CRC-5s as well. If it observes three consecutive correct framing patterns, and two correct CRC-5 sequences, then frame is declared. Otherwise, a reframe is initiated.

When CRC_REFR is set to logic 0, the framing algorithm simply searches for three consecutive correct framing patterns.

SFRME

When the Single Framing Bit Error (SFRME) bit is set to logic 1, then the J2-FRMR will indicate (to the PMON) a single framing error for every J2 multi-frame which contains one or more framing errors. When the SFRME bit is set to logic 0, the J2-FRMR will identify every framing error to the PMON.

LOSTHR[1:0]

The Loss of Signal Threshold bits select the number of consecutive zeroes required before the J2-FRMR will declare Loss of Signal (LOS), and the number of bit periods without an occurrence of excess zeroes that must pass before the J2-FRMR will de-assert Loss of Signal. The thresholds are as follows:

Table 14 - J2 FRMR LOS Threshold Configurations

LOSTHR[1]	LOSTHR[0]	Threshold
0	0	15
0	1	31
1	0	63
1	1	255

Thus, if LOSTHR[1:0] = 11 binary, LOS will be declared after the 255th consecutive binary zero, and de-asserted when 255 bit periods have passed without an occurrence of a string of eight or more consecutive zeroes.

Register 045H, 145H, 245H, 345H: J2-FRMR Status

Bit	Type	Function	Default
Bit 7	R	LOS	X
Bit 6	R	LOF	X
Bit 5		Unused	X
Bit 4	R	RAI	X
Bit 3	R	RLOF	X
Bit 2		Unused	X
Bit 1	R	PHYAIS	X
Bit 0	R	PLDAIS	X

LOS, LOF, RAI, RLOF, PHYAIS, PLDAIS

These register bits reflect the current state of the Loss of Signal (LOS), Loss of Frame (LOF), Remote Alarm Indication (RAI), Remote Loss of Frame (RLOF, also known as the a-bit), Physical AIS (PHYAIS), and Payload AIS (PLDAIS) conditions.

Register 046H, 146H, 246H, 346H: J2-FRMR Alarm Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	LOSE	0
Bit 6	R/W	LOFE	0
Bit 5	R/W	COFAE	0
Bit 4	R/W	RAIE	0
Bit 3	R/W	RLOFE	0
Bit 2	R/W	RLOF_THR	1
Bit 1	R/W	PHYAISE	0
Bit 0	R/W	PLDAISE	0

LOSE

When LOSE is logic 1, the J2-FRMR will generate an interrupt when the LOS condition changes state. Note that the LOS bit is not valid when the UNI bit is set in the J2-FRMR Configuration Register.

LOFE

When LOFE is logic 1, the J2-FRMR will generate an interrupt when LOF changes state.

COFAE

When COFAE is logic 1, the J2-FRMR will generate an interrupt when a change of frame alignment occurs.

RAIE

When RAIE is logic 1, the J2-FRMR will generate an interrupt when RAI changes state.

RLOFE

When RLOFE is logic 1, the J2-FRMR will generate an interrupt when RLOF changes state.

RLOF_THR

The RLOF Threshold bit determines the number of consecutive a-bits that are required for the state of RLOF to change. When RLOF_THR is logic 0, RLOF

is asserted when the a-bit has been logic 1 for three consecutive frames, and de-asserted when the a-bit has been logic 0 for three consecutive frames. When RLOF_THR is logic 1, RLOF is asserted when the a-bit has been logic 1 for five consecutive frames, and de-asserted when the a-bit has been logic 0 for five consecutive frames. The default setting is that five consecutive a-bits are required.

PHYAISE

When PHYAISE is logic 1, the J2-FRMR will generate an interrupt when a change is detected in the Physical AIS condition.

PLDAISE

When PLDAISE is logic 1, the J2-FRMR will generate an interrupt when a change is detected in the Payload AIS condition.

Register 047H, 147H, 247H, 347H: J2-FRMR Alarm Interrupt Status

Bit	Type	Function	Default
Bit 7	R	LOSI	X
Bit 6	R	LOFI	X
Bit 5	R	COFAI	X
Bit 4	R	RAII	X
Bit 3	R	RLOFI	X
Bit 2		Unused	X
Bit 1	R	PHYAISI	X
Bit 0	R	PLDAISI	X

LOSI

The LOSI bit is set to logic 1 if a change occurs in the LOS condition. LOSI is cleared when this register is read.

LOFI

The LOFI bit is set to logic 1 if a change occurs in the state of LOF. LOFI is cleared when this register is read.

COFAI

The COFAI bit is set to logic 1 if a change in frame alignment occurs. COFAI is cleared when this register is read.

RAII

The RAII bit is set to logic 1 if a change in the value of RAI occurs. RAII is cleared when this register is read.

RLOFI

The RLOFI bit is set to logic 1 if a change in the value of RLOF occurs. RLOFI is cleared when this register is read.

PHYAISI

The PHYAISI bit is set to logic 1 if a change in the condition of PHYAIS occurs. PHYAISI is cleared when this register is read.

PLDAISI

The PLDAISI bit is set to logic 1 if a change in the condition of PLDAIS occurs. PLDAISI is cleared when this register is read.

Register 048H, 148H, 248H, 348H: J2-FRMR Error/Xbit Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	CRCEE	0
Bit 6	R/W	FRMEE	0
Bit 5	R/W	BPVE	0
Bit 4	R/W	EXZE	0
Bit 3	R/W	XBITE	0
Bit 2		Unused	X
Bit 1	R/W	XBIT_DEB	0
Bit 0	R/W	XBIT_THR	0

CRCEE

When CRCEE is logic 1, the J2-FRMR will generate an interrupt if a multiframe fails its CRC-5 check.

FRMEE

When FRMEE is logic 1, the J2-FRMR will generate an interrupt upon the reception of an errored framing bit.

BPVE

When BPVE is logic 1, the J2-FRMR will generate an interrupt upon the reception of a bipolar violation which is not part of a valid B8ZS code (when UNI is set to logic 0 in the J2-FRMR Configuration Register) or on the reception of a logic 1 on RLCV (when UNI is set to logic 1).

EXZE

When EXZE is logic 1, the J2-FRMR will generate an interrupt upon the reception of a string of eight-or-more consecutive zeroes. EXZE has no effect when UNI is set to logic 1 in the J2-FRMR Configuration Register.

XBITE

When XBITE is logic 1, the J2-FRMR will generate an interrupt when any of the x-bits (X1, X2, X3) change state. Because the XBIT interrupt is generated when the x-bit indications change, the interrupt is debounced along with them via the XBIT_DEB and XBIT_THR bits.

XBIT_DEB

When XBIT_DEB is set to logic 0, the x-bit indications in the J2-FRMR Error/Xbit Interrupt Status Register reflect the most recent value of the x-bits. When XBIT_DEB is set to logic 1, the x-bit indications change value only when an x-bit has maintained its value for 3 or 5 consecutive multiframes, depending on the setting of XBIT_THR.

XBIT_THR

When XBIT_THR is set to logic 1, then XBIT_THR controls the debouncing threshold of the x-bit indications in the J2-FRMR Error/Xbit Interrupt Status Register. When XBIT_THR is logic 0, the threshold is set to 3 consecutive multiframes; when XBIT_THR is logic 1, the threshold is set to 5 consecutive multiframes.

Register 049H, 149H, 249H, 349H: J2-FRMR Error/Xbit Interrupt Status

Bit	Type	Function	Default
Bit 7	R	CRCEI	X
Bit 6	R	FRMEI	X
Bit 5	R	BPVI	X
Bit 4	R	EXZI	X
Bit 3	R	XBITI	X
Bit 2	R	X3	X
Bit 1	R	X2	X
Bit 0	R	X1	X

CRCEI

The CRCEI bit is set to logic 1 if a failed CRC-5 check occurs. CRCEI is cleared when this register is read.

FRMEI

The FRMEI bit is set to logic 1 if an errored framing bit occurs. FRMEI is cleared when this register is read.

BPVI

The BPVI bit is set to logic 1 if a bipolar violation that is not part of a valid B8ZS code occurs (when UNI is logic 0 in the J2-FRMR Configuration Register) or if a 0 to 1 transition is detected on RLCV (when UNI is logic 1). BPVI is cleared when this register is read.

EXZI

The EXZI bit is set to logic 1 upon reception of eight-or-more consecutive zeroes. EXZI remains logic 0 while UNI is set to logic 1 in the J2_FRMR Configuration Register. EXZI is cleared when this register is read.

XBITI

The XBITI bit is set to logic 1 if a change in the debounced (if XBIT_DEB is set to logic 1) x-bits (X1, X2, and X3) is detected. XBITI is cleared when this register is read.

X1, X2, X3:

The X1, X2, and X3 bits reflect the most recent (debounced if XBIT_DEB is set to logic 1) value of bits 785, 786, and 787 respectively of frame 3 of each multiframe. These bits are the spare or 'x-bits'

Register 04CH, 14CH, 24CH, 34CH: J2-TRAN Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	X3SET	1
Bit 2	R/W	X2SET	1
Bit 1	R/W	X1SET	1
Bit 0	R/W	RLOF	0

RLOF:

The RLOF bit controls the state of the A-bit. When RLOF is a logic 1, the A-bit is also set to logic 1. When RLOF is a logic 0, the A-bit is set to logic 0. The A-bit in the transmit stream may also be set to logic 1 if an LOF condition in the J2 FRMR is detected and the RBLEN bit is logic 1 in the S/UNI-QJET Data Link and FERF/RAI Control register.

X1SET:

The X1SET bit controls the state of the X1 bit (bit 785 in the third frame of a J2 multiframe). When X1SET is a logic 1, the X1 bit is set to logic 1. When X1SET is a logic 0, the X1 bit is set to logic 0.

X2SET:

The X2SET bit controls the state of the X2 bit (bit 786 in the third frame of a J2 multiframe). When X2SET is a logic 1, the X2 bit is set to logic 1. When X2SET is a logic 0, the X2 bit is set to logic 0.

X3SET:

The X3SET bit controls the state of the X3 bit (bit 787 in the third frame of a J2 multiframe). When X3SET is a logic 1, the X3 bit is set to logic 1. When X3SET is a logic 0, the X3 bit is set to logic 0.

Reserved:

The reserved register bits should be set to logic 0 for proper operation.

Register 04DH, 14DH, 24DH, 34DH: J2-TRAN Diagnostic

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	PLDAIS	0
Bit 4	R/W	PHYAIS	0
Bit 3	R/W	DCRC	0
Bit 2	R/W	DLOS	0
Bit 1	R/W	DBPV	0
Bit 0	R/W	DFERR	0

DFERR:

The DFERR bit controls the insertion of framing alignment signal errors. When DFERR is set to logic 1, the framing alignment signal is inverted. When DFERR is set to logic 0, the framing alignment signal is not inverted.

DBPV:

The DBPV bit controls the insertion of single bipolar violations. When DBPV bit transitions from 0 to 1, a violation is generated by masking the first violation pulse of a B8ZS signature. To generate another violation, this bit must first be written to 0 and then to logic 1 again. When DBPV is a logic 0, no violation is generated.

DLOS:

When set to logic 1, the DLOS bit forces the unipolar and bipolar outputs of the J2 TRAN to be all zeros. When DLOS is logic 0, the outputs of the J2 TRAN operate normally.

DCRC:

When set to logic 1, a the CRC-5 check bits (e_{1-5}) are inverted before transmission. DCRC inverts the e_{1-5} bits even if CDIS of the J2 TRAN Configuration register is set to logic 1.

PHYAIS:

When set to logic 1, PHYAIS will cause the J2 TRAN to transmit an all 1's Alarm Indication Signal (AIS).

PLDAIS:

When set to logic 1, PLDAIS will cause the J2 TRAN to insert all 1's in the payload data bits. When PLDAIS is a logic 0, data is processed normally through the J2 TRAN.

Register 04EH, 14EH, 24EH, 34EH: J2-TRAN TS97 Signaling

Bit	Type	Function	Default
Bit 7	R/W	TS97[1]	1
Bit 6	R/W	TS97[2]	1
Bit 5	R/W	TS97[3]	1
Bit 4	R/W	TS97[4]	1
Bit 3	R/W	TS97[5]	1
Bit 2	R/W	TS97[6]	1
Bit 1	R/W	TS97[7]	1
Bit 0	R/W	TS97[8]	1

TS97[1:8]:

The TS97[1:8] bits control what is inserted into the J2 timeslot 97 bits. TS97[1] is the first bit of timeslot 97 transmitted.

Register 04FH, 14FH, 24FH, 34FH: J2-TRAN TS98 Signaling

Bit	Type	Function	Default
Bit 7	R/W	TS98[1]	1
Bit 6	R/W	TS98[2]	1
Bit 5	R/W	TS98[3]	1
Bit 4	R/W	TS98[4]	1
Bit 3	R/W	TS98[5]	1
Bit 2	R/W	TS98[6]	1
Bit 1	R/W	TS98[7]	1
Bit 0	R/W	TS98[8]	1

TS98[1:8]:

The TS98[1:8] bits control what is inserted into the J2 timeslot 98 bits. TS98[1] is the first bit of timeslot 98 transmitted.

Register 050H, 150H, 250H,350H: RDLC Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	MEN	0
Bit 2	R/W	MM	0
Bit 1	R/W	TR	0
Bit 0	R/W	EN	0

EN:

The EN bit controls the overall operation of the RDLC. When EN is set to logic 1, RDLC is enabled; when set to logic 0, RDLC is disabled. When RDLC is disabled, the RDLC FIFO buffer and interrupts are all cleared. When RDLC is enabled, it will immediately begin looking for flags.

TR:

Setting the terminate reception (TR) bit to logic 1 forces the RDLC to immediately terminate the reception of the current data frame, empty the RDLC FIFO buffer, clear the interrupts, and begin searching for a new flag sequence. The RDLC handles a terminate reception event in the same manner as it would the toggling of the EN bit from logic 1 to logic 0 and back to logic 1. Thus, the RDLC state machine will begin searching for flags. An interrupt will be generated when the first flag is detected. The TR bit will reset itself to logic 0 after the register write operation is completed and a rising and falling edge occurs on the internal datalink clock input. If the RDLC Configuration Register is read after this time, the TR bit value returned will be logic 0.

MEN:

Setting the Match Enable (MEN) bit to logic 1 enables the detection and storage in the RDLC FIFO of only those packets whose first data byte matches either of the bytes written to the Primary or Secondary Match Address Registers, or the universal all ones address. When the MEN bit is logic 0, all packets received are written into the RDLC FIFO.

MM:

Setting the Match Mask (MM) bit to logic 1 ignores the PA[1:0] bits of the Primary Address Match Register, the SA[1:0] bits of the Secondary Address Match Register, and the two least significant bits of the universal all ones address when performing the address comparison.

Reserved:

This register bit should be set to logic 0 for proper operation.

Register 051H, 151H, 251H, 351H: RDLC Interrupt Control

Bit	Type	Function	Default
Bit 7	R/W	INTE	0
Bit 6	R/W	INTC[6]	0
Bit 5	R/W	INTC[5]	0
Bit 4	R/W	INTC[4]	0
Bit 3	R/W	INTC[3]	0
Bit 2	R/W	INTC[2]	0
Bit 1	R/W	INTC[1]	0
Bit 0	R/W	INTC[0]	0

INTC[6:0]:

The INTC[6:0] bits control the assertion of FIFO fill level set point interrupts. The value of INTC[6:0] = ‘b0000000 sets the interrupt FIFO fill level to 128.

INTE:

The Interrupt Enable bit (INTE) must set to logic 1 to allow the internal interrupt status to be propagated to the INTB output. When the INTE bit is logic 0 the RDLC will not assert INTB.

The contents of the Interrupt Control Register should only be changed when the EN bit in the RDLC Configuration Register is logic 0. This prevents any erroneous interrupt generation.

Register 052H, 152H, 252H, 352H: RDLC Status

Bit	Type	Function	Default
Bit 7	R	FE	X
Bit 6	R	OVR	X
Bit 5	R	COLS	X
Bit 4	R	PKIN	X
Bit 3	R	PBS[2]	X
Bit 2	R	PBS[1]	X
Bit 1	R	PBS[0]	X
Bit 0	R	INTR	X

Consecutive reads of the RDLC Status and Data registers should not occur at rates greater than 1/10 that of the clock selected by the LINESYSCLK bit of the S/UNI-QJET Misc. register (09BH, 19BH, 29BH, 39BH).

INTR:

The interrupt (INTR) bit reflects the status of the internal RDLC interrupt. If the INTE bit in the RDLC Interrupt Control Register is set to logic 1, a RDLC interrupt (INTR is a logic 1) will cause INTB to be asserted low. The INTR register bit will be set to logic 1 when one of the following conditions occurs:

1. the number of bytes specified in the RDLC Interrupt Control register have been received on the data link and written into the FIFO
2. RDLC FIFO buffer overrun has been detected
3. the last byte of a packet has been written into the RDLC FIFO
4. the last byte of an aborted packet has been written into the RDLC FIFO
5. transition of receiving all ones to receiving flags has been detected.

PBS[2:0]:

The packet byte status (PBS[2:0]) bits indicate the status of the data last read from the FIFO as indicated in the following table:

Table 15 - RDLC PBS[2:0] Data Status

PBS[2:0]	Data Status
000	The data byte read from the FIFO is not special.
001	The data byte read from the FIFO is the dummy byte that was written into the FIFO when the first HDLC flag sequence (01111110) was detected. This indicates that the data link became active.
010	The data byte read from the FIFO is the dummy byte that was written into the FIFO when the HDLC abort sequence (01111111) was detected. This indicates that the data link became inactive.
011	Unused.
100	The data byte read from the FIFO is the last byte of a normally terminated packet with no CRC error and the packet received had an integer number of bytes.
101	The data byte read from the FIFO must be discarded because there was a non-integer number of bytes in the packet.
110	The data byte read from the FIFO is the last byte of a normally terminated packet with a CRC error. The packet was received in error.
111	The data byte read from the FIFO is the last byte of a normally terminated packet with a CRC error and a non-integer number of bytes. The packet was received in error.

PKIN:

The Packet In (PKIN) bit is logic 1 when the last byte of a non-aborted packet is written into the FIFO. The PKIN bit is cleared to logic 0 after the RDLC Status Register is read.

COLS:

The Change of Link Status (COLS) bit is set to logic 1 if the RDLC has detected the HDLC flag sequence (01111110) or HDLC abort sequence (01111111) in the data. This indicates that there has been a change in the data link status. The COLS bit is cleared to logic 0 by reading this register or by clearing the EN bit in the RDLC Configuration Register. For each change in link status, a byte is written into the FIFO. If the COLS bit is found to be logic 1 then the RDLC FIFO must be read until empty. The status of the data

link is determined by the PBS[2:0] bits associated with the data read from the RDLC FIFO.

OVR:

The overrun (OVR) bit is set to logic 1 when data is written over unread data in the RDLC FIFO buffer. This bit is not reset to logic 0 until after the Status Register is read. While the OVR bit is logic 1, the RDLC and RDLC FIFO buffer are held in the reset state, causing the COLS and PKIN bits to be reset to logic 0.

FE:

The FIFO buffer empty (FE) bit is set to logic 1 when the last RDLC FIFO buffer entry is read. The FE bit goes to logic 0 when the FIFO is loaded with new data.

Register 053H, 153H, 253H, 353H: RDLC Data

Bit	Type	Function	Default
Bit 7	R	RD[7]	X
Bit 6	R	RD[6]	X
Bit 5	R	RD[5]	X
Bit 4	R	RD[4]	X
Bit 3	R	RD[3]	X
Bit 2	R	RD[2]	X
Bit 1	R	RD[1]	X
Bit 0	R	RD[0]	X

Consecutive reads of the RDLC Status and Data registers should not occur at rates greater than 1/10 that of the clock selected by the LINESYSCLK bit of the S/UNI-QJET Misc. register (09BH, 19BH, 29BH, 39BH).

RD[7:0]:

RD[7:0] contains the received data link information. RD[0] corresponds to the first received bit of the data link message.

This register reads from the RDLC 128-byte FIFO buffer. If data is available, the FE bit in the FIFO Input Status Register is logic 0.

When an overrun is detected, an interrupt is generated and the FIFO buffer is held cleared until the RDLC Status Register is read.

Register 054H, 154H, 254H, 354H: RDLC Primary Address Match

Bit	Type	Function	Default
Bit 7	R/W	PA[7]	1
Bit 6	R/W	PA[6]	1
Bit 5	R/W	PA[5]	1
Bit 4	R/W	PA[4]	1
Bit 3	R/W	PA[3]	1
Bit 2	R/W	PA[2]	1
Bit 1	R/W	PA[1]	1
Bit 0	R/W	PA[0]	1

PA[7:0]:

The first byte received after a flag character is compared against the contents of this register. If a match occurs, the packet data, including the matching first byte, is written into the FIFO. PA[0] corresponds to the first received bit of the data link message. The MM bit in the Configuration Register is used mask off PA[1:0] during the address comparison.

Register 055H, 155H, 255H, 355H: RDLC Secondary Address Match

Bit	Type	Function	Default
Bit 7	R/W	SA[7]	1
Bit 6	R/W	SA[6]	1
Bit 5	R/W	SA[5]	1
Bit 4	R/W	SA[4]	1
Bit 3	R/W	SA[3]	1
Bit 2	R/W	SA[2]	1
Bit 1	R/W	SA[1]	1
Bit 0	R/W	SA[0]	1

SA[7:0]:

The first byte received after a flag character is compared against the contents of this register. If a match occurs, the packet data, including the matching first byte, is written into the FIFO. SA[0] corresponds to the first received bit data link message. The MM bit in the Configuration Register is used mask off SA[1:0] during the address comparison.

Register 058H, 158H, 258H, 358H: TDPR Configuration

Bit	Type	Function	Default
Bit 7	R/W	FLGSHARE	1
Bit 6	R/W	FIFOCLR	0
Bit 5	R/W	Reserved	0
Bit 4		Unused	X
Bit 3	R/W	EOM	0
Bit 2	R/W	ABT	0
Bit 1	R/W	CRC	1
Bit 0	R/W	EN	0

Consecutive writes to the TDPR Configuration, TDPR Interrupt Status/UDR Clear, and TDPR Transmit Data register and reads of the TDPR Interrupt Status/UDR Clear register should not occur at rates greater than 1/8th that of the clock selected by the LINESYSCLK bit of the S/UNI-QJET Misc. register (09BH, 19BH, 29BH, 39BH).

EN:

The EN bit enables the TDPR functions. When EN is set to logic 1, the TDPR is enabled and flag sequences are sent until data is written into the TDPR Transmit Data register. When the EN bit is set to logic 0, the TDPR is disabled and an all 1's Idle sequence is transmitted on the datalink.

CRC:

The CRC enable bit controls the generation of the CCITT_CRC frame check sequence (FCS). Setting the CRC bit to logic 1 enables the CCITT-CRC generator and appends the 16-bit FCS to the end of each message. When the CRC bit is set to logic 0, the FCS is not appended to the end of the message. The CRC type used is the CCITT-CRC with generator polynomial $x^{16} + x^{12} + x^5 + 1$. The high order bit of the FCS word is transmitted first.

ABT:

The Abort (ABT) bit controls the sending of the 7 consecutive ones HDLC abort code. Setting the ABT bit to a logic 1 causes the 01111111 code (the 0 is transmitted first) to be transmitted after the current byte from the TDPR FIFO is transmitted. The TDPR FIFO is then reset. All data in the TDPR

FIFO will be lost. Aborts are continuously sent and the FIFO is held in reset until this bit is reset to a logic 0. At least one Abort sequence will be sent when the ABT bit transitions from logic 0 to logic 1.

EOM:

The EOM bit indicates that the last byte of data written in the Transmit Data register is the end of the present data packet. If the CRC bit is set then the 16-bit FCS word is appended to the last data byte transmitted and a continuous stream of flags is generated. The EOM bit is automatically cleared upon a write to the TDPR Transmit Data register.

Reserved:

This bit should be set to logic 0 for proper operation.

FIFOCLR:

The FIFOCLR bit resets the TDPR FIFO. When set to logic 1, FIFOCLR will cause the TDPR FIFO to be cleared.

FLGSHARE:

The FLGSHARE bit configures the TDPR to share the opening and closing flags between successive frames. If FLGSHARE is logic 1, then the opening and closing flags between successive frames are shared. If FLGSHARE is logic 0, then separate closing and opening flags are inserted between successive frames.

Register 059H, 159H, 259H, 359H: TDPR Upper Transmit Threshold

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	UTHR[6]	1
Bit 5	R/W	UTHR[5]	0
Bit 4	R/W	UTHR[4]	0
Bit 3	R/W	UTHR[3]	0
Bit 2	R/W	UTHR[2]	0
Bit 1	R/W	UTHR[1]	0
Bit 0	R/W	UTHR[0]	0

UTHR[6:0]:

The UTHR[6:0] bits define the TDPR FIFO fill level which will automatically cause the bytes stored in the TDPR FIFO to be transmitted. Once the fill level exceeds the UTHR[6:0] value, transmission will begin. Transmission will not stop until the last complete packet is transmitted and the TDPR FIFO fill level is below UTHR[6:0] + 1.

The value of UTHR[6:0] must always be greater than the value of LINT[6:0] unless both values are equal to 00H.

Register 05AH, 15AH, 25AH, 35AH: TDPR Lower Interrupt Threshold

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	LINT[6]	0
Bit 5	R/W	LINT[5]	0
Bit 4	R/W	LINT[4]	0
Bit 3	R/W	LINT[3]	0
Bit 2	R/W	LINT[2]	1
Bit 1	R/W	LINT[1]	1
Bit 0	R/W	LINT[0]	1

LINT[6:0]:

The LINT[6:0] bits define the TDPR FIFO fill level which causes an internal interrupt (LFILLI) to be generated. Once the TDPR FIFO level decrements to empty or to a value less than LINT[6:0], LFILLI and BLFILL register bits will be set to logic 1. LFILLI will cause an interrupt on INTB if LFILLE is set to logic 1.

The value of LINT[6:0] must always be less than the value of UTHR[6:0] unless both values are equal to 00H.

Register 05BH, 15BH, 25BH, 35BH: TDPR Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	FULLE	0
Bit 2	R/W	OVRE	0
Bit 1	R/W	UDRE	0
Bit 0	R/W	LFILLE	0

LFILLE:

The LFILLE enables a transition to logic 1 on LFILLI to generate an interrupt on INTB. If LFILLE is a logic 1, a transition to logic 1 on LFILLI will generate an interrupt on INTB. If LFILLE is a logic 0, a transition to logic 1 on LFILLI will not generate an interrupt on INTB.

UDRE:

The UDRE enables a transition to logic 1 on UDRI to generate an interrupt on INTB. If UDRE is a logic 1, a transition to logic 1 on UDRI will generate an interrupt on INTB. If UDRE is a logic 0, a transition to logic 1 on UDRI will not generate an interrupt on INTB.

OVRE:

The OVRE enables a transition to logic 1 on OVRI to generate an interrupt on INTB. If OVRE is a logic 1, a transition to logic 1 on OVRI will generate an interrupt on INTB. If OVRE is a logic 0, a transition to logic 1 on OVRI will not generate an interrupt on INTB.

FULLE:

The FULLE enables a transition to logic 1 on FULLI to generate an interrupt on INTB. If FULLE is a logic 1, a transition to logic 1 on FULLI will generate an interrupt on INTB. If FULLE is a logic 0, a transition to logic 1 on FULLI will not generate an interrupt on INTB.

Reserved:

This bit should be set to logic 0 for proper operation.

Register 05CH, 15CH, 25CH, 35CH: TDPR Interrupt Status/UDR Clear

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	FULL	X
Bit 5	R	BLFILL	X
Bit 4	R	Unused	X
Bit 3	R	FULLI	X
Bit 2	R	OVRI	X
Bit 1	R	UDRI	X
Bit 0	R	LFILLI	X

Consecutive writes to the TDPR Configuration, TDPR Interrupt Status/UDR Clear, and TDPR Transmit Data register and reads of the TDPR Interrupt Status/UDR Clear register should not occur at rates greater than 1/8th that of the clock selected by the LINESYSCLK bit of the S/UNI-QJET Misc. register (09BH, 19BH, 29BH, 39BH).

LFILLI:

The LFILLI bit will transition to logic 1 when the TDPR FIFO level transitions to empty or falls below the value of LINT[6:0] programmed in the TDPR Lower Interrupt Threshold register. LFILLI will assert INTB if it is a logic 1 and LFILLE is programmed to logic 1. LFILLI is cleared when this register is read.

UDRI:

The UDRI bit will transition to 1 when the TDPR FIFO underruns. That is, the TDPR was in the process of transmitting a packet when it ran out of data to transmit. UDRI will assert INTB if it is a logic 1 and UDRE is programmed to logic 1. UDRI is cleared when this register is read.

OVRI:

The OVRI bit will transition to 1 when the TDPR FIFO overruns. That is, the TDPR FIFO was already full when another data byte was written to the TDPR Transmit Data register. OVRI will assert INTB if it is a logic 1 and OVRE is programmed to logic 1. OVRI is cleared when this register is read.

FULLI:

The FULLI bit will transition to logic 1 when the TDPR FIFO is full. FULLI will assert INTB if it is a logic 1 and FULLE is programmed to logic 1. FULLI is cleared when this register is read.

BLFILL:

The BLFILL bit is set to logic 1 if the current FIFO fill level is below the LINT[7:0] level or is empty.

FULL:

The FULL bit reflects the current condition of the TDPR FIFO. If FULL is a logic 1, the TDPR FIFO already contains 128-bytes of data and can accept no more.

Register 05DH, 15DH, 25DH, 35DH: TDPR Transmit Data

Bit	Type	Function	Default
Bit 7	R/W	TD[7]	X
Bit 6	R/W	TD[6]	X
Bit 5	R/W	TD[5]	X
Bit 4	R/W	TD[4]	X
Bit 3	R/W	TD[3]	X
Bit 2	R/W	TD[2]	X
Bit 1	R/W	TD[1]	X
Bit 0	R/W	TD[0]	X

Consecutive writes to the TDPR Configuration, TDPR Interrupt Status/UDR Clear, and TDPR Transmit Data register and reads of the TDPR Interrupt Status/UDR Clear register should not occur at rates greater than 1/8th that of the clock selected by the LINESYSCLK bit of the S/UNI-QJET Misc. register (09BH, 19BH, 29BH, 39BH).

TD[7:0]:

The TD[7:0] bits contain the data to be transmitted on the data link. Data written to this register is serialized and transmitted (TD[0] is transmitted first).

Register 060H, 160H, 260H, 360H: RXCP-50 Configuration 1

Bit	Type	Function	Default
Bit 7	R/W	DDSCR	0
Bit 6	R/W	HDSCR	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	HCSADD	1
Bit 1	R/W	HCSDQDB	0
Bit 0	R/W	DISCOR	0

DISCOR:

The DISCOR bit controls the HCS error correction algorithm. When DISCOR is a logic 0, the error correction algorithm is enabled, and single-bit errors detected in the cell header are corrected. When DISCOR is a logic 1, the error correction algorithm is disabled, and any error detected in the cell header is treated as an uncorrectable HCS error.

HCSDQDB:

The HCSDQDB bit enables HCS checking for either ATM type cells or DQDB type cells. When logic 0, ATM type cells are processed by checking all 4 octets in the header for HCS validation. When logic 1, DQDB cells are processed by checking only 3 of the header octets (octets 2, 3 and 4) for HCS validation.

HCSADD:

The HCSADD bit controls the addition of the coset polynomial, $x^6+x^4+x^2+1$, to the HCS octet prior to comparison. When HCSADD is a logic 1, the polynomial is added, and the resulting HCS is compared. When HCSADD is a logic 0, the polynomial is not added, and the unmodified HCS is compared.

HDSCR:

HDSCR enables the self-synchronous $x^{43} + 1$ descrambler to continue running through the bytes which should contain the ATM cell headers. When HDSCR is set to logic 0, the descrambling polynomial will function only over the ATM payload bytes. When HDSCR is set to logic 1, the descrambling

polynomial will function over all bytes, including the 5 ATM header bytes. This function is available for use with PPP packets and flags which are scrambled at the source to prevent the generation of "killer" sequences.

DDSCR:

The DDSCR bit controls the descrambling of the cell payload with the polynomial $x^{43} + 1$. When DDSCR is set to logic 1, cell payload descrambling is disabled. When DDSCR is set to logic 0, payload descrambling is enabled.

Register 061H, 161H, 261H, 361H: RXCP-50 Configuration 2

Bit	Type	Function	Default
Bit 7	R/W	CCDIS	0
Bit 6	R/W	HCSPASS	0
Bit 5	R/W	IDLEPASS	0
Bit 4	R/W	IN52	0
Bit 3	R/W	ALIGN[1]	0
Bit 2	R/W	ALIGN[0]	0
Bit 1	R/W	HCSFTR[1]	0
Bit 0	R/W	HCSFTR[0]	0

HCSFTR[1:0]:

The HCS filter bits, HCSFTR[1:0] indicate the number of consecutive error-free cells required, while in detection mode, before reverting back to correction mode.

Table 16 - RXCP-50 HCS Filtering Configurations

HCSFTR[1:0]	Cell Acceptance Threshold
00	One ATM cell with correct HCS before resumption of cell acceptance. This cell is accepted.
01	Two ATM cells with correct HCS before resumption of cell acceptance. The last cell is accepted.
10	Four ATM cells with correct HCS before resumption of cell acceptance. The last cell is accepted.
11	Eight ATM cells with correct HCS before resumption of cell acceptance. The last cell is accepted.

ALIGN[1:0]:

ALIGN[1:0] configures the RXCP-50 to perform cell delineation based on byte, nibble, or bit wide search algorithms when ATM Direct Mapping is used. Cell alignment is relative to overhead bits in the serial input data stream. The ALIGN[1:0] bits are valid only if ATM direct mapping is used - PLCP framing must be disabled. Recommended settings for DS3, E3, and J2 are shown.

Table 17 - RXCP-50 Cell Delination Algorithm Base

ALIGN[1:0]	Cell Delineation Algorithm base
00	Bit
01	Nibble (DS3)
10	Byte (E3,J2, E1, T1)
11	Unused

IN52:

The IN52 bit defines the number of bytes contained in incoming cells. When IN52 is a logic '0', incoming cells are 53 bytes in length. When IN52 is a logic '1', incoming cells are 52 bytes in length. In order for ATM cell delineation to function properly, incoming cells must be 53 bytes in length including a valid HCS byte. The HCS byte can be stripped off on the Utopia side using the DS27_53 register bit. If the S/UNI QJET is operating in PPP mode, incoming "cells" may be composed of 52 or 53 bytes without an HCS byte. In this case, the CCDIS register bit should be set to disable cell delineation, and the DS27_53 register bit should be set so that it is consistent with IN52.

IDLEPASS:

The IDLEPASS bit controls the function of the Idle Cell filter. When IDLEPASS is written with a logic 0, all cells that match the Idle Cell Header Pattern and Idle Cell Header Mask are filtered out. When IDLEPASS is a logic 1, the Idle Cell Header Pattern and Mask registers are ignored. The default state of this bit and the bits in the Idle Cell Header Mask and Idle Cell Header Pattern Registers enable the dropping of idle cells.

HCSPASS:

The HCSPASS bit controls the dropping of cells based on the detection of an uncorrectable HCS error. When HCSPASS is a logic 0, cells containing an uncorrectable HCS error are dropped. When HCSPASS is a logic 1, cells are passed to the receive FIFO regardless of errors detected in the HCS. Additionally, the HCS verification finite state machine never exits the correction mode.

Regardless of the programming of this bit, cells are always dropped while the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states unless the CCDIS bit in this register is set to logic 1.

CCDIS:

The CCDIS bit can be used to disable all cell filtering and cell delineation. All payload data read by the RXCP-50 is passed into its FIFO without the requirement of having to find cell delineation first. If PLCP framing is disabled, then alignment of the data read out of the ATM interface with respect to the line overhead is set by the ALIGN[1:0] bits of this register.

Register 062H, 162H, 262H, 362H: RXCP-50 FIFO/UTOPIA Control & Config

Bit	Type	Function	Default
Bit 7	R/W	RXPTYP	0
Bit 6		Unused	X
Bit 5	R/W	RCAINV	0
Bit 4	R/W	RCALEVEL0	1
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	FIFORST	0

FIFORST:

The FIFORST bit is used to reset the four-cell receive FIFO. When FIFORST is set to logic 0, the FIFO operates normally. When FIFORST is set to logic 1, the FIFO is immediately emptied and further writes into the FIFO are ignored (no incoming ATM cells will be stored in the FIFO). The FIFO remains empty and continues to ignore writes until a logic 0 is written to FIFORST.

See section 12.8 on resetting the receive and transmit FIFOs.

RCALEVEL0:

The RCALEVEL0 register bit selects the behavior of RCA and DRCA[x] when they de-assert (transition to logic 0 if RCAINV is logic 0, or transition to logic 1 if RCAINV is logic 1) as the receive FIFO empties.

When RCALEVEL0 is set to logic 1, DRCA[x] and RCA indicates that the receive FIFO is empty. RCA (and DRCA[x]), if polled, will de-assert on the rising RFCLK edge after Payload byte 48 (ATM8=1) or Payload byte 24 (ATM8=0) is output.

When RCALEVEL0 is set to logic 0, DRCA[x] and RCA, if polled, indicates that the receive FIFO is near empty. DRCA[x] and RCA, if polled, will de-assert on the rising RFCLK edge after Payload byte 43 (ATM8=1) or Payload byte 19 (ATM8=0) is output.

RCAINV:

The RCAINV bit inverts the polarity of the DRCA[x] and RCA output signal. When RCAINV is a logic 1, the polarity of DRCA[x] and RCA is inverted (DRCA[x] and RCA at logic 0 means there is a receive cell available to be read). When RCAINV is a logic 0, the polarity of RCA and DRCA[x] is not inverted.

RXPTYP:

The RXPTYP bit selects even or odd parity for output RXPRTY. When set to logic 1, output RXPRTY is the even parity bit for outputs RDAT[15:0]. When RXPTYP is set to logic 0, RXPRTY is the odd parity bit for outputs RDAT[15:0].

Register 063H, 163H, 263H, 363H: RXCP-50 Interrupt Enables and Counter Status

Bit	Type	Function	Default
Bit 7	R	XFERI	X
Bit 6	R	OVR	X
Bit 5		Unused	X
Bit 4	R/W	XFERE	0
Bit 3	R/W	OOCDE	0
Bit 2	R/W	HCSE	0
Bit 1	R/W	FOVRE	0
Bit 0	R/W	LCDE	0

LCDE:

The LCDE bit enables the generation of an interrupt due to a change in the LCD state. When LCDE is set to logic 1, the interrupt is enabled.

FOVRE:

The FOVRE bit enables the generation of an interrupt due to a FIFO overrun error condition. When FOVRE is set to logic 1, the interrupt is enabled.

HCSE:

The HCSE bit enables the generation of an interrupt due to the detection of a corrected or an uncorrected HCS error. When HCSE is set to logic 1, the interrupt is enabled.

OOCDE:

The OOCDE bit enables the generation of an interrupt due to a change in cell delineation state. When OOCDE is set to logic 1, the interrupt is enabled.

XFERE:

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the RXCP-50 Count registers. When XFERE is set to logic 1, the interrupt is enabled.

OVR:

The OVR bit is the overrun status of the RXCP-50 Performance Monitoring Count registers. A logic 1 in this bit position indicates that a previous transfer (indicated by XFERI being logic 1) has not been acknowledged before the next accumulation interval has occurred and that the contents of the RXCP-50 Count registers have been overwritten. OVR is set to logic 0 when this register is read.

XFERI:

The XFERI bit indicates that a transfer of RXCP-50 Performance Monitoring Count data has occurred. A logic 1 in this bit position indicates that the RXCP-50 Count registers have been updated. This update is initiated by writing to one of the RXCP-50 Count register locations or to the S/UNI-QJET Identification, Master Reset, and Global Monitor Update register. XFERI is set to logic 0 when this register is read.

Register 064H, 164H, 264H, 364H: RXCP-50 Status/Interrupt Status

Bit	Type	Function	Default
Bit 7	R	OOCDV	X
Bit 6	R	LCDV	X
Bit 5		Unused	X
Bit 4	R	OOCDI	X
Bit 3	R	CHCSI	X
Bit 2	R	UHCSI	X
Bit 1	R	FOVRI	X
Bit 0	R	LCDI	X

LCDI:

The LCDI bit is set high when there is a change in the loss of cell delineation (LCD) state. This bit is reset immediately after a read to this register.

FOVRI:

The FOVRI bit is set to logic 1 when a FIFO overrun occurs. This bit is reset immediately after a read to this register. No further FIFO overrun indications will occur until the condition which caused the original overrun has cleared. In the case where continuous FIFO overruns are occurring, only a single overrun indication (FOVRI -> '1') will be recorded until the overruns cease.

UHCSI:

The UHCSI bit is set high when an uncorrected HCS error is detected. This bit is reset immediately after a read to this register.

CHCSI:

The CHCSI bit is set high when a corrected HCS error is detected. This bit is reset immediately after a read to this register.

OOCDI:

The OOCDI bit is set high when the RXCP-50 enters or exits the SYNC state. The OOCDV bit indicates whether the RXCP-50 is in the SYNC state or not. The OOCDI bit is reset immediately after a read to this register.

LCDV:

The LCDV bit gives the Loss of Cell Delineation state. When LCD is logic 1, an out of cell delineation (OCD) defect has persisted for the number of cells specified in the LCD Count Threshold register. When LCD is logic 0, no OCD has persisted for the number of cells specified in the LCD Count Threshold register. The cell time period can be varied by using the LCDC[7:0] register bits in the RXCP-50 LCD Count Threshold register.

OOCDV:

The OOCDV bit indicates the cell delineation state. When OOCDV is high, the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states and is hunting for the cell boundaries. When OOCDV is low, the cell delineation state machine is in the 'SYNC' state and cells are passed through the receive FIFO.

Register 065H, 165H, 265H, 365H: RXCP-50 LCD Count Threshold (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	LCDC[10]	0
Bit 1	R/W	LCDC[9]	0
Bit 0	R/W	LCDC[8]	1

Register 066H, 166H, 266H, 366H: RXCP-50 LCD Count Threshold (LSB)

Bit	Type	Function	Default
Bit 7	R/W	LCDC[7]	0
Bit 6	R/W	LCDC[6]	1
Bit 5	R/W	LCDC[5]	1
Bit 4	R/W	LCDC[4]	0
Bit 3	R/W	LCDC[3]	1
Bit 2	R/W	LCDC[2]	0
Bit 1	R/W	LCDC[1]	0
Bit 0	R/W	LCDC[0]	0

LCDC[10:0]:

The LCDC[10:0] bits represent the number of consecutive cell periods the receive cell processor must be out of cell delineation before loss of cell delineation (LCD) is declared. Likewise, LCD is not de-asserted until receive cell processor is in cell delineation for the number of cell periods specified by LCDC[10:0].

The default value of LCD[10:0] is 360, which translates to the following integration periods:

Table 18 - RXCP-50 LCD Integration Periods

Format	Average cell period	Default LCD integration period
DS3 Direct Mapping	9.59 µs	3.45 ms
DS3 PLCP	10.42 µs	3.75 ms
E3 G.751 Direct Mapping	12.46 µs	4.49 ms
E3 G.751 PLCP	13.89 µs	5.00 ms
E3 G.832	12.50 µs	4.50 ms
J2 Direct Mapping	69.01 µs	24.84 ms
DS1 Direct Mapping	276.00 µs	99.40 ms
DS1 PLCP	300.00 us	108.00 ms
E1 Direct Mapping	220.83 µs	79.50 ms
E1 PLCP	237.50 µs	85.50 ms

Register 067H, 167H, 267H, 367H: RXCP-50 Idle Cell Header Pattern

Bit	Type	Function	Default
Bit 7	R/W	GFC[3]	0
Bit 6	R/W	GFC[2]	0
Bit 5	R/W	GFC[1]	0
Bit 4	R/W	GFC[0]	0
Bit 3	R/W	PTI[3]	0
Bit 2	R/W	PTI[2]	0
Bit 1	R/W	PTI[1]	0
Bit 0	R/W	CLP	1

GFC[3:0]:

The GFC[3:0] bits contain the pattern to match in the first, second, third, and fourth bits of the first octet of the 53-octet cell, in conjunction with the Idle Cell Header Mask Register. The IDLEPASS bit in the Configuration 2 Register must be set to logic zero to enable dropping of cells matching this pattern. Note that an all-zeros pattern must be present in the VPI and VCI fields of the idle or unassigned cell.

PTI[2:0]:

The PTI[2:0] bits contain the pattern to match in the fifth, sixth, and seventh bits of the fourth octet of the 53-octet cell, in conjunction with the Idle Cell Header Mask Register. The IDLEPASS bit in the Configuration 2 Register must be set to logic zero to enable dropping of cells matching this pattern.

CLP:

The CLP bit contains the pattern to match in the eighth bit of the fourth octet of the 53-octet cell, in conjunction with the Match Header Mask Register. The IDLEPASS bit in the Configuration 2 Register must be set to logic zero to enable dropping of cells matching this pattern.

Register 068H, 168H, 268H, 368H: RXCP-50 Idle Cell Header Mask

Bit	Type	Function	Default
Bit 7	R/W	MGFC[3]	1
Bit 6	R/W	MGFC[2]	1
Bit 5	R/W	MGFC[1]	1
Bit 4	R/W	MGFC[0]	1
Bit 3	R/W	MPTI[2]	1
Bit 2	R/W	MPTI[1]	1
Bit 1	R/W	MPTI[0]	1
Bit 0	R/W	MCLP	1

MGFC[3:0]:

The MGFC[3:0] bits contain the mask pattern for the first, second, third, and fourth bits of the first octet of the 53-octet cell. This mask is applied to the Idle Cell Header Pattern Register to select the bits included in the cell filter. A logic one in any bit position enables the corresponding bit in the pattern register to be compared. A logic zero causes the masking of the corresponding bit.

MPTI[3:0]:

The MPTI[3:0] bits contain the mask pattern for the fifth, sixth, and seventh bits of the fourth octet of the 53-octet cell. This mask is applied to the Idle Cell Header Pattern Register to select the bits included in the cell filter. A logic one in any bit position enables the corresponding bit in the pattern register to be compared. A logic zero causes the masking of the corresponding bit.

MCLP:

The CLP bit contains the mask pattern for the eighth bit of the fourth octet of the 53-octet cell. This mask is applied to the Idle Cell Header Pattern Register to select the bits included in the cell filter. A logic one in this bit position enables the MCLP bit in the pattern register to be compared. A logic zero causes the masking of the MCLP bit.

Register 069H, 169H, 269H, 369H: RXCP-50 Corrected HCS Error Count

Bit	Type	Function	Default
Bit 7	R	CHCS[7]	X
Bit 6	R	CHCS[6]	X
Bit 5	R	CHCS[5]	X
Bit 4	R	CHCS[4]	X
Bit 3	R	CHCS[3]	X
Bit 2	R	CHCS[2]	X
Bit 1	R	CHCS[1]	X
Bit 0	R	CHCS[0]	X

CHCS[7:0]:

The CHCS[7:0] bits indicate the number of corrected HCS error events that occurred during the last accumulation interval. The contents of these registers are valid after 24 RCLK periods containing cell header or payload data (line or PLCP overhead periods do not count) after a transfer is triggered by a write to one of RXCP-50's performance monitor counters (registers x69H - x71H) or to the S/UNI-QJET Identification, Master Reset, and Global Monitor Update register (006H).

Register 06AH, 16AH, 26AH, 36AH: RXCP-50 Uncorrected HCS Error Count

Bit	Type	Function	Default
Bit 7	R	UHCS[7]	X
Bit 6	R	UHCS[6]	X
Bit 5	R	UHCS[5]	X
Bit 4	R	UHCS[4]	X
Bit 3	R	UHCS[3]	X
Bit 2	R	UHCS[2]	X
Bit 1	R	UHCS[1]	X
Bit 0	R	UHCS[0]	X

UHCS[7:0]:

The UHCS[7:0] bits indicate the number of uncorrectable HCS error events that occurred during the last accumulation interval. The contents of these registers are valid after 24 RCLK periods containing cell header or payload data (line or PLCP overhead periods do not count) after a transfer is triggered by a write to one of RXCP-50's performance monitor counters (registers x69H - x71H) or to the S/UNI-QJET Identification, Master Reset, and Global Monitor Update register (006H).

Register 06BH, 16BH, 26BH, 36BH: RXCP-50 Receive Cell Counter (LSB)

Bit	Type	Function	Default
Bit 7	R	RCELL[7]	X
Bit 6	R	RCELL[6]	X
Bit 5	R	RCELL[5]	X
Bit 4	R	RCELL[4]	X
Bit 3	R	RCELL[3]	X
Bit 2	R	RCELL[2]	X
Bit 1	R	RCELL[1]	X
Bit 0	R	RCELL[0]	X

Register 06CH, 16CH, 26CH, 36CH: RXCP-50 Receive Cell Counter

Bit	Type	Function	Default
Bit 7	R	RCELL[15]	X
Bit 6	R	RCELL[14]	X
Bit 5	R	RCELL[13]	X
Bit 4	R	RCELL[12]	X
Bit 3	R	RCELL[11]	X
Bit 2	R	RCELL[10]	X
Bit 1	R	RCELL[9]	X
Bit 0	R	RCELL[8]	X

Register 06DH, 16DH, 26DH, 36DH: RXCP-50 Receive Cell Counter (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	RCELL[18]	X
Bit 1	R	RCELL[17]	X
Bit 0	R	RCELL[16]	X

RCELL[18:0]:

The RCELL[18:0] bits indicate the number of cells received and written into the receive FIFO during the last accumulation interval. Cells received and filtered due to HCS errors or Idle cell matches are not counted. The counter should be polled every second to avoid saturation. The contents of these registers are valid after 24 RCLK periods containing cell header or payload data (line or PLCP overhead periods do not count) after a transfer is triggered by a write to one of RXCP-50's performance monitor counters (registers x69H - x71H) or to the S/UNI-QJET Identification, Master Reset, and Global Monitor Update register (006H).

Register 06EH, 16EH, 26EH, 36EH: RXCP-50 Idle Cell Counter (LSB)

Bit	Type	Function	Default
Bit 7	R	ICELL[7]	X
Bit 6	R	ICELL[6]	X
Bit 5	R	ICELL[5]	X
Bit 4	R	ICELL[4]	X
Bit 3	R	ICELL[3]	X
Bit 2	R	ICELL[2]	X
Bit 1	R	ICELL[1]	X
Bit 0	R	ICELL[0]	X

Register 06FH, 16FH, 26FH, 36FH: RXCP-50 Idle Cell Counter

Bit	Type	Function	Default
Bit 7	R	ICELL[15]	X
Bit 6	R	ICELL[14]	X
Bit 5	R	ICELL[13]	X
Bit 4	R	ICELL[12]	X
Bit 3	R	ICELL[11]	X
Bit 2	R	ICELL[10]	X
Bit 1	R	ICELL[9]	X
Bit 0	R	ICELL[8]	X

Register 070H, 170H, 270H, 370H: RXCP-50 Idle Cell Counter (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	ICELL[18]	X
Bit 1	R	ICELL[17]	X
Bit 0	R	ICELL[16]	X

ICELL[18:0]:

The ICELL[18:0] bits indicate the number of idle cells received during the last accumulation interval. The counter should be polled every second to avoid saturation. The contents of these registers are valid after 24 RCLK periods containing cell header or payload data (line or PLCP overhead periods do not count) after a transfer is triggered by a write to one of RXCP-50's performance monitor counters (registers x69H - x71H) or to the S/UNI-QJET Identification, Master Reset, and Global Monitor Update register (006H).

Register 080H, 180H, 280H, 380H: TXCP-50 Configuration 1

Bit	Type	Function	Default
Bit 7	R/W	TPTYP	0
Bit 6	R/W	TCALEVEL0	0
Bit 5	R/W	HSCR	0
Bit 4	R/W	HCSDQDB	0
Bit 3	R/W	HCSB	0
Bit 2	R/W	HCSADD	1
Bit 1	R/W	DSCR	0
Bit 0	R/W	FIFORST	0

FIFORST:

The FIFORST bit is used to reset the four cell transmit FIFO. When FIFORST is set to logic zero, the FIFO operates normally. When FIFORST is set to logic one, the FIFO is immediately emptied and ignores writes. The FIFO remains empty and continues to ignore writes until a logic zero is written to FIFORST. Null/unassigned cells are transmitted until a subsequent cell is written to the FIFO.

See section 12.8 on resetting the receive and transmit FIFOs.

DSCR:

The DSCR bit controls the scrambling of the cell payload. When DSCR is a logic one, cell payload scrambling is disabled. When DSCR is a logic zero, payload scrambling is enabled. In the case where HSCR is logic one, the payload will be scrambled (along with the header) regardless of the setting of the DSCR bit.

HCSADD:

The HCSADD bit controls the addition of the coset polynomial, $x^6+x^4+x^2+1$, to the HCS octet prior to insertion in the synchronous payload envelope. When HCSADD is a logic one, the polynomial is added, and the resulting HCS is inserted. When HCSADD is a logic zero, the polynomial is not added, and the unmodified HCS is inserted. HCSADD takes effect unconditionally regardless of whether a null/unassigned cell is being transmitted or whether the HCS octet has been read from the FIFO.

HCSB:

The active low HCSB bit enables the internal generation and insertion of the HCS octet into the transmit cell stream. When HCSB is logic zero, the HCS is generated and inserted internally. When the HCSB and DS27_53 register bits are logic one, the HCS octet read from the transmit FIFO is inserted transparently into the transmit cell stream, but the TXCP-50 will still generate and insert the HCS octet for idle cells. If HCSB is logic one and the 26 word data structure is selected (DS27_53 is logic 0), then no HCS octet is inserted in the transmit data stream.

HCSDQDB:

The HCSDQDB bit controls the cell header octets included in the HCS calculation. When a logic 1 is written to HCSDQDB, header octets, 2, 3, and 4 are included in the HCS calculation as required by IEEE-802.6 DQDB specification. When a logic 0 is written to HCSDQDB, all four header octets are included in the HCS calculation as required by the ATM Forum UNI specification and ITU-T Recommendation I.432.

HSCR:

The Header Scramble enable bit, HSCR, enables scrambling of the ATM five octet header along with the payload. When set to logic one, the ATM header and payload are both scrambled. When set to logic zero, the header is left unscrambled and payload scrambling is determined by the DSCR bit.

TCALEVEL0:

The active high TCA (and DTCA[x]) level 0 bit, TCALEVEL0 determines what output TCA (and DTCA[x]) indicates when it de-asserts (transitions to logic 0 if TCAINV is logic 0, or transitions to logic 1 if TCAINV is logic 1).

When TCALEVEL0 is set to logic 1, TCA (and DTCA[x]) indicates that the transmit FIFO is full and can accept no more writes. DTCA[x] and TCA, if polled, will de-assert on the rising TFCLK edge when Payload byte 47 (ATM8=1) or Payload word 23 (ATM8=0) is sampled.

When TCALEVEL0 is set to logic zero, TCA (and DTCA[x]) indicates that the transmit FIFO is near full. DTCA[x] and TCA, if polled, will de-assert on the rising TFCLK edge when Payload byte 43 (ATM8=1) or Payload word 19 (ATM8=0) is sampled.

TPTYP:

The TPTYP bit selects even or odd parity for input TPRTY. When set to logic one, input TPRTY is the even parity bit for the TDAT input bus. When set to

logic zero, input TPRTY is the odd parity bit for the TDAT input bus. When ATM8 is set to logic one, the input bus consists of TDAT[7:0]. When ATM8 is logic zero, the input bus consists of TDAT[15:0].

Register 081H, 181H, 281H, 381H: TXCP-50 Configuration 2

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	TCAINV	0
Bit 3	R/W	FIFODP[1]	0
Bit 2	R/W	FIFODP[0]	0
Bit 1	R/W	DHCS	0
Bit 0	R/W	HCSCTLEB	0

HCSCTLEB:

The active low HCS control enable, HCSCTLEB bit enables the XORing of the HCS Control byte with the generated HCS. When set to logic zero, the HCS Control byte provided in the third word of the 27 word data structure is XORed with the generated HCS. When set to logic one, XORing is disabled and the HCS Control byte is ignored.

DHCS:

The DHCS bit controls the insertion of HCS errors for diagnostic purposes. When DHCS is set to logic one, the HCS octet is inverted prior to insertion in the synchronous payload envelope. DHCS takes effect unconditionally regardless of whether a null/unassigned cell is being transmitted or whether the HCS octet has been read from the FIFO. DHCS occurs after any error insertion caused by the Control Byte in the 27-word data structure.

FIFODP[1:0]:

The FIFODP[1:0] bits determine the transmit FIFO cell depth at which TCA and DTCA[x] de-assert. FIFO depth control may be important in systems where the cell latency through the TXCP-50 must be minimized. When the FIFO is filled to the specified depth, the transmit cell available signal, TCA (and DTCA[x]) is deasserted. Note that regardless of what fill level FIFODP[1:0] is set to, the transmit cell processor can store 4 complete cells. The selectable FIFO cell depths are shown below:

Table 19 - TXCP-50 FIFO Depth Configurations

FIFODP[1]	FIFODP[0]	FIFO DEPTH
0	0	4 cells
0	1	3 cells
1	0	2 cells
1	1	1 cell

TCAINV:

The TCAINV bit inverts the polarity of the TCA (and DTCA[x]) output signal. When TCAINV is a logic 1, the polarity of TCA (and DTCA[x]) is inverted (TCA (and DTCA[x]) at logic 0 means there is transmit cell space available to be written to). When TCAINV is a logic 0, the polarity of TCA (and DTCA[x]) is not inverted.

Register 082H, 182H, 282H, 382H: TXCP-50 Cell Count Status

Bit	Type	Function	Default
Bit 7	R/W	XFERE	0
Bit 6	R	XFERI	X
Bit 5	R	OVR	X
Bit 4		Unused	X
Bit 3	R/W	Reserved	1
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Reserved:

These bits should be set to their default values for proper operation

XFERI:

The XFERI bit indicates that a transfer of Transmit Cell Count data has occurred. A logic 1 in this bit position indicates that the Transmit Cell Count registers have been updated. This update is initiated by writing to one of the Transmit Cell Count register locations or to the S/UNI-QJET Identification, Master Reset, and Global Monitor Update register. XFERI is set to logic 0 when this register is read.

OVR:

The OVR bit is the overrun status of the Transmit Cell Count registers. A logic 1 in this bit position indicates that a previous transfer (indicated by XFERI being logic 1) has not been acknowledged before the next accumulation interval has occurred and that the contents of the Transmit Cell Count registers have been overwritten. OVR is set to logic 0 when this register is read.

XFERE:

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the Transmit Cell Count registers. When XFERE is set to logic 1, the interrupt is enabled.

Register 083H, 183H, 283H, 383H: TXCP-50 Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7	R/W	TPRTYE	0
Bit 6	R/W	FOVRE	0
Bit 5	R/W	TSOCE	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	TPRTYI	X
Bit 1	R	FOVRI	X
Bit 0	R	TSOCI	X

TSOCI:

The TSOCI bit is set high when the TSOC input is sampled high during any position other than the first word of the selected data structure. The write address counter is reset to the first word of the data structure when TSOC is sampled high. This bit is reset immediately after a read to this register.

FOVRI:

The FOVRI bit is set high when an attempt is made to write into the FIFO when it is already full. This bit is reset immediately after a read to this register

TPRTYI:

The TPRTYI bit indicates if a parity error was detected on the TDAT input bus. When logic one, the TPRTYI bit indicates a parity error over the active TDAT bus. The active TDAT bus is TDAT[15:0] when ATM8 is tied low and is TDAT[7:0] when ATM8 is tied high. This bit is cleared when this register is read. Odd or even parity is selected using the TPTYPE bit.

TSOCE:

The TSOCE bit enables the generation of an interrupt when the TSOC input is sampled high during any position other than the first word of the selected data structure. When TSOCE is set to logic one, the interrupt is enabled.

FOVRE:

The FOVRE bit enables the generation of an interrupt due to an attempt to write the FIFO when it is already full. When FOVRE is set to logic one, the interrupt is enabled.

TPRTYE:

The TPRTYE bit enables transmit parity interrupts. When set to logic one, parity errors are indicated on INT and TPRTYI. When set to logic zero, parity errors are indicated using bit TPRTYI but are not indicated on output INT.

Register 084H, 184H, 284H, 384H: TXCP-50 Idle Cell Header Control

Bit	Type	Function	Default
Bit 7	R/W	GFC[3]	0
Bit 6	R/W	GFC[2]	0
Bit 5	R/W	GFC[1]	0
Bit 4	R/W	GFC[0]	0
Bit 3	R/W	PTI[2]	0
Bit 2	R/W	PTI[1]	0
Bit 1	R/W	PTI[0]	0
Bit 0	R/W	CLP	1

CLP:

The CLP bit contains the eighth bit position of the fourth octet of the idle/unassigned cell pattern. Cell rate decoupling is accomplished by transmitting idle cells when the TXCP-50 detects that no outstanding cells exist in the transmit FIFO.

PTI[3:0]:

The PTI[3:0] bits contains the fifth, sixth, and seventh bit positions of the fourth octet of the idle/unassigned cell pattern. Idle cells are transmitted when the TXCP-50 detects that no outstanding cells exist in the transmit FIFO.

GFC[3:0]:

The GFC[3:0] bits contain the first, second, third, and fourth bit positions of the first octet of the idle/unassigned cell pattern. Idle/unassigned cells are transmitted when the TXCP-50 detects that no outstanding cells exist in the transmit FIFO. The all zeros pattern is transmitted in the VCI and VPI fields of the idle cell.

Register 085H, 185H, 285H, 385H: TXCP-50 Idle Cell Payload Control

Bit	Type	Function	Default
Bit 7	R/W	PAYLD[7]	0
Bit 6	R/W	PAYLD[6]	1
Bit 5	R/W	PAYLD[5]	1
Bit 4	R/W	PAYLD[4]	0
Bit 3	R/W	PAYLD[3]	1
Bit 2	R/W	PAYLD[2]	0
Bit 1	R/W	PAYLD[1]	1
Bit 0	R/W	PAYLD[0]	0

PAYLD[7:0]:

The PAYLD[7:0] bits contain the pattern inserted in the idle cell payload. Idle cells are inserted when the TXCP-50 detects that the transmit FIFO contains no outstanding cells. PAYLD[7] is the most significant bit and is the first bit transmitted. PAYLD[0] is the least significant bit.

Register 086H, 186H, 286H, 386H: TXCP-50 Transmit Cell Count (LSB)

Bit	Type	Function	Default
Bit 7	R	TCELL[7]	X
Bit 6	R	TCELL[6]	X
Bit 5	R	TCELL[5]	X
Bit 4	R	TCELL[4]	X
Bit 3	R	TCELL[3]	X
Bit 2	R	TCELL[2]	X
Bit 1	R	TCELL[1]	X
Bit 0	R	TCELL[0]	X

Register 087H, 187H, 287H, 387H: TXCP-50 Transmit Cell Count

Bit	Type	Function	Default
Bit 7	R	TCELL[15]	X
Bit 6	R	TCELL[14]	X
Bit 5	R	TCELL[13]	X
Bit 4	R	TCELL[12]	X
Bit 3	R	TCELL[11]	X
Bit 2	R	TCELL[10]	X
Bit 1	R	TCELL[9]	X
Bit 0	R	TCELL[8]	X

Register 088H, 188H, 288H, 388H: TXCP-50 Transmit Cell Count (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	TCELL[18]	X
Bit 1	R	TCELL[17]	X
Bit 0	R	TCELL[16]	X

TCELL[18:0]:

The TCELL[18:0] bits indicate the number of cells read from the transmit FIFO and inserted into the transmission stream during the last accumulation interval. Idle cells inserted into the transmission stream are not counted.

A write to any one of the TXCP-50 Transmit Cell Counter registers or to the S/UNI-QJET Identification, Master Reset, and Global Monitor Update register (006H) loads the registers with the current counter value and resets the internal 19 bit counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to the Transmit Cell Counter registers. The counter should be polled every second to avoid saturating. The contents of these registers are valid after 24 TICLK periods containing cell header or payload data (line or PLCP overhead periods do not count) after a transfer is triggered by a write to a TXCP-50 Transmit Cell count Register or the S/UNI-QJET Identification, Master Reset, and Global Monitor Update register (006H).

Register 090H, 190H, 290H, 390H: TTB Control

Bit	Type	Function	Default
Bit 7	R/W	ZEROEN	0
Bit 6	R/W	RRAMACC	0
Bit 5	R/W	RTIUIE	0
Bit 4	R/W	RTIMIE	0
Bit 3	R/W	PER5	0
Bit 2	R/W	TNULL	1
Bit 1	R/W	NOSYNC	0
Bit 0	R/W	Reserved	0

Reserved:

The reserved bit should be set to logic 0 for proper operation.

NOSYNC:

The NOSYNC bit disables synchronization to the Trail Trace message. When NOSYNC is set high, synchronization is disabled and the bytes of the Trail Trace message are captured by the TTB in a circular buffer. When NOSYNC is set low, the TTB synchronizes to the byte with the most significant bit set high and places that byte in the first location in the capture buffer page.

TNULL:

The transmit null (TNULL) bit controls the insertion of all-zeros into the outgoing Trail Trace message. The null insertion should be used when microprocessor accesses that change the outgoing trail trace message are being performed. When TNULL is set high, an all-zeros byte is inserted to the transmit stream. When this bit is set low, the contents of the transmit trace buffer are sent.

PER5:

The receive trace identifier persistency bit (PER5) controls the number of times that persistency check is made in order to accept the received message. When this bit is set high, five identical message required in order to accept the message. When this bit set low, three unchanged consecutive messages are required.

RTIMIE:

The receive trace identifier mismatch interrupt enable (RTIMIE) controls the activation of the interrupt output when comparison between the accepted trace identifier message and the expected trace identifier message changes state from match to mismatch and vice versa. When RTIMIE is set high, changes in match state will activate the interrupt output. When RTIMIE set low, trail trace message match state changes will not affect INTB.

RTIUIE:

The receive trace identifier unstable interrupt enable (RTIUIE) control the activation of the interrupt output when the receive trace identifier message changes state from stable to unstable and vice versa. When RTIUIE is set high, changes in the state of the trail trace message unstable indication will activate the interrupt output. When RTIUIE set low, trail trace unstable state changes will not effect INTB.

RRAMACC**:**

The receive RAM access (RRAMACC) control bit is used by the microprocessor to identify that the access from the microprocessor is to the receive trace buffers (addresses 0 - 127) or to the transmit trace buffer (addresses 128 - 191). When RRAMACC is set high, subsequent microprocessor read and write accesses are directed to the receive side trace buffers. When RRAMACC is set low, microprocessor accesses are directed to the transmit side trace buffer.

ZEROEN**:**

The zero enable bit (ZEROEN) enables TIM assertion and removal based on an all ZEROs path trace message string. When ZEROEN is set high, all ZEROs path trace message strings are considered when entering and exiting TIM states. When ZEROEN is set low, all ZEROs path trace message strings are ignored.

Register 091H, 191H, 291H, 391H: TTB Trail Trace Identifier Status

Bit	Type	Function	Default
Bit 7	R	BUSY	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	RTIUI	X
Bit 2	R	RTIUV	X
Bit 1	R	RTIMI	X
Bit 0	R	RTIMV	X

RTIMV:

The receive trace identifier mismatch value status bit (RTIMV) is set high when the accepted message differs from the expected message. RTIMV is set low when the accepted message is equal to the expected message. A mismatch is not declared if the accepted trail trace message string is all-zeros.

RTIMI:

The receive trace identifier mismatch indication status bit (RTIMI) is set high when match/mismatch status of the trace identifier framer changes state. This bit (and the interrupt) is cleared when this register is read.

RTIUV:

The receive trace identifier unstable value status bit (RTIUV) is set high when 8 messages that differ from its immediate predecessor are received. RTIUV is set low and the unstable message count is reset when 3 or 5 (depending on PER5 control bit) consecutive identical messages are received.

RTIUI:

The receive trace identifier unstable indication status bit (RTIUV) is set high when the stable/unstable status of the trace identifier framer changes state. This bit (and the interrupt) is cleared when this register is read.

BUSY:

The BUSY bit reports whether a previously initiated indirect read or write to the trail trace RAM has been completed. BUSY is set high upon writing to the TTB Indirect Address register, and stays high until the access has completed. At this point, BUSY is set low. This register should be polled to determine when either new data is available in the TTB Indirect Data register after an indirect read, or when the TTB is ready to accept another write access.

Register 092H, 192H, 292H, 392H: TTB Indirect Address

Bit	Type	Function	Default
Bit 7	R/W	RWB	0
Bit 6	R/W	A[6]	0
Bit 5	R/W	A[5]	0
Bit 4	R/W	A[4]	0
Bit 3	R/W	A[3]	0
Bit 2	R/W	A[2]	0
Bit 1	R/W	A[1]	0
Bit 0	R/W	A[0]	0

A[6:0]:

The indirect read address bits (A[6:0]) indexes into the trail trace identifier buffers. When RRAMACC is set high, decimal addresses 0 to 63 reference the receive capture page while addresses 64 to 127 reference the receive expected page. The receive capture page contains the identifier bytes extracted from the receive G.832 E3 stream. The receive expected page contains the expected trace identifier message down-loaded from the microprocessor. When RRAMACC is set low, decimal addresses 0 to 63 reference the transmit message buffer which contains the identifier message to be inserted in the TR bytes of the G.832 E3 transmit stream. In this case A[6] is a don't care (I.e., address 0 and address 64 are indexes to the same location in the buffer). Note that only the first 16 addresses need to be written with the trail trace message to be transmitted.

RWB:

The access control bit (RWB) selects between an indirect read or write access to the static page of the trail trace message buffer. Writing to this indirect address register initiates an external microprocessor access to the static page of the trail trace message buffer. When RWB is set high, a read access is initiated. The data read is available upon completion of the access in the TTB Indirect Data register. When RWB is set low, a write access is initiated. The data in the TTB Indirect Data register will be written to the addressed location in the static page.

Register 093H, 193H, 293H, 393H: TTB Indirect Data

Bit	Type	Function	Default
Bit 7	R/W	D[7]	X
Bit 6	R/W	D[6]	X
Bit 5	R/W	D[5]	X
Bit 4	R/W	D[4]	X
Bit 3	R/W	D[3]	X
Bit 2	R/W	D[2]	X
Bit 1	R/W	D[1]	X
Bit 0	R/W	D[0]	X

D[7:0]:

The indirect data bits (D[7:0]) contain either the data read from a message buffer after an indirect read operation has completed, or the data to be written to the RAM for an indirect write operation. Note that the write data must be set up in this register before an indirect write is initiated. Data read from this register reflects the value written until the completion of a subsequent indirect read operation.

Register 094H, 194H, 294H, 394H: TTB Expected Payload Type Label

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	EXPLD[2]	0
Bit 1	R/W	EXPLD[1]	0
Bit 0	R/W	EXPLD[0]	0

EXPLD[2:0]:

The EXPLD[2:0] bits contain the expected payload type label bits of the G.832 E3 Maintenance and Adaptation (MA) byte. The EXPLD[2:0] bits are compared with the received payload type label extracted from the receive stream. A payload type label mismatch (PLDM) is declared if the received payload type bits differs from the expected payload type. If enabled, an interrupt is asserted upon declaration and removal of PLDM.

For compatibility with old equipment that inserts 000B for unequipped or 001B for equipped, regardless of the payload type, the receive payload type label mismatch mechanism is based on the following table:

Table 20 - TTB Payload Type Match Configurations

Expected	Received	Action
000	000	Match
000	001	Mismatch
000	XXX	Mismatch
001	000	Mismatch
001	001	Match
001	XXX	Match
XXX	000	Mismatch

Expected	Received	Action
XXX	001	Match
XXX	XXX	Match
XXX	YYY	Mismatch

Note:

XXX, YYY = anything except 000B or 001B, and XXX is not equal to YYY.

Reserved:

The reserved bits must be written to logic 0 for proper operation.

Register 095H, 195H, 295H, 395H: TTB Payload Type Label Control/Status

Bit	Type	Function	Default
Bit 7	R/W	RPLDUIE	0
Bit 6	R/W	RPLDMIE	0
Bit 5	R	Unused	X
Bit 4	R	Unused	X
Bit 3	R	RPLDUI	X
Bit 2	R	RPLDUV	X
Bit 1	R	RPLDMI	X
Bit 0	R	RPLDMV	X

RPLDMV:

The receive payload type label mismatch status bit (RPLDMV) reports the match/mismatch status between the expected and the received payload type label. RPLDMV is set high when the received payload type bits differ from the expected payload type written to the TTB Expected Payload Type Label Register. The PLDMV bit is set low when the received payload type matches the expected payload type.

RPLDMI:

The receive payload type label mismatch interrupt status bit (RPLDMI) is set high when the match/mismatch status between the received and the expected payload type label changes state. This bit (and the interrupt) is cleared when this register is read.

RPLDUV:

The receive payload type label unstable status bit (RPLDUV) reports the stable/unstable status of the payload type label bits in the receive stream. RPLDUV is set high when 5 labels that differ from its immediate predecessor are received. RPLDUV is set low and the unstable label count is reset when 5 consecutive identical labels are received.

RPLDUI:

The receive payload type label unstable interrupt status bit (RPLDUI) is set high when the stable/unstable status of the path signal label changes state. This bit (and the interrupt) is cleared when this register is read.

RPLDMIE:

The receive payload type label mismatch interrupt enable bit (RPLDMIE) controls the activation of the interrupt output when the comparison between received and the expected payload type label changes state from match to mismatch and vice versa. When RPLDMIE is set high, changes in match state activates the interrupt output. When RPLDMIE is set low, changes from match to mismatch or mismatch to match will not generate an interrupt.

RPLDUIE:

The receive payload type label unstable interrupt enable bit (RPLDUIE) controls the activation of the interrupt output when the received payload type label changes state from stable to unstable and vice versa. When RPLDUIE is set high, changes in stable state activates the interrupt output. When RPLDUIE is set low, changes in the stable state will not generate and interrupt.

Register 098H, 198H, 298H, 398H: RBOC Configuration/Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	IDLE	0
Bit 1	R/W	AVC	0
Bit 0	R/W	FEACE	0

FEACE:

The FEACE bit enables the generation of an interrupt when a valid far end alarm and control (FEAC) code is detected. When a logic 1 is written to FEACE, the interrupt generation is enabled.

AVC:

The AVC bit position selects the validation criterion used in determining a valid FEAC code. When a logic 0 is written to AVC, a FEAC code is validated when 8 out of the last 10 received codes are identical. The FEAC code is removed when 2 out of the last 10 received code do not match the validated code.

When a logic 1 is written to AVC, a FEAC code is validated when 4 out of the last 5 received codes are identical. The FEAC code is removed when a single received FEACs does not match the validated code.

IDLE:

The IDLE bit enables the generation of an interrupt when a validated FEAC is removed. When a logic 1 is written to IDLE, the interrupt generation is enabled.

Register 099H, 199H, 299H, 399H: RBOC Interrupt Status

Bit	Type	Function	Default
Bit 7	R	IDLI	X
Bit 6	R	FEACI	X
Bit 5	R	FEAC[5]	X
Bit 4	R	FEAC[4]	X
Bit 3	R	FEAC[3]	X
Bit 2	R	FEAC[2]	X
Bit 1	R	FEAC[1]	X
Bit 0	R	FEAC[0]	X

FEAC[5:0]:

The FEAC[5:0] bits contain the received far end alarm and control channel codes. The FEAC[5:0] bits are set to all ones ("111111") when no code has been validated.

FEACI:

The FEACI bit is set to logic 1 when a new FEAC code is validated. The FEAC code value is contained in the FEAC[5:0] bits. The FEACI bit position is set to logic 0 when this register is read.

IDLI:

The IDLI bit is set to logic 1 when a validated FEAC code is removed. The FEAC[5:0] bits are set to all ones when the code is removed. The IDLI bit position is set to logic 0 when this register is read.

Register 09AH, 19AH, 29AH, 39AH: XBOC Code

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	FEAC[5]	1
Bit 4	R/W	FEAC[4]	1
Bit 3	R/W	FEAC[3]	1
Bit 2	R/W	FEAC[2]	1
Bit 1	R/W	FEAC[1]	1
Bit 0	R/W	FEAC[0]	1

FEAC[5:0]:

FEAC[5:0] contain the six bit code that is transmitted on the far end alarm and control channel (FEAC). The transmitted code consists of a sixteen bit sequence that is repeated continuously. The sequence consists of 8 ones followed by a zero, followed by the six bit code sequence transmitted in order FEAC0, FEAC1, ..., FEAC5, followed by a zero. The all ones sequence is inserted in the FEAC channel when FEAC[5:0] is written with all ones.

Note: If configured for J2 transmission format (TFRM[1:0] is 10 binary) and any of LCDEN, AISEN, OOFEN, LOSEN are set to logic 1 in the S/UNI-QJET Data Link and FERF/RAI Control, FEAC[5:0] in this register must all be set to logic 1 for proper RAI transmission upon detection of LCD, PHYAIS, LOF, or LOS by the J2 FRMR. Otherwise, the BOC code configured by the FEAC[5:0] bits of this register will be transmitted instead of the RAI.

Register 09BH, 19BH, 29BH, 39BH: S/UNI-QJET Misc.

Bit	Type	Function	Default
Bit 7	R/W	AISOOF	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	TPRBS	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	TCELL	0
Bit 2	R/W	LOC_RESET	0
Bit 1	R/W	FORCELOS	0
Bit 0	R/W	LINESYSCLK	0

LINESYSCLK:

LINESYSCLK is used to select the high-speed system clock which the TDPR and RDLC transmit and receive HDLC controllers use as a reference. If LINESYSCLK is set to logic 1, then the RDLC uses the receive line clock (RCLK[x]) and the TDPR uses the transmit line clock (TICLK[x]) as its high-speed system reference clock respectively. If LINESYSCLK is set to logic 0, the RDLC uses the receive ATM Utopia interface clock (RFCLK) and the TDPR uses the transmit ATM Utopia interface clock (TFCLK) as its high-speed system reference clock respectively.

The read/write access rate to the RDLC and TDPR are limited by their high-speed reference clock frequency. Data and Configuration settings can be written into the TDPR at a maximum rate equal to 1/8 of its high-speed reference clock frequency. Data and status indications can be read from the TDPR at a maximum rate equal to 1/8 of its high-speed reference clock frequency. Data and status indications can be read from the RDLC at a maximum rate equal to 1/10 of its high-speed reference clock frequency.

Instantaneous variations in the high-speed reference clock frequencies (e.g. jitter in the receive line clock) must be considered when determining the procedure used to read and write the TDPR and RDLC registers.

FORCELOS:

FORCELOS is used to force a Loss of Signal (LOS) condition on the transmit unipolar or bipolar data outputs TPOS/TDATO[x] and TNEG[x]. When FORCELOS is logic 1, the TPOS/TDATO[x] and TNEG[x] outputs will be

forced to logic 0. When FORCELOS is logic 0, the TPOS/TDATO[x] and TNEG[x] outputs will operate normally.

LOC_RESET:

LOC_RESET performs a software local reset of the corresponding quadrant of the S/UNI-QJET. When LOC_RESET is logic 1, the corresponding quadrant of the S/UNI-QJET is held in a reset state. When LOC_RESET is logic 0, the quadrant is in normal operational mode.

The LOC_RESET bit for quadrant 1 (reg 09BH) also resets the chip level Utopia bus. While the LOC_RESET for quadrant 1 is set to logic 1, the QJETs Utopia bus will be held in a reset state, and will not function. In applications where the Utopia bus is required, the LOC_RESET for quadrant 1 should not be permanently set to logic 1.

TCELL:

When the TCELL bit is a logic 1, the TPOHFP/TFPO/TMFPO/TGAPCLK/TCELL[4:1] pin takes on the TCELL function, and pulses once for every transmitted cell (idle or unassigned).

Reserved:

The reserved bit should be set to logic 0 for proper operation.

TPRBS:

Register bit TPRBS is used to insert a pseudo-random binary sequence into the transmit stream in place of other payload data. The exact nature of the PRBS is configurable through the PRGD registers (xA0H to xAFH).

Reserved:

The reserved bit should be set to logic 0 for proper operation.

AISOOF:

The AISOOF bit allows the receive data output stream on RDATO[x] to be forced to all 1's when the DS3, E3, or J2 FRMR loses frame. When AISOOF is set to logic 1, RDATO[x] will be forced to all 1's when frame alignment is lost. When AISOOF is set to logic 0, RDATO[x] will continue to output raw data even when frame alignment is lost.

Note that AISOOF is only valid in framer-only mode (FRMRONLY=1, S/UNI-QJET Configuration 1 register).

Register 09CH, 19CH, 29CH, 39CH: S/UNI-QJET FRMR LOF Status.

Bit	Type	Function	Default
Bit 7	R	FRMLOF	X
Bit 6	R/W	FRMLOFE	0
Bit 5	R	FRMLOFI	X
Bit 4	R/W	J2SIGTHRU	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

FRMLOFI:

The FRMLOFI bit shows that a transition has occurred on the FRMLOF state. When FRMLOFI is logic 1, the FRMLOF state has changed since the last read of this register. The FRMLOFI bit is cleared whenever this register is read.

FRMLOFE:

The FRMLOFE bit enables the generation of an interrupt due to a change in the FRMLOF state. When FRMLOFE is a logic 1, the interrupt is enabled.

FRMLOF:

The FRMLOF bit shows the current state of the E3/T3 LOF or the J2 Extended LOF indication (depending on which mode is enabled). When FRMLOF is logic 1, the framer has lost frame synchronization for greater than 1ms, 2ms, or 3ms depending on the setting of the LOFINT[1:0] bits in the S/UNI-QJET Receive Configuration register.

J2SIGTHRU:

The J2SIGTHRU bit allows the signaling bits in timeslot 97 and 98 on the TDATI[x] stream to pass transparently through the J2 TRAN. When J2SIGTHRU is logic 1, timeslots 97 and 98 are passed transparently through from TDATI[x]. When J2SIGTHRU is logic 0, timeslots 97 and 98 are sourced from the J2 TRAN TS97 Signaling and J2 TRAN TS98 Signaling registers.

If J2SIGTHRU is set to logic 1 and TPRBS (S/UNI-QJET Misc. register) is also set to logic 1, the transmitted PRBS will continue through timeslots 97 and 98.

J2SIGTHRU is only valid in framer-only mode (FRMRONLY=1, S/UNI-QJET Configuration 1 register).

Reserved:

The reserved bits should be set to logic 0 for proper operation.

Register 0A0H, 1A0H, 2A0H, 3A0H: PRGD Control

Bit	Type	Function	Default
Bit 7	R/W	PDR[1]	0
Bit 6	R/W	PDR[0]	0
Bit 5	R/W	QRSS	0
Bit 4	R/W	PS	0
Bit 3	R/W	TINV	0
Bit 2	R/W	RINV	0
Bit 1	R/W	AUTOSYNC	1
Bit 0	R/W	MANSYNC	0

PDR[1:0]:

The PDR[1:0] bits select the content of the four pattern detector registers (at addresses xACH to xAFH) to be any one of the pattern receive registers, the error count holding registers, or the bit count holding registers. The selection is shown in the following table:

Table 21 - PRGD Pattern Detector Register Configuration

PDR[1:0]	PDR#1	PDR#2	PDR#3	PDR#4
00, 01	Pattern Receive (LSB)	Pattern Receive	Pattern Receive	Pattern Receive (MSB)
10	Error Count (LSB)	Error Count	Error Count	Error Count (MSB)
11	Bit Count (LSB)	Bit Count	Bit Count	Bit Count (MSB)

QRSS:

The QRSS bit enables the zero suppression feature required when generating the QRSS sequence. When QRSS is a logic 1, a one is forced in the TDATO stream when the following 14 bit positions are all zeros. When QRSS is a logic 0, the zero suppression feature is disabled.

PS:

The PS bit selects the generated pattern. When PS is a logic 1, a repetitive pattern is generated. When PS is a logic 0, a pseudo-random pattern is generated.

The PS bit must be programmed to the desired setting before programming any other PRGD registers, or the transmitted pattern may be corrupted. Any time the setting of the PS bit is changed, the rest of the PRGD registers should be reprogrammed.

TINV:

The TINV bit controls the logical inversion of the generated data stream. When TINV is a logic 1, the data is inverted. When TINV is a logic 0, the data is not inverted

RINV:

The RINV bit controls the logical inversion of the receive data stream before processing. When RINV is a logic 1, the received data is inverted before being processed by the pattern detector. When RINV is a logic 0, the received data is not inverted

AUTOSYNC:

The AUTOSYNC bit enables the automatic resynchronization of the pattern detector. The automatic resynchronization is activated when 6 or more bit errors are detected in the last 64 bit periods. When AUTOSYNC is a logic 1, the auto resync feature is enabled. When AUTO SYNC is a logic 0, the auto sync feature is disabled, and pattern resynchronization is accomplished using the MANSYNC bit.

MANSYNC:

The MANSYNC bit is used to initiate a manual resynchronization of the pattern detector. A low to high transition on MANSYNC initiates the resynchronization.

Register 0A1H, 1A1H, 2A1H, 3A1H: PRGD Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7	R/W	SYNCE	0
Bit 6	R/W	BEE	0
Bit 5	R/W	XFERE	0
Bit 4	R	SYNCV	X
Bit 3	R	SYNCI	X
Bit 2	R	BEI	X
Bit 1	R	XFERI	X
Bit 0	R	OVR	X

SYNCE:

The SYNCE bit enables the generation of an interrupt when the pattern detector changes synchronization state. When SYNCE is set to logic 1, the interrupt is enabled.

BEE:

The BEE bit enables the generation of an interrupt when a bit error is detected in the receive data. When BEE is set to logic 1, the interrupt is enabled.

XFERE:

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the receive pattern registers, the bit counter holding registers, and the error counter holding registers. When XFERE is set to logic 1, the interrupt is enabled.

SYNCV:

The SYNCV bit indicates the synchronization state of the pattern detector. When SYNCV is a logic 1 the pattern detector is synchronized (the pattern detector has observed at least 32 consecutive error free bit periods). When SYNCV is a logic 0, the pattern detector is out of sync (the pattern detector has detected 6 or more bit errors in a 64 bit period window).

SYNCI:

The SYNCI bit indicates that the detector has changed synchronization state since the last time this register was read. If SYNCI is logic 1, then the pattern detector has gained or lost synchronization at least once. SYNCI is set to logic 0 when this register is read.

BEI:

The BEI bit indicates that one or more bit errors have been detected since the last time this register was read. When BEI is set to logic 1, at least one bit error has been detected. BEI is set to logic 0 when this register is read.

XFERI:

The XFERI bit indicates that a transfer of pattern detector data has occurred. A logic 1 in this bit position indicates that the pattern receive registers, the bit counter holding registers and the error counter holding registers have been updated. This update is initiated by writing to one of the pattern detector register locations, or by writing to the S/UNI-QJET Identification, Master Reset, and Global Monitor Update register (006H). XFERI is set to logic 0 when this register is read.

OVR:

The OVR bit is the overrun status of the pattern detector registers. A logic 1 in this bit position indicates that a previous transfer (indicated by XFERI being logic 1) has not been acknowledged before the next accumulation interval has occurred and that the contents of the pattern receive registers, the bit counter holding registers and the error counter holding registers have been overwritten. OVR is set to logic 0 when this register is read.

Register 0A2H, 1A2H, 2A2H, 3A2H: PRGD Length

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	PL[4]	0
Bit 3	R/W	PL[3]	0
Bit 2	R/W	PL[2]	0
Bit 1	R/W	PL[1]	0
Bit 0	R/W	PL[0]	0

PL[4:0]:

PL[4:0] determine the length of the generated pseudo random or repetitive pattern. The pattern length is equal to the value of PL[4:0] + 1.

Register 0A3H, 1A3H, 2A3H, 3A3H: PRGD Tap

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	PT[4]	0
Bit 3	R/W	PT[3]	0
Bit 2	R/W	PT[2]	0
Bit 1	R/W	PT[1]	0
Bit 0	R/W	PT[0]	0

PT[4:0]:

PT[4:0] determine the feedback tap position of the generated pseudo random pattern. The feedback tap position is equal to the value of PT[4:0] + 1.

Register 0A4H, 1A4H, 2A4H, 3A4H: PRGD Error Insertion Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	EVENT	0
Bit 2	R/W	EIR[2]	0
Bit 1	R/W	EIR[1]	0
Bit 0	R/W	EIR[0]	0

EVENT:

A low to high transition on the EVENT bit causes a single bit error to be inserted in the generated pattern. This bit must be cleared and set again for a subsequent error to be inserted.

EIR[2:0]:

The EIR[2:0] bits control the insertion of a programmable bit error rate as indicated in the following table:

Table 22 - PRGD Generated Bit Error Rate Configurations

EIR[2:0]	Generated Bit Error Rate
000	No errors inserted
001	10^{-1}
010	10^{-2}
011	10^{-3}
100	10^{-4}
101	10^{-5}
110	10^{-6}
111	10^{-7}

Register 0A8H, 1A8H, 2A8H, 3A8H: Pattern Insertion #1

Bit	Type	Function	Default
Bit 7	R/W	PI[7]	0
Bit 6	R/W	PI[6]	0
Bit 5	R/W	PI[5]	0
Bit 4	R/W	PI[4]	0
Bit 3	R/W	PI[3]	0
Bit 2	R/W	PI[2]	0
Bit 1	R/W	PI[1]	0
Bit 0	R/W	PI[0]	0

Register 0A9H, 1A9H, 2A9H, 3A9H: Pattern Insertion #2

Bit	Type	Function	Default
Bit 7	R/W	PI[15]	0
Bit 6	R/W	PI[14]	0
Bit 5	R/W	PI[13]	0
Bit 4	R/W	PI[12]	0
Bit 3	R/W	PI[11]	0
Bit 2	R/W	PI[10]	0
Bit 1	R/W	PI[9]	0
Bit 0	R/W	PI[8]	0

Register 0AAH, 1AAH, 2AAH, 3AAH: Pattern Insertion #3

Bit	Type	Function	Default
Bit 7	R/W	PI[23]	0
Bit 6	R/W	PI[22]	0
Bit 5	R/W	PI[21]	0
Bit 4	R/W	PI[20]	0
Bit 3	R/W	PI[19]	0
Bit 2	R/W	PI[18]	0
Bit 1	R/W	PI[17]	0
Bit 0	R/W	PI[16]	0

Register 0ABH, 1ABH, 2ABH, 3ABH: Pattern Insertion #4

Bit	Type	Function	Default
Bit 7	R/W	PI[31]	0
Bit 6	R/W	PI[30]	0
Bit 5	R/W	PI[29]	0
Bit 4	R/W	PI[28]	0
Bit 3	R/W	PI[27]	0
Bit 2	R/W	PI[26]	0
Bit 1	R/W	PI[25]	0
Bit 0	R/W	PI[24]	0

PI[31:0]:

PI[31:0] contain the data that is loaded in the pattern generator each time a new pattern (pseudo random or repetitive) is to be generated. When a pseudo random pattern is to be generated, PI[31:0] should be set to 0xFFFFFFFF. The data is loaded each time pattern insertion register #4 is written. Pattern insertion registers #1 - #3 should be loaded with the desired data before pattern register #4 is written.

Register 0ACH, 1ACH, 2ACH, 3ACH: PRGD Pattern Detector #1

Bit	Type	Function	Default
Bit 7	R	PD[7]	0
Bit 6	R	PD[6]	0
Bit 5	R	PD[5]	0
Bit 4	R	PD[4]	0
Bit 3	R	PD[3]	0
Bit 2	R	PD[2]	0
Bit 1	R	PD[1]	0
Bit 0	R	PD[0]	0

Register 0ADH, 1ADH, 2ADH, 3ADH: PRGD Pattern Detector #2

Bit	Type	Function	Default
Bit 7	R	PD[15]	0
Bit 6	R	PD[14]	0
Bit 5	R	PD[13]	0
Bit 4	R	PD[12]	0
Bit 3	R	PD[11]	0
Bit 2	R	PD[10]	0
Bit 1	R	PD[9]	0
Bit 0	R	PD[8]	0

Register 0AEH, 1AEH, 2AEH, 3AEH: PRGD Pattern Detector #3

Bit	Type	Function	Default
Bit 7	R	PD[23]	0
Bit 6	R	PD[22]	0
Bit 5	R	PD[21]	0
Bit 4	R	PD[20]	0
Bit 3	R	PD[19]	0
Bit 2	R	PD[18]	0
Bit 1	R	PD[17]	0
Bit 0	R	PD[16]	0

Register 0AFH, 1AFH, 2AFH, 3AFH: PRGD Pattern Detector #4

Bit	Type	Function	Default
Bit 7	R	PD[31]	0
Bit 6	R	PD[30]	0
Bit 5	R	PD[29]	0
Bit 4	R	PD[28]	0
Bit 3	R	PD[27]	0
Bit 2	R	PD[26]	0
Bit 1	R	PD[25]	0
Bit 0	R	PD[24]	0

PD[31:0]:

PD[31:0] contain the pattern detector data. The values contained in these registers are determined by the PDR[1:0] bits in the control register.

When PDR[1:0] is set to 00 or 01, PD[31:0] contain the pattern receive register. The 32 bits received immediately before the last accumulation interval are present on PD[31:0}. PD[31] contains the first of the 32 received bits, PD[0] contains the last of the 32 received bits.

When PDR[1:0] is set to 10, PD[31:0] contain the error counter holding register. The value in this register represents the number of bit errors that have been accumulated since the last accumulation interval. Note that bit errors are not accumulated while the pattern detector is out of sync.

When PDR[1:0] is set to 11, PD[31:0] contain the bit counter holding register. The value in this register represents the total number of bits that have been received since the last accumulation interval.

The values of PD[31:0] are updated whenever one of the four PRGD Pattern Detector registers is written or when register 006H, the S/UNI-QJET Identification, Master Reset, and Global Monitor Update register is written.

11 TEST FEATURES DESCRIPTION

Simultaneously asserting (low) the CSB, RDB and WRB inputs causes all digital output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the S/UNI-QJET. Test mode registers (as opposed to normal mode registers) are selected when A[10] is high.

Test mode registers may also be used for board testing. When all of the TSBs within the S/UNI-QJET are placed in test mode 0, device inputs may be read and device outputs may be forced via the microprocessor interface (refer to the section "Test Mode 0" for details).

In addition, the S/UNI-QJET also supports a standard IEEE 1149.1 five-signal JTAG boundary scan test port for use in board testing. All digital device inputs may be read and all digital device outputs may be forced via the JTAG test port.

Table 23 - Test Mode Register Memory Map

Address				Register
000H-3FFH				Normal Mode Registers
400H				Master Test Register
408H	508H	608H	708H	SPLR Test Register 0
409H	509H	609H	709H	SPLR Test Register 1
40AH	50AH	60AH	70AH	SPLR Test Register 2
40BH	50BH	60BH	70BH	Reserved
40CH	50CH	60CH	70CH	SPLT Test Register 0
40DH	50DH	60DH	70DH	SPLT Test Register 1
40EH	50EH	60EH	70EH	SPLT Test Register 2
40FH	50FH	60FH	70FH	SPLT Test Register 3
410H	510H	610H	710H	PMON Test Register 0
411H	511H	611H	711H	PMON Test Register 1
412H-41FH	512H-51FH	612H-61FH	712H-71FH	Reserved

Address				Register
420H	520H	620H	720H	CPPM Test Register 0
421H	521H	621H	721H	CPPM Test Register 1
422H	522H	622H	722H	CPPM Test Register 2
423H-42FH	523H-52FH	623H-62FH	723H-72FH	Reserved
430H	530H	630H	730H	DS3 FRMR Test Register 0
431H	531H	631H	731H	DS3 FRMR Test Register 1
432H	532H	632H	732H	DS3 FRMR Test Register 2
433H	533H	633H	733H	DS3 FRMR Test Register 3
434H	534H	634H	734H	DS3 TRAN Test Register 0
435H	535H	635H	735H	DS3 TRAN Test Register 1
436H	536H	636H	736H	DS3 TRAN Test Register 2
437H	537H	637H	737H	Reserved
438H	538H	638H	738H	E3 FRMR Test Register 0
439H	539H	639H	739H	E3 FRMR Test Register 1
43AH	53AH	63AH	73AH	E3 FRMR Test Register 2
43BH-43FH	53BH-53FH	63BH-63FH	73BH-73FH	Reserved
440H	540H	640H	740H	E3 TRAN Test Register 0
441H	541H	641H	741H	E3 TRAN Test Register 1
442H	542H	642H	742H	E3 TRAN Test Register 2
443H	543H	643H	743H	Reserved
444H	544H	644H	744H	J2 FRMR Test Register 0
445H	545H	645H	745H	J2 FRMR Test Register 1
446H	546H	646H	746H	J2 FRMR Test Register 2
447H	547H	647H	747H	J2 FRMR Test Register 3
448H-44BH	548H-54BH	648H-64BH	748H-74BH	Reserved
44CH	54CH	64CH	74CH	J2 TRAN Test Register 0

Address				Register
44DH	54DH	64DH	74DH	J2 TRAN Test Register 1
44EH	54EH	64EH	74EH	J2 TRAN Test Register 2
44FH	54FH	64FH	74FH	J2 TRAN Test Register 3
450H	550H	650H	750H	RDLC Test Register 0
451H	551H	651H	751H	RDLC Test Register 1
452H	552H	652H	752H	RDLC Test Register 2
453H	553H	653H	753H	RDLC Test Register 3
454H	554H	654H	754H	RDLC Test Register 4
455H-457H	555H-557H	655H-657H	755H-757H	Reserved
458H	558H	658H	758H	TDPR Test Register 0
459H	559H	659H	759H	TDPR Test Register 1
45AH	55AH	65AH	75AH	TDPR Test Register 2
45BH	55BH	65BH	75BH	TDPR Test Register 3
45CH-45FH	55CH-55FH	65CH-65FH	75CH-75FH	Reserved
460H	560H	660H	760H	RXCP-50 Test Register 0
461H	561H	661H	761H	RXCP-50 Test Register 1
462H	562H	662H	762H	RXCP-50 Test Register 2
463H	563H	663H	763H	RXCP-50 Test Register 3
464H	564H	664H	764H	RXCP-50 Test Register 4
465H	565H	665H	765H	RXCP-50 Test Register 5
466H-47FH	566H-57FH	666H-67FH	766H-77FH	Reserved
480H	580H	680H	780H	TXCP-50 Test Register 0
481H	581H	681H	781H	TXCP-50 Test Register 1
482H	582H	682H	782H	TXCP-50 Test Register 2
483H	583H	683H	783H	TXCP-50 Test Register 3
484H	584H	684H	784H	TXCP-50 Test Register 4

Address				Register
485H	585H	685H	785H	TXCP-50 Test Register 5
486H-48FH	586H-58FH	686H-68FH	786H-78FH	Reserved
490H	590H	690H	790H	TTB Test Register 0
491H	591H	691H	791H	TTB Test Register 1
492H	592H	692H	792H	TTB Test Register 2
493H-497H	593H-597H	693H-697H	793H-797H	Reserved
498H	598H	698H	798H	RBOC Test Register 0
499H	599H	699H	799H	RBOC Test Register 1
49AH	59AH	69AH	79AH	XBOC Test Register 1
49BH	59BH	69BH	79BH	XBOC Test Register 0
49CH-49FH	59CH-59FH	69CH-69FH	79CH-79FH	Reserved
4A0H	5A0H	6A0H	7A0H	PRGD Test Register 0
4A1H	5A1H	6A1H	7A1H	PRGD Test Register 1
4A2H	5A2H	6A2H	7A2H	PRGD Test Register 2
4A3H	5A3H	6A3H	7A3H	PRGD Test Register 3
4A4H-4FFH	5A4H-5FFH	6A4H-6FFH	7A4H-7FFH	Reserved

Notes on Test Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.

2. Writable test mode register bits are not initialized upon reset unless otherwise noted.

Register 400H: S/UNI-QJET Master Test

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	W	A_TM[9]	X
Bit 5	W	A_TM[8]	X
Bit 4	W	PMCTST	X
Bit 3	W	DBCTRL	0
Bit 2	R/W	IOTST	0
Bit 1	W	HIZDATA	0
Bit 0	R/W	HIZIO	0

This register is used to enable S/UNI-QJET test features. All bits, except PMCTST and A_TM[9:8], are reset to zero by a hardware reset of the S/UNI-QJET. The S/UNI-QJET Master Test register is not affected by a software reset (via the S/UNI-QJET Identification, Master Reset, and Global Monitor Update register (006H)).

HIZIO, HIZDATA:

The HIZIO and HIZDATA bits control the tri-state modes of the S/UNI-QJET . While the HIZIO bit is a logic one, all output pins of the S/UNI-QJET except the data bus and output TDO are held tri-state. The microprocessor interface is still active. While the HIZDATA bit is a logic one, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles. The HIZDATA bit is overridden by the DBCTRL bit.

IOTST:

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each TSB block in the S/UNI-QJET for board level testing. When IOTST is a logic one, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequentially the device outputs (refer to the "Test Mode 0 Details" in the "Test Features" section).

DBCTRL:

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic one and either IOTST or PMCTST

are logic one, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the S/UNI-QJET to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

PMCTST:

The PMCTST bit is used to configure the S/UNI-QJET for PMC's manufacturing tests. When PMCTST is set to logic one, the S/UNI-QJET microprocessor port becomes the test access port used to run the PMC manufacturing test vectors. The PMCTST bit is logically "ORed" with the IOTST bit, and can be cleared by setting CSB to logic one or by writing logic zero to the bit.

A_TM[9:8]:

The state of the A_TM[9:8] bits internally replace the input address lines A[9:8] respectively when PMCTST is set to logic 1. This allows for more efficient use of the PMC manufacturing test vectors.

11.1 Test Mode 0 Details

In test mode 0, the S/UNI-QJET allows the logic levels on the device inputs to be read through the microprocessor interface and allows the device outputs to be forced to either logic level through the microprocessor interface. The IOTST bit in the S/UNI-QJET Master Test register must be set to logic one to access the device I/O.

To enable test mode 0, the IOTST bit in the S/UNI-QJET Master Test register is set to logic one and the device should be left in its default state after reset unless otherwise noted. All Test Register 1 locations of all blocks must be written with the value 0 (see Table 23).

Reading the following address locations returns the values on the indicated inputs:

Table 24 - Test Mode 0 Input Read Address Locations

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
40CH		TIOHM[1]	TICLK[1]	TPOH[1]	TPOHINS[1]			
430H								RCLK[1]
436H							TOH[1]	TOHINS[1]
444H					RPOS[1]	RNEG[1]		

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
465H							RENB[3]	
466H	RADR[4][4]	RADR[3][4]	RADR[2][4]	RADR[1][4]	RADR[0][4]			RFCLK
480H				ATM8				
482H	PHY_ADR[2]	TADR[4][1]			TSOC	TENB[2]	TPRTY	TFCLK
483H	PHY_ADR[1]	PHY_ADR[0]			TADR[3][1]	TADR[2][1]	TADR[1][1]	TADR[0][1]
484H	TDAT[15]	TDAT[14]	TDAT[13]	TDAT[12]	TDAT[11]	TDAT[10]	TDAT[9]	TDAT[8]
485H	TDAT[7]	TDAT[6]	TDAT[5]	TDAT[4]	TDAT[3]	TDAT[2]	TDAT[1]	TDAT[0]
50CH		TIOHM[2]	TICLK[2]	TPOH[2]	TPOHINS[2]			
50FH								REF8KI
530H								RCLK[2]
536H							TOH[2]	TOHINS[2]
544H					RPOS[2]	RNEG[2]		
565H							RADR[1][4]	
60CH		TIOHM[3]	TICLK[3]	TPOH[3]	TPOHINS[3]			
630H								RCLK[3]
636H							TOH[3]	TOHINS[3]
644H					RPOS[3]	RNEG[3]		
665H							RADR[2][4]	
70CH		TIOHM[4]	TICLK[4]	TPOH[4]	TPOHINS[4]			
730H								RCLK[4]
736H							TOH[4]	TOHINS[4]
744H					RPOS[4]	RNEG[4]		
765H							RADR[3][4]	

1. Before reading these values, the input must be set to the test state, TENB must be set to logic 1, and TFCLK must transition from logic 0 to logic 1.

2. TENB must be set to its test state and TFCLK must transition from logic 0 to logic 1 before its value will be captured in the test register.

3. RENB must be set to its test state and RFCLK must transition from logic 0 to logic 1 before its value will be captured in the test register.

4. Before reading these values, the input must be set to the test state, RENB must be set to logic 1, and RFCLK must transition from logic 0 to logic 1.

Writing the following address locations forces the outputs to the value in the corresponding bit position (zeros should be written to all unused test register locations):

Table 25 - Test Mode 0 Output Write Address Locations

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
408H					RPOHCLK[1]	RPOH[1]	REF8KO[1]	
40AH	FRMSTAT[1]							INTB[1]
40CH						TPOHFP[1]	TPOHCLK[1]	
410H								INTB[1]
430H	INTB[1]							
434H								TCLK[1]
436H							TOHFP[1]	TOHCLK[1]
432H			ROH[1]					ROHCLK[1]
433H				ROHFP[1]				
44CH	TPOS[1]							
44EH								TNEG[1]
450H								INTB[1]
458H								INTB[1]
463H	RDAT[15][2]	RDAT[14][2]	RDAT[13][2]	RDAT[12][2]	RDAT[11][2]	RDAT[10][2]	RDAT[9][2]	RDAT[8][2]
464H	RDAT[7][2]	RDAT[6][2]	RDAT[5][2]	RDAT[4][2]	RDAT[3][2]	RDAT[2][2]	RDAT[1][2]	RDAT[0][2]
465H		LCD[1]	RSOC[2]	RPRTY[2]	RCA[3]	DRCA[1]	INTB[1]	
480H						TCA[4,5], DTCA[1][5]		INTB[1]
490H								INTB[1]
498H		INTB[1]						
4A2H							INTB[1]	
508H					RPOHCLK[2]	RPOH[2]	REF8KO[2]	
50AH	FRMSTAT[2]							INTB[1]
50CH						TPOHFP[2]	TPOHCLK[2]	
510H								INTB[1]
530H	INTB[1]							
534H								TCLK[2]
536H							TOHFP[2]	TOHCLK[2]

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
532H			ROH[2]					ROHCLK[2]
533H				ROHFP[2]				
54CH	TPOS[2]							
54EH								TNEG[2]
550H								INTB[1]
558H								INTB[1]
565H		LCD[2]	RSOC[2]	RPRTY[2]		DRCA[2]	INTB[1]	
580H						DTCA[2][5]		INTB[1]
590H								INTB[1]
598H		INTB[1]						
5A2H							INTB[1]	
608H					RPOHCLK[3]	RPOH[3]	REF8KO[3]	
60AH	FRMSTAT[3]							INTB[1]
60CH						TPOHFP[3]	TPOHCLK[3]	
610H								INTB[1]
630H	INTB[1]							
634H								TCLK[3]
636H							TOHFP[3]	TOHCLK[3]
632H			ROH[3]					ROHCLK[3]
633H				ROHFP[3]				
64CH	TPOS[3]							
64EH								TNEG[3]
650H								INTB[1]
658H								INTB[1]
665H		LCD[3]	RSOC[2]	RPRTY[2]		DRCA[3]	INTB[1]	
680H						DTCA[3][5]		INTB[1]
690H								INTB[1]
698H		INTB[1]						
6A2H							INTB[1]	
708H					RPOHCLK[4]	RPOH[4]	REF8KO[4]	
70AH	FRMSTAT[4]							INTB[1]
70CH						TPOHFP[4]	TPOHCLK[4]	

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
710H								INTB[1]
730H	INTB[1]							
734H								TCLK[4]
736H							TOHFP[4]	TOHCLK[4]
732H			ROH[4]					ROHCLK[4]
733H				ROHFP[4]				
74CH	TPOS[4]							
74EH								TNEG[4]
750H								INTB[1]
758H								INTB[1]
765H		LCD[4]	RSOC[2]	RPRTY[2]		DRCA[4]	INTB[1]	
780H						DTCA[4] [5]		INTB[1]
790H								INTB[1]
798H		INTB[1]						
7A2H							INTB[1]	

1. All these register bits must be set to logic 0 for the INTB output to be tri-stated. If any one of these register bits is a logic 1, then INTB will be driven to logic 0.

2. To enable these outputs, after setting the desired state, RADR[0] must be set to logic 0, RENB must be set to logic 1, bit 4 of register 09BH must be set to logic 1, and RFCLK must transition from logic 0 to logic 1.

3. To enable this output, after setting the desired state, RADR[4:2] must be set equal to PHY_ADR[2:0], RADR[1:0] must be set equal to binary 00, RFCLK must transition from logic 0 to logic 1.

4. To enable this output, after setting the desired state, TADR[4:2] must be set equal to PHY_ADR[2:0], TADR[1:0] must be set equal to binary 00, TFCLK must transition from logic 0 to logic 1.

5. Bit 1 of this register must be logic 0.

11.2 JTAG Test Port

The S/UNI-QJET JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

Table 26 - Instruction Register

Length - 3 bits

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Identification Register

Length - 32 bits

Version number - 2H

Part Number - 7346H

Manufacturer's identification code - 0CDH

Device identification - 273460CDH

Table 27 - Boundary Scan Register

Length - 198 bits

Pin/Enable	Register Bit	Cell Type	ID Bit	Pin/Enable	Register Bit	Cell Type	ID Bit
TDAT[15][1]	0	IN_CELL	0	RX_OEB[4]	66	OUT_CELL	(0)
TDAT[14]	1	IN_CELL	0	TICLK[4;1]	67:70	IN_CELL	(0)
TDAT[13]	2	IN_CELL	1	TIOHM[4:1]	71:74	IN_CELL	(0)
TDAT[12]	3	IN_CELL	0	TPOH[4:1]	75:78	IN_CELL	(0)
TDAT[11]	4	IN_CELL	0	TPOHINS[4:1]	79:82	IN_CELL	(0)
TDAT[10]	5	IN_CELL	1	TPOHCLK[4:1]	83:86	OUT_CELL	(0)
TDAT[9]	6	IN_CELL	1	TPOHFP[4:1]	87:90	OUT_CELL	(0)
TDAT[8]	7	IN_CELL	1	LCD[4:1]	91:94	OUT_CELL	(0)
TDAT[7]	8	IN_CELL	0	RPOH[4:1]	95:98	OUT_CELL	(0)
TDAT[6]	9	IN_CELL	0	RPOHCLK[4:1]	99:102	OUT_CELL	(0)
TDAT[5]	10	IN_CELL	1	REF8KO[4:1]	103:106	OUT_CELL	(0)
TDAT[4]	11	IN_CELL	1	FRMSTAT[4:1]	107:110	OUT_CELL	(0)
TDAT[3]	12	IN_CELL	0	REF8KI	111	IN_CELL	(0)
TDAT[2]	13	IN_CELL	1	ROHCLK[4:1]	112;115	OUT_CELL	(0)
TDAT[1]	14	IN_CELL	0	ROHFP[4:1]	116:119	OUT_CELL	(0)
TDAT[0]	15	IN_CELL	0	ROH[4:1]	120:123	OUT_CELL	(0)
TFCLK	16	IN_CELL	0	TOHFP[4:1]	124:127	OUT_CELL	(0)
TADR[4]	17	IN_CELL	1	TOHCLK[4:1]	128:131	OUT_CELL	(0)
TADR[3]	18	IN_CELL	1	TOHINS[4:1]	132:135	IN_CELL	(0)
TADR[2]	19	IN_CELL	0	TOH[4:1]	136:139	IN_CELL	(0)
TADR[1]	20	IN_CELL	0	RCLK[4:1]	140:143	IN_CELL	(0)
TADR[0]	21	IN_CELL	0	RNEG[4:1]	144;147	IN_CELL	(0)
TPRTY	22	IN_CELL	0	RPOS[4:1]	148:151	IN_CELL	(0)
TSOC	23	IN_CELL	0	TCLK[4:1]	152:155	OUT_CELL	(0)
TENB	24	IN_CELL	1	TNEG[4:1]	156:159	OUT_CELL	(0)
TCA	25	OUT_CELL	1	TPOS[4:1]	160:163	OUT_CELL	(0)
TCA_OEB[2]	26	OUT_CELL	0	INTB	164	OUT_CELL	(0)
DTCA[4]	27	OUT_CELL	0	RSTB	165	IN_CELL	(0)
DTCA[3]	28	OUT_CELL	1	WRB	166	IN_CELL	(0)
DTCA[2]	29	OUT_CELL	1	RDB	167	IN_CELL	(0)
DTCA[1]	30	OUT_CELL	0	ALE	168	IN_CELL	(0)
PHY_ADR[2]	31	IN_CELL	1	CSB	169	IN_CELL	(0)
PHY_ADR[1]	32	IN_CELL	(1)	A[10:0]	170:180	IN_CELL	(0)
PHY_ADR[0]	33	IN_CELL	(1)	D[7]	181	IO_CELL	(0)
ATM8	34	IN_CELL	(0)	DOENB [7][5]	182	OUT_CELL	(0)
DRCA[4]	35	OUT_CELL	(0)	D[6]	183	IO_CELL	(0)
DRCA[3]	36	OUT_CELL	(0)	DOENB[6][5]	184	OUT_CELL	(0)
DRCA[2]	37	OUT_CELL	(0)	D[5]	185	IO_CELL	(0)
DRCA[1]	38	OUT_CELL	(0)	DOENB [5][5]	186	OUT_CELL	(0)
RCA	39	OUT_CELL	(0)	D[4]	187	IO_CELL	(0)

RCA_OEB[3]	40	OUT_CELL	(0)	DOENB [4][5]	188	OUT_CELL	(0)
RSOC	41	OUT_CELL	(0)	D[3]	189	IO_CELL	(0)
RENB	42	IN_CELL	(0)	DOENB [3][5]	190	OUT_CELL	(0)
RFCLK	43	IN_CELL	(0)	D[2]	191	IO_CELL	(0)
RADR[4]	44	IN_CELL	(0)	DOENB [2][5]	192	OUT_CELL	(0)
RADR[3]	45	IN_CELL	(0)	D[1]	193	IO_CELL	(0)
RADR[2]	46	IN_CELL	(0)	DOENB [1][5]	194	OUT_CELL	(0)
RADR[1]	47	IN_CELL	(0)	D[0]	195	IO_CELL	(0)
RADR[0]	48	IN_CELL	(0)	DOENB [0][5]	196	OUT_CELL	(0)
RPRTY	49	OUT_CELL	(0)	HIZ[6]	197	OUT_CELL	(0)
RDAT[15:0]	50:65	OUT_CELL	(0)				

NOTES:

1. TDAT[15] is the first bit of the boundary scan chain.

2. TCA_OEB will set TCA to tri-state when set to logic 1. When set to logic 0, TCA will be driven.

3. RCA_OEB will set RCA to tri-state when set to logic 1. When set to logic 0, RCA will be driven.

4. RX_OEB will set RDAT[15:0], RPRTY, and RSOC to tri-state when set to logic 1. When set to logic 0, RDAT[15:0], RPRTY, and RSOC will be driven.

5. The DOENB signals will set the corresponding bidirectional signal (the one preceding the DOENB in the boundary scan chain — see note 1 also) to an output when set to logic 0. When set to logic 1, the bidirectional signal will be tri-stated.

6. HIZ will set all outputs not controlled by TCA_OEB, RCA_OEB, RX_OEB, and DOENB to tri-state when set to logic 1. When set to logic 0, those outputs will be driven.

12 OPERATION

12.1 Software Initialization Sequence

The S/UNI QJET can come out of reset in a mode that consumes excess power. The device functionality is not altered except for excessive power consumption resulting excess heat dissipation which could lead to long term reliability problems.

The software initialization sequence in this section will put the S/UNI QJET into a normal power consumption state should the device come out of reset in the excess power state. This reset sequence must be used to guarantee long term reliability of the device.

1. Reset the S/UNI QJET.

2. Set IOTST (bit 2) in the Master Test Register (datasheet pg. 291) to '1' (by writing 00000100 to register 400H).

3. Put the QJET Receive Cell Processor (RXCP) into test mode by writing:

    00000101 to test register 461H

    00000101 to test register 561H

    00000101 to test register 661H

    00000101 to test register 761H

4. Set QJET Receive Cell Processor block built in set test (BIST) controls signals by writing:

    01000000 to test register 462H

    01000000 to test register 562H

    01000000 to test register 662H

    01000000 to test register 762H

    10101010 to test register 463H

    10101010 to test register 563H

10101010 to test register 663H

10101010 to test register 763H

5. Put the QJET Transmit Cell Processor (TXCP) into test mode by writing:

00000011 to test register 481H

00000011 to test register 581H

00000011 to test register 681H

00000011 to test register 781H

6. Set QJET Transmit Cell Processor block built in set test (BIST) controls signals by writing:

10000000 to test register 480H

10000000 to test register 580H

10000000 to test register 680H

10000000 to test register 780H

10101010 to test register 482H

10101010 to test register 582H

10101010 to test register 682H

10101010 to test register 782H

7. Toggle REF8KI (pin T3, datasheet page 29) signal several times (this provides the clock to the RAM). REF8KI is the test clock used by the TXCP and RXCP blocks when in test mode.

8. Set IOTST (bit 2) in the Master Test register (datasheet pg. 291) to '0' (by writing 00000000 to register 400H).

9. Resume normal device programming.

12.2 Register Settings for Basic Configurations

Table 28 - Register Settings for Basic Configurations

Mode of Operation	S/UNI-QJET Registers (values in Hexadecimal)																	
	x00	x02	x03	x04	x08	x0C	x30	x34	x38	x39	x40	x41	x44	x4C	x60	x61	x80	x9B
T3 C-bit ADM	C0	00	00	F8	00	00	83	01	--	--	--	--	--	--	04	04	04	00
T3 M23 ADM	C0	00	00	F8	00	00	82	00	--	--	--	--	--	--	04	04	04	00
T3 C-bit PLCP	40	00	00	F8	04	04	83	01	--	--	--	--	--	--	04	00	04	00
T3 M23 PLCP	40	00	00	F8	04	04	82	00	--	--	--	--	--	--	04	00	04	00
T3 C-bit framer only[1]	50	00	00	78	00	00	83	01	--	--	--	--	--	--	--	--	--	01
T3 M23 framer only[1]	50	00	00	78	00	00	82	00	--	--	--	--	--	--	--	--	--	01
E3 G.832 ADM	C0	40	40	F8	00	00	--	--	04	00	01	01	--	--	04	08	04	00
E3 G.832 framer only[1]	50	40	40	78	00	00	--	--	04	00	01	01	--	--	--	--	--	01
E3 G.751 ADM	C0	40	40	F8	00	00	--	--	00	00	00	01	--	--	04	08	04	00
E3 G.751 PLCP	40	40	40	F8	44	44	--	--	00	04	00	41	--	--	04	00	04	00
E3 G.751 framer only[1]	50	40	40	78	00	00	--	--	00	00	00	01	--	--	--	--	--	01
J2 ADM	C0	80	80	F8	00	00	--	--	--	--	--	--	03	0E	04	08	04	00
J2 framer	50	80	80	78	00	00	--	--	--	--	--	--	03	0E	--	--	--	01

only[1]																		
E1 PLCP	40	C0	C0	--	C4	C4	--	--	--	--	--	--	--	--	04	00	04	00
E1 ADM	40	C0	C0	--	C0	C0	--	--	--	--	--	--	--	--	04	00	04	00
T1 PLCP	40	C0	C0	--	84	84	--	--	--	--	--	--	--	--	04	00	04	00
T1 ADM	40	C0	C0	--	80	80	--	--	--	--	--	--	--	--	04	00	04	00
External Framer ADM[2]	40	C0	C0	--	01	01	--	--	--	--	--	--	--	--	04	00[4]	04	00

1. In framer only modes, TGAPCLK[x] and RGAPCLK[x] are enabled by programming register x01H to 0CH.

2. Byte, nibble, or bit alignment of the ATM Cell bytes to the line overhead is configured using the TOCTA bit in register x00H, and the FORM[1:0] bits in register x0CH.

3. Unipolar mode is selected for DS3, E3, and J2 modes by setting the TUNI bit to logic 1 in register x02H and the UNI bit in x30H, x38H, and x44H respectively. When the DS3, E3, or J2 framers are bypassed, unipolar mode is selected by default.

4. Bit, Nibble, and Byte alignment of the ATM cell octets to the arbitrary external frame overhead is set using the ALIGN[1:0] bits of register x61H.

5. ATM cells are configured to have the Coset Polynomial added to the HCS byte and payload scrambling/descrambling is enabled.

6. ATM Idle cell header octets H1, H2, H3, and H4 are configured to be 00H 00H 00H 01H respectively.

12.3 PLCP Frame Formats

The S/UNI-QJET provides support for four different PLCP frame formats: the DS3 PLCP format, the DS1 frame format, the G.751 E3 frame format, and the E1 frame format. The structure of each of these formats is quite similar, and is illustrated in Figure 12 through Figure 15.

Figure 12 - DS3 PLCP Frame Format

A1	A2	P11	Z6	ATM Cell	
A1	A2	P10	Z5	ATM Cell	
A1	A2	P9	Z4	ATM Cell	
A1	A2	P8	Z3	ATM Cell	
A1	A2	P7	Z2	ATM Cell	
A1	A2	P6	Z1	ATM Cell	
A1	A2	P5	F1	ATM Cell	PLCP Frame Rate 125 µs
A1	A2	P4	B1	ATM Cell	
A1	A2	P3	G1	ATM Cell	
A1	A2	P2	M2	ATM Cell	
A1	A2	P1	M1	ATM Cell	
A1	A2	P0	C1	ATM Cell	Trailer
Framing (3 octets)			POH	53 octets	13 or 14 nibbles

The DS3 PLCP frame provides the transmission of 12 ATM cells every 125 µs. The PLCP frame is nibble aligned to the overhead bits in the DS3 frame; however, there is no relationship between the start of the PLCP frame and the start of the DS3 M-frame. A trailer is inserted at the end of each PLCP frame. The number of nibbles inserted (13 or 14) is varied continuously such that the resulting PLCP frame rate can be locked to an 8 kHz reference.

Figure 13 - DS1 PLCP Frame Format

A1	A2	P9	Z4	ATM Cell	PLCP Frame Rate 3 ms
A1	A2	P8	Z3	ATM Cell	
A1	A2	P7	Z2	ATM Cell	
A1	A2	P6	Z1	ATM Cell	
A1	A2	P5	F1	ATM Cell	
A1	A2	P4	B1	ATM Cell	
A1	A2	P3	G1	ATM Cell	
A1	A2	P2	M2	ATM Cell	
A1	A2	P1	M1	ATM Cell	
A1	A2	P0	C1	ATM Cell	Trailer
Framing (3 octets)			POH	53 octets	6 octets

The DS1 PLCP frame provides the transmission of 10 ATM cells every 3 ms. The PLCP frame is octet aligned to the framing bit in the DS1 frame; there is no relationship between the start of the PLCP frame, and the start of the DS1 frame. A trailer is inserted at the end of each PLCP frame. The number of octets inserted is always six, and cannot be varied.

Figure 14 - G.751 E3 PLCP Frame Format

A1	A2	P8	Z3	ATM Cell	PLCP Frame Rate 125 µs
A1	A2	P7	Z2	ATM Cell	
A1	A2	P6	Z1	ATM Cell	
A1	A2	P5	F1	ATM Cell	
A1	A2	P4	B1	ATM Cell	
A1	A2	P3	G1	ATM Cell	
A1	A2	P2	M2	ATM Cell	
A1	A2	P1	M1	ATM Cell	
A1	A2	P0	C1	ATM Cell	Trailer
Framing (3 octets)			POH	53 octets	17,18,19,20, or 21 octets

The G.751 E3 PLCP frame provides the transmission of 9 ATM cells every 125 µs. The PLCP frame is octet aligned to the 16 overhead bits in the ITU-T Recommendation G.751 E3 frame; there is no relationship between the start of the PLCP frame, and the start of the E3 frame. A trailer is inserted at the end of each PLCP frame. The number of octets inserted is nominally 18, 19, or 20, and is based on the number of E3 overhead octets (4, 5, or 6) that have been inserted during the PLCP frame period. The nominal octet stuffing can be varied by ±1 octet to allow the E3 PLCP frame to be locked to an external 8 kHz reference. Thus the trailer can be 17, 18, 19, 20, or 21 octets in length.

Figure 15 - E1 PLCP Frame Format

A1	A2	P9	Z4	ATM Cell	PLCP Frame Rate 2.375 ms
A1	A2	P8	Z3	ATM Cell	
A1	A2	P7	Z2	ATM Cell	
A1	A2	P6	Z1	ATM Cell	
A1	A2	P5	F1	ATM Cell	
A1	A2	P4	B1	ATM Cell	
A1	A2	P3	G1	ATM Cell	
A1	A2	P2	M2	ATM Cell	
A1	A2	P1	M1	ATM Cell	
A1	A2	P0	C1	ATM Cell	
Framing (3 octets)		POH		53 octets	

The E1 PLCP frame provides the transmission of 10 ATM cells every 2.375 ms. Thirty of the thirty-two available E1 channels are used for transporting the PLCP frame. The remaining two channels are reserved for E1 framing and signaling functions. The PLCP frame is octet aligned to the channel boundaries in the E1 frame. The PLCP frame is aligned to the 125 µs E1 frame (the A1 octet of the first row of the PLCP frame is inserted in timeslot 1 of the E1 frame).

12.3.1 PLCP Path Overhead Octet Processing

Table 29 - PLCP Overhead Processing

Overhead Field	Transmit Operation	Receive Operation
A1, A2: Frame	Inserts the PLCP frame alignment pattern (F628H)	Searches the receive stream for the PLCP frame alignment pattern.

Overhead Field	Transmit Operation	Receive Operation
Alignment Pattern		When the pattern has been detected for two consecutive rows, along with two valid, and sequential path overhead identifier octets, the S/UNI-QJET declares in-frame. Note that the ATM cell boundaries are implicitly known when the PLCP frame is located, thus cell delineation is accomplished by locating the PLCP frame. When errors are detected in both octets in a single row, or when errors are detected in two consecutive path overhead identifier octets, the S/UNI-QJET declares an out-of-frame defect. The loss-of-frame defect is an integrated version of the out-of-frame defect state.
P0-P11: Path Overhead Identifier	Inserts the path overhead identifier codes in accordance with the PLCP frame alignment. See Table 30.	Identifies the PLCP path overhead bytes by monitoring the sequence of the POI bytes.
Z1-Z6: Growth:	These octets are unused and are nominally programmed with all zeros. Access to these octets is provided by the PLCP transmit overhead access port.	These octets are ignored and are extracted on the RPOH pin.
F1: User Channel	This octet is unused and the value inserted in this octet is controlled by an internal register or by TPOH pin.	This octet is ignored and is extracted on the RPOH pin.
B1: Bit Interleaved Parity	This octet contains an 8-bit interleaved parity (BIP) calculated across the entire PLCP frame (excluding the A1, A, Pn octets and the trailer). The B1 value is calculated based on even parity and the value inserted in the current frame is the BIP	The bit interleaved parity is calculated for the current frame and stored. The B1 octet contained in the subsequent frame is extracted and compared against the calculated value. Differences between the two values provide an indication of the end-to-end bit error rate. These differences are

Overhead Field	Transmit Operation	Receive Operation
	result calculated for the previous frame.	accumulated in a counter in the CPPM block.
G1: Path Status	The first four bit positions provide a PLCP far end block error function and indicates the number of B1 errors detected at the near end. The FEBE field has nine legal values (0000b-1000b) indicating between zero and eight B1 errors. The fifth bit position is used to transmit PLCP yellow alarm. The last three bit positions provide the link status signal used in IEEE-802.6 DQDB implementations. Yellow alarm and link status signal insertion is controlled by the internal registers or by TPOH pin.	The G1 byte provides the PLCP FEBE function and is accumulated in an a counter in the CPPM block. PLCP yellow alarm is detected or removed when the yellow bit is set to logic one or zero for ten consecutive frames. The yellow alarm state and the link status signal state are contained in the SPLR Status register.
M1, M2: Control Information	These octets carry the DQDB layer management information. Internal register controls the nominal value inserted in these octets. These octets are unused in ATM Forum T3 UNI 3.0 specification.	These octets are ignored and are extracted on the RPOH pin.
C1: Cycle/Stuff Counter	The coding of this octet depends on the PLCP frame format. For DS1 and E3 PLCP formats, this octet is programmed with all zeros. For the DS3 PLCP format, this octet indicates the number of stuff nibbles (13 or 14) at the end of each PLCP frame. The C1 value is varied in a three frame cycle where the first frame always	Interprets the trailer length according to the selected PLCP frame format and the received C1 code.

Overhead Field	Transmit Operation	Receive Operation
	contains 13 stuff nibbles, the second frame always contains 14 nibbles, and the third frame contains 13 or 14 nibbles. The stuffing may be varied by a nibble so that the PLCP frame rate can be locked to an external 8 kHz timing reference from REF8KI, a looptimed 8 kHz reference, or fixed stuffing via the FIXSTUFF bit in the SPLT Configuration Register. See Table 31. For the G.751 E3 PLCP format, this octet indicates the number of stuff octets (17 to 21) at the end of the PLCP frame. Depending on the alignment of the G.751 E3 frame to the E3 PLCP frame, 18, 19 or 20 octets are nominally stuffed. The stuffing may be varied by ±1 octet so that the PLCP frame rate can be locked to an external 8 kHz timing reference from REF8KI. The S/UNI-QJET also supports fixed timing using the FIXSTUFF bit in the SPLT Configuration Register. See Table 32.	

Table 30 - PLCP Path Overhead Identifier Codes

POI	POI Code (Hex)
P11	2C
P10	29

POI	POI Code (Hex)
P9	25
P8	20
P7	1C
P6	19
P5	15
P4	10
P3	0D
P2	08
P1	04
P0	01

Table 31 - DS3 PLCP Trailer Length

C1(Hex)	Frame/Trailer Length
FF	1 (13 Nibbles)
00	2 (14 Nibbles)
66	3 (13 Nibbles)
99	3 (14 Nibbles)

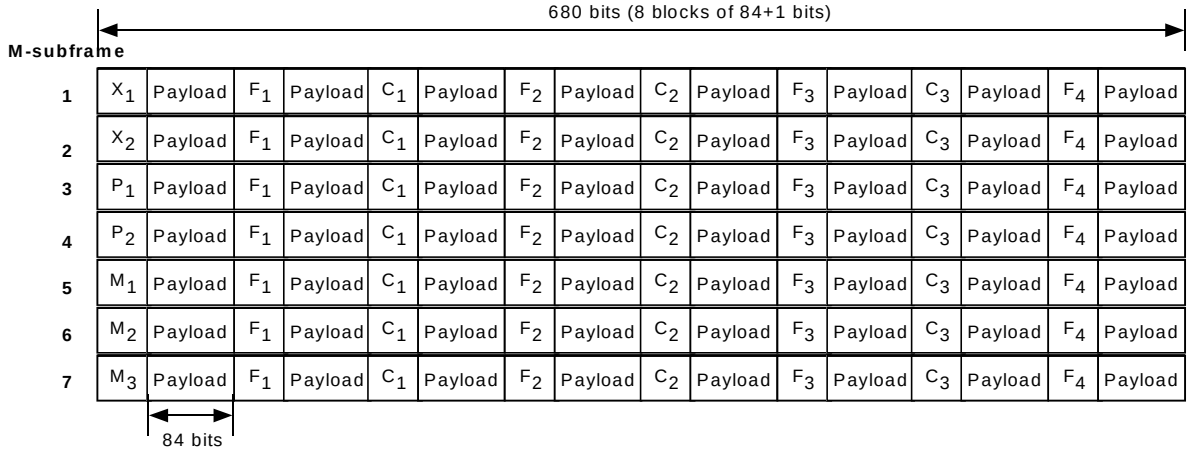
Table 32 - E3 PLCP Trailer Length

C1(Hex)	Trailer Length
3B	17 octets
4F	18 octets
75	19 octets
9D	20 octets
A7	21 octets

12.4 DS3 Frame Format

The S/UNI-QJET supports both M23 and C-bit parity DS3 framing formats. This format can be extended to support direct byte mapping or PLCP mapping of ATM cells. An overview of the DS3 frame format is shown in Figure 16.

Figure 16 - DS3 Frame Structure



The DS3 receiver decodes a B3ZS-encoded signal and provides indications of line code violations (LCVs). The B3ZS decoding algorithm and the LCV definition are software selectable.

While in-frame, the DS3 receiver continuously checks for line code violations, M-bit or F-bit framing bit errors, and P-bit parity errors. When C-bit parity mode is selected, both C-bit parity errors and far end block errors are accumulated.

When the C-bit parity framing format is detected, both the far end alarm and control (FEAC) channel and the path maintenance data link are extracted. HDLC messages in the Path Maintenance Data Link are received by an internal data link receiver.

The DS3 transmitter allows for the insertion of the overhead bits into a DS3 bit stream and produces a B3ZS-encoded signal. Status signals such as far end receive failure (FERF), the alarm indication signal (AIS) and the idle signal can be inserted when the transmission of these signals is enabled

The processing of the overhead bits in the DS3 frame is described in the following table. In the transmit direction, the overhead bits can be inserted on a bit-by-bit basis from a user supplied data stream using the TOH[x], TOHINS[x],

TOHFP[x], and TOHCLK[x] signals. In the receive direction, most of the overhead bits our brought out serially on the ROH[x] data stream.

Table 33 - DS3 Frame Overhead Operation

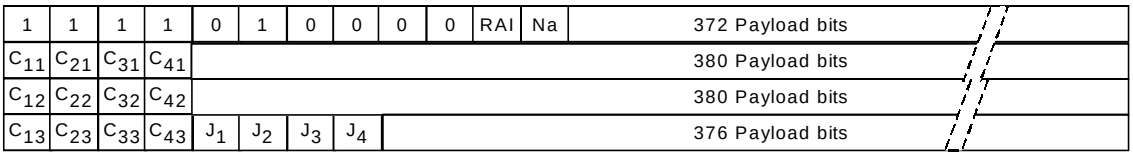
Control Bit	Transmit Operation	Receive Operation
Xx: X-Bit Channel	Inserts the FERF signal on the X-bits.	Monitors and detects changes in the state of the FERF signal on the X-bits.
Px: P-Bit Channel	Calculates the parity for the payload data over the previous M-frame and inserts it into the P1 and P2 bit positions.	Calculates the parity for the received payload. Errors are accumulated in internal registers.
Mx: M-Frame Alignment Signal	Generates the M-frame alignment signal (M1=0, M2=1, M3=0).	Finds the M-frame alignment by searching for the F-bits and the M-bits. Out-of-frame is removed if the M-bits are correct for three consecutive M-frames while no discrepancies have occurred in the F-bits.
Fx: M-subframe Alignment Signal	Generates the M-subframe signal (F1=1, F2=0, F3=0, F4=1).	Finds M-frame alignment by searching for the F-bits and the M-bits. Out-of-frame is removed if the M-bits are correct for three consecutive M-frames while no discrepancies have occurred in the F-bits.
Cx: C-Bit Channels	<u>M23 Operation:</u> The C bits are passed through transparently in M23 framer only mode except for the C-bit Parity ID bit which toggles every M-frame. In M23 ATM applications, the C bits other than the Parity ID bit are forced to logic 1. <u>C-bit Parity Operation:</u> The C-bit Parity ID bit is forced to logic 1. The second C-bit in M-subframe 1 is set to logic 1. The third C-bit in M-subframe 1 provides a far-	The state of the C-bit parity ID bit is stored in a register. This bit indicates whether an M23 or C-bit parity format is received. <u>C-bit Parity Operation:</u> The FEAC channel on the third C-bit in M-subframe 1 is detected by the RBOC block. Path parity errors and FEBEs on the C-bits in M-subframes 3 and 4 are accumulated in counters. The path maintenance datalink signal is extracted by the receive HDLC controller.

Control Bit	Transmit Operation	Receive Operation
	end alarm and control (FEAC) signal. The FEAC channel is sourced by the XBOC block. The 3 C-bits in M-subframe 3 carry path parity information. The value of these 3 C-bits is the same as that of the P-bits. The 3 C-bits in M-subframe 4 are the FEBE bits. The 3 C-bits in M-subframe 5 contain the 28.2 Kbit/s path maintenance datalink. The remaining C-bits are unused and set to logic 1.	

12.5 G.751 E3 Frame Format

The S/UNI-QJET provides support for the G.751 E3 frame format. This format can be extended to allow for direct byte mapping or PLCP mapping of ATM cells. The G.751 E3 frame format is shown in Figure 17.

Figure 17 - G.751 E3 Frame Structure



The processing of the overhead bits in the G.751 E3 frame is described in the following table. In the transmit direction, the overhead bits can be inserted on a bit-by-bit basis from a user supplied data stream using the TOH[x], TOHINS[x], TOHFP[x], and TOHCLK[x] signals. In the receive direction, most of the overhead bits are brought out serially on the ROH[x] data stream.

When used to transport ATM cells in either ATM direct mapping mode or with PLCP framing, bits 13, 14, 15 and 16 of the E3 frame (directly following the RAI and Na bits) are set to 1, 1, 0 and 0.

Table 34 - G.751 E3 Frame Overhead Operation

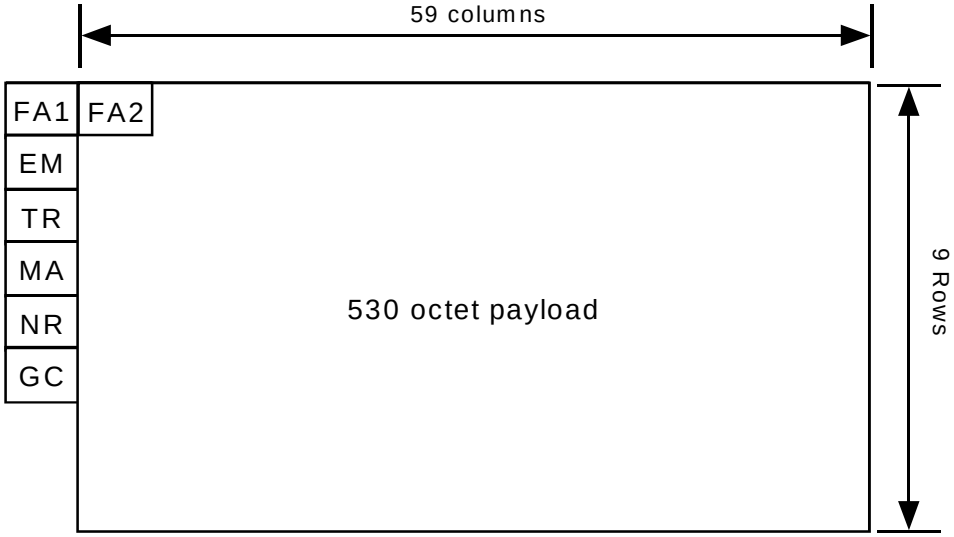
Control Bit	Transmit Operation	Receive Operation
Frame Alignment Signal	Inserts the frame alignment signal 1111010000b.	Finds frame alignment by searching for the frame alignment signal. When the pattern has been detected for three consecutive frames, an in-frame condition is declared. When errors are detected in four consecutive frames, an out-of-frame condition is declared.
RAI: Remote Alarm Indication	Optionally asserts the RAI signal under a register control or when LOS, OOF, AIS and LCD conditions are detected.	Extracts the RAI signal and outputs it on the ROH output pin. The state of the RAI signal is also written to a register bit.
Na: National Use Bit	Asserts the National Use bit under a register control or from the internal HDLC controller.	Extracts the National Use bit and stores the value in a register bit.
Cjk: Justification Service Bits	When the device is configured as an E3 G.751 framer device, the Justification Service Bits can be inserted on the TDATI[x] input pin the same way as normal payload data. When the device is configured for ATM application, the Justification Service Bits are used as payload bits.	Extracts the Justification Service Bits on the ROH output pin when the Cjk bits are configured as overhead.
Jk: Tributary Justification Bits	When the device is configured as a E3 G.751 framer, the Tributary Justification Bits can be inserted on the TDATI[x] input pin the same way as normal payload data. When the device is configured for ATM application, the Tributary Justification Bits are used a	Extracts the Tributary Justification Bits on the ROH output pin when the Jk bits are configured as overhead.

Control Bit	Transmit Operation	Receive Operation
	payload bits.	

12.6 G.832 E3 Frame Format

The S/UNI-QJET provides support for the G.832 E3 frame format. This format can be extended to allow for direct byte mapping of ATM cells. The G.832 E3 frame format is shown in Figure 18.

Figure 18 - G.832 E3 Frame Structure



The processing of the overhead bits in the G.832 E3 frame is described in the following table. In the transmit direction, the overhead bits can be inserted on a bit-by-bit basis from a user supplied data stream using the TOH[x], TOHINS[x], TOHFP[x], and TOHCLK[x] signals. In the receive direction, the overhead bits are brought out serially on the ROH[x] data stream.

Table 35 - G.832 E3 Frame Overhead Operation

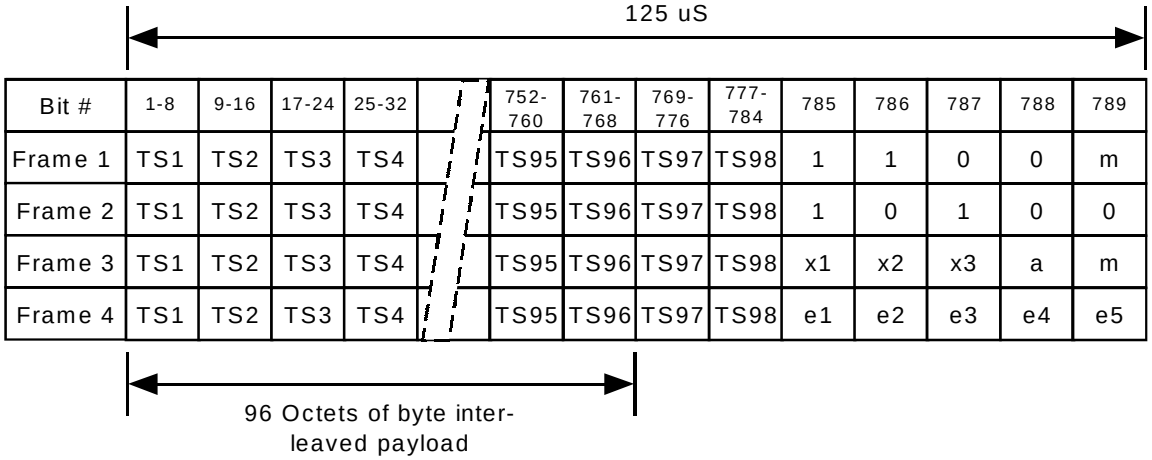
Control	Transmit Operation	Receive Operation
FA1, FA2: Frame Alignment Pattern	Inserts the G.832 E3 frame alignment pattern (F628H).	Searches the receive stream for the G.832 E3 frame alignment pattern. When the pattern is detected for two consecutive frames, an in-frame condition is declared. Note that there is no ATM cell alignment with the G.832

Control	Transmit Operation	Receive Operation
		E3 frame. Therefore cell delineation must be performed to locate the ATM cell boundaries.
EM: Error Monitor, BIP-8	Inserts the calculated BIP-8 by computing even parity over all transmit bits, including the overhead bits of the previous 125 µs frame.	Computes the incoming BIP-8 value over one 125 µs frame. The result is held and compared against the value in the EM byte of the subsequent frame.
TR: Trail Trace	Inserts the 16 byte trail access point identifier specified in internal registers.	Extracts the repetitive trail access point identifier and verifies that the same pattern is received. Compares the received pattern to the expected pattern programmed in a register.
MA: Maintenance and Adaptation Byte	Inserts the FERF, FEBE, Payload Type bits, Tributary Unit Multiframe Indicator bits and the Timing Marker bit as programmed in a register or as indicated by detection of receive OOF or BIP-8 errors.	Extracts and reports the FERF bit value when it has been the same for 3 or 5 consecutive frames. S/UNI-QJET also extracts and accumulates FEBE occurrences and extracts the Payload Type, Tributary Unit Multiframe, and Timing Market indicator bits and reports them through microprocessor accessible registers.
NR: Network Operator Byte	Inserts the Network Operator byte from the TOH overhead stream or optionally from the TDPR. All 8 bits of the Network Operator byte are inserted from TOH or from the TDPR.	Extracts the Network Operator byte and outputs it on ROH or optionally terminates it in the RDLC. All 8 bits of the Network Operator byte are extracted and presented on ROH or to the RDLC.
GC: General Purpose Communication Channel	Inserts the GC byte from the TOH overhead stream or optionally from the TDPR block.	Extracts the GC byte and outputs it on ROH or optionally terminates it in the RDLC block.

12.7 J2 Frame Format

The S/UNI-QJET provides support for the G.704 and NTT J2 frame format. This format can be extended to allow for direct byte mapping of ATM cells as specified in G.804. The J2 frame format consists of 789 bits frames each 125 us long, consisting of 96 bytes of payload, 2 reserved bytes, and 5 F-bits. The frames are grouped into 4 frame multiframes as shown in Figure 19.

Figure 19 - J2 Frame Structure



Bit #	1-8	9-16	17-24	25-32		752-760	761-768	769-776	777-784	785	786	787	788	789
Frame 1	TS1	TS2	TS3	TS4		TS95	TS96	TS97	TS98	1	1	0	0	m
Frame 2	TS1	TS2	TS3	TS4		TS95	TS96	TS97	TS98	1	0	1	0	0
Frame 3	TS1	TS2	TS3	TS4		TS95	TS96	TS97	TS98	x1	x2	x3	a	m
Frame 4	TS1	TS2	TS3	TS4		TS95	TS96	TS97	TS98	e1	e2	e3	e4	e5

The J2 framer decodes a unipolar or B8ZS encoded signal and frames to the resulting 6,312 Kbit/s J2 bit stream. Once in frame, the J2 framer provides indications of frame and multiframe boundaries and marks overhead bits, x-bits, m-bits and reserved channels (TS97 and TS98). Indications of loss of signal, bipolar violations, excessive zeroes, change of frame alignment, framing errors, and CRC errors are provided and accumulated in internal counters.

The J2 transmitter inserts the overhead bits into a J2 bit stream and produces a B8ZS-encoded signal. The J2 transmitter adheres to the framing format specified in G.704 and NTT Technical Reference for High Speed Digital Leased Circuit Services.

The processing of the overhead bits in the J2 frame is described in the following table. In the transmit direction, the overhead bits can be inserted on a bit-by-bit basis from a user supplied data using the TOH[x], TOHINS[x], TOHFP[x], and TOHCLK[x] signals. In the receive direction, the overhead bits are brought out serially on the ROH[x] data stream.

Table 36 - J2 Frame Overhead Operation

Control	Transmit Operation	Receive Operation
TS1-TS96: Byte Interleaved Payload	Inserts the ATM cells into TS1 to TS96 octets.	Extracts the ATM cell octet payload and performs cell delineation.
TS97-TS98: Signaling channels	Inserts the signaling bytes from either register bits or from the TOH and TOHINS inputs. These bits can be optionally inserted via TDATI input when in framer only mode.	Extracts signaling bytes on the ROH output.
Frame Alignment Signal	Inserts the frame alignment signal automatically.	Finds J2 frame alignment by searching for the frame alignment signal.
M-bits: 4kHz Data Link	Inserts the 4 KHz data link signal from the internal HDLC controller or from the bit oriented code generator.	Extracts the 4 KHz data link signal for the internal HDLC controller.
X-bits: Spare Bits	Inserts the spare bits via register bits or via TOH and TOHINS input pins.	Extracts and presents the x-bits on register bits. The X-bit states can be debounced and presented on the ROH output pin. An interrupt change can be generated to signal a change in the X-bit state.
A-bit: Remote Loss of Frame Indication	Inserts the A-bit via register bit. The A-bit can be optionally be asserted when the J2 framer is in loss of frame condition.	Extracts and presents the A-bit on a register bit. The A-bit state can be debounced and presented on the ROH output pin. An interrupt can be generated to signal a change in the A-bit state.
E1-E5: CRC-5 Check Sequence	Automatically calculates and inserts the CRC-5 check sequence.	Calculates the CRC-5 check sequence for the received data stream. Discrepancies with the received CRC-5 code can be configured to generate an interrupt. CRC-5 errors are accumulated in an internal counter.

12.8 S/UNI-QJET Cell Data Structure

ATM cells may be passed to/from the S/UNI-QJET using a 26 word data structure, a 27 word data structure, a 52 word, or a 53 word data structure. These data structures are shown in Figure 20, Figure 21, Figure 22, and Figure 23.

Figure 20 - 16-bit Wide, 26 Word Structure

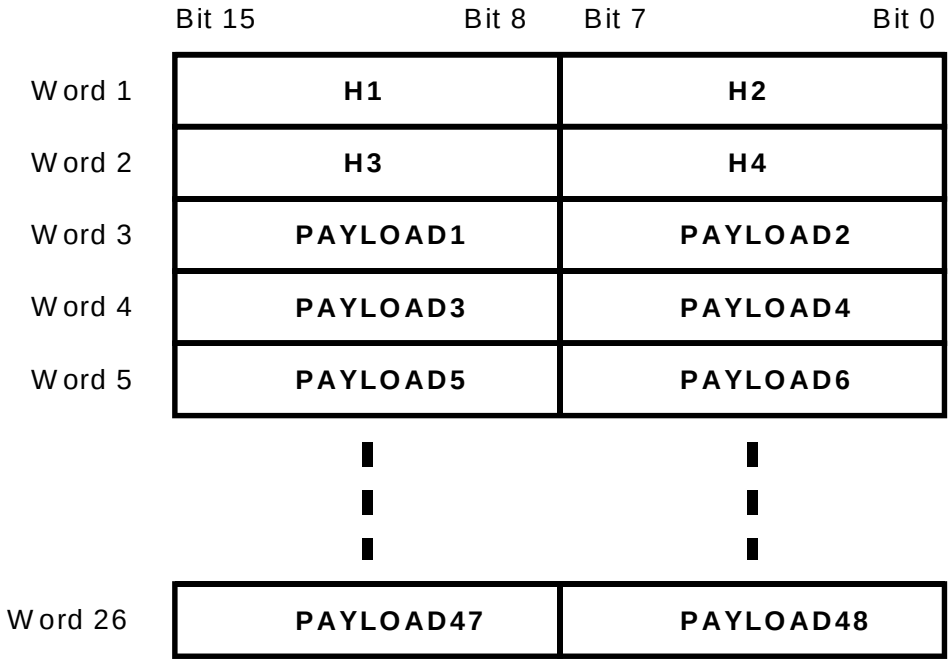
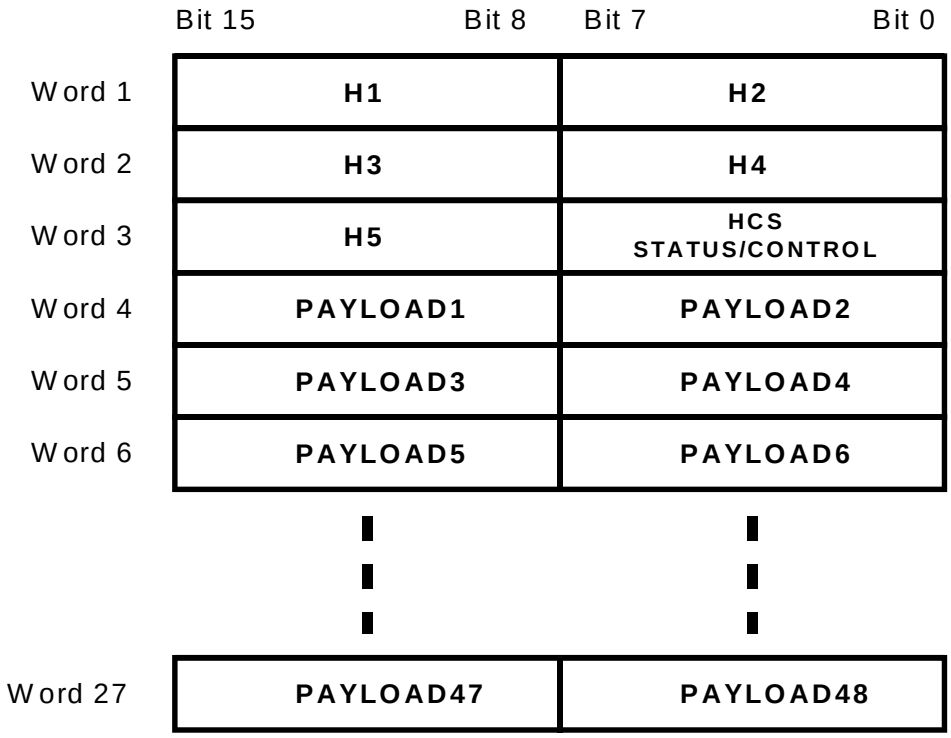


Figure 21 - 16-bit Wide, 27 Word Structure



The 16-bit SCI-PHY compliant data structure is selected when the ATM8 input is tied low. Bit 15 of each word is the most significant bit (which corresponds to the first bit transmitted or received). Selection between the 26 word and 27 word structure is done with the DS27_53 register bit in the S/UNI-QJET Configuration 1 register. The 26 word structure is chosen when DS27_53 is set to logic 0. The 27 word structure is chosen when DS27_53 is set to logic 1. The start of cell indication input and output (TSOC and RSOC) are coincident with Word 1 (containing the first two header octets). The header check sequence octet (HCS) is only passed through the 27 word structure. Word 3 of this structure contains the HCS octet in bits 15 to 8.

In the receive direction with the 27 word structure, the lower 8 bits of Word 3 contain the HCS status octet. An all-zeros pattern in these 8 bits indicates that the associated header is error free. An all-ones pattern indicates that the header contains an uncorrectable error (if the HCSPASS bit in the RXCP-50 Configuration 2 Register is set to logic zero, the all-ones pattern will never be passed in this structure). An alternating ones and zeros pattern (xxAA) indicates that the header contained a correctable error. In this case the header passed through the structure is the "corrected" header.

In the transmit direction, with the 27 word structure, the HCSB bit in the TXCP-50 Configuration 1 register determines whether the HCS is calculated internally or is inserted directly from the upper 8 bits of Word 3. The lower 8 bits of Word 3 contain the HCS control octet. The HCS control octet is an error mask that allows the insertion of one or more errors in the HCS octet. A logic one in a given bit position causes the inversion of the corresponding HCS bit position (for example a logic one in bit 7 causes the most significant bit of the HCS to be inverted).

With the 26 word structure, if the HCSB bit in the TXCP-50 is logic 1, then no HCS byte is inserted on the data read from the Utopia interface or on the Idle cells. In such a configuration, the RXCP-50 should be configured to pass the 26 word output without requiring cell delineation by setting the CCDIS bit to logic 1. This setting is useful for passing arbitrary payload through the transmit and receive Utopia interfaces.

Figure 22 - 8-bit Wide, 52 Word Structure

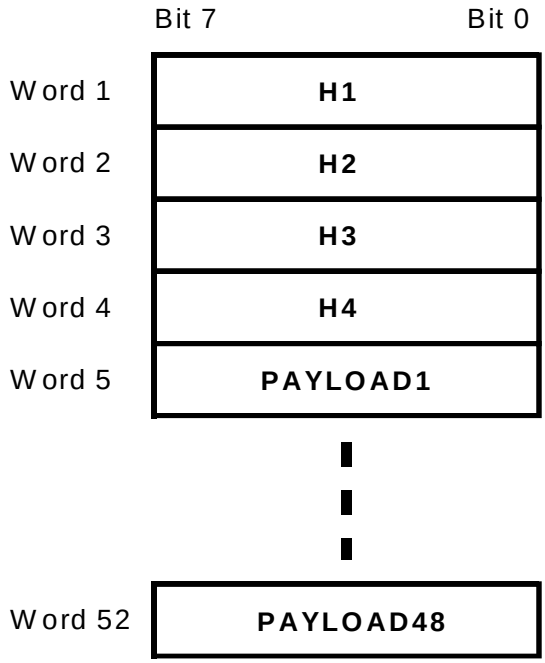
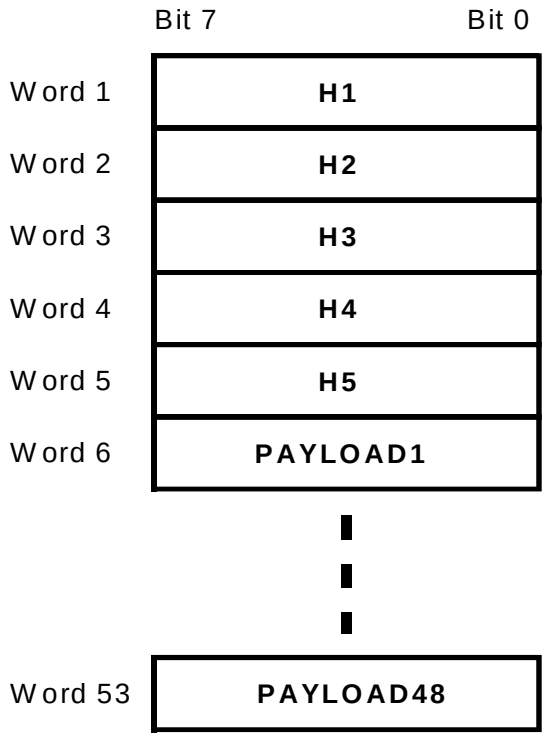


Figure 23 - 8-bit Wide, 53 Word Structure



The 8-bit SCI-PHY compliant data structure is selected when the ATM8 input is tied high. Bit 7 of each word is the most significant bit (which corresponds to the first bit transmitted or received). Selection between the 52-byte and 53-byte structures is done by the DS27_53 register bit in the S/UNI-QJET Configuration 1 register. The 52 byte structure is chosen when DS27_53 is set to logic 0. The 53 byte structure is chosen when DS27_53 is set to logic 1. The start of cell indication input and output (TSOC and RSOC) are coincident with Word 1 (containing the first cell header octet). The header check sequence octet (HCS) is passed through the 53 byte structure. Word 5 of this structure contains the HCS octet.

In the receive direction, cells containing "detected and uncorrected" header errors are dropped when the HCSPASS bit in the RXCP-50 Configuration 2 Register is set to logic zero. No HCS status information is passed within this data structure. Cells with error free headers and "detected and corrected" headers are passed when HCSPASS and DISCOR are logic zero. Cells containing uncorrectable HCS errors are dropped while the HCSPASS bit is set to logic zero. Error free headers, "detected and corrected" headers, and "detected and uncorrected" headers are passed when HCSPASS is a logic one.

In the receive direction, idle cells are dropped when the IDLEPASS bit in the RXCP-50 Configuration 2 Register is set to a logic 0. No cells are passed when the S/UNI-QJET is in the PLCP loss of frame defect state (for PLCP based transmission), or when the S/UNI-QJET is in the out of cell delineation defect state (for non-PLCP based transmission).

In the transmit direction, the HCSB bit in the TXCP-50 Configuration 1 Register determines whether the HCS is calculated internally or is inserted directly from Word 5. For the 52 byte structure, if the HCSB bit in the TXCP-50 is logic 1, then no HCS byte is inserted and the TXCP-50 will only transmit the data present on the 52 words. In such a configuration, the RXCP-50 should be configured to pass the 52 word output without requiring cell delineation by setting the CCDIS bit to logic 1. This setting is useful for passing arbitrary payload through the transmit and receive Utopia interfaces.

12.9 Resetting the RXFF and TXFF FIFOs

Resetting the receive and transmit FIFOs can be accomplished using the FIFORST bits (RXCP-50 FIFO/UTOPIA Control & Config, TXCP-50 Configuration 1 registers). When resetting, the FIFORST bit should be written with a logic 1, and held for two or more clock cycles (the longer of two Utopia clock cycles or 16 line clock cycles). After de-asserting FIFORST, data can be safely written to the TXFF after two or more clock cycles have passed.

12.10 Servicing Interrupts

The S/UNI-QJET will assert INTB to logic 0 when a condition which is configured to produce an interrupt occurs. To find which condition caused this interrupt to occur, the procedure outlined below should be followed:

1. Read the INT[4:1] bits of the S/UNI-QJET Clock Activity Monitor and Interrupt Identification register (007H) to identify which quadrant of the S/UNI-QJET produced the interrupt. For example, a logic one on the INT[3] register bit indicates that quadrant number 3 of the S/UNI-QJET produced the interrupt.

2. Having identified the quadrant which produced the interrupt, read the S/UNI-QJET Interrupt Status Register (005H, 105H, 205H, and 305H) to identify which block in the quadrant produced the interrupt. For example, a logic one on the TDPRI register bit in register 205H indicates that the TDPR block in quadrant number 3 of the S/UNI-QJET produced the interrupt.

3. Service the interrupt.

4. If the INTB pin is still logic 0, then there are still interrupts to be serviced. Otherwise, all interrupts have been serviced. Wait for the next assertion of INTB.

12.11 Using the Performance Monitoring Features

The PMON and CPPM blocks are provided for performance monitoring purposes. The RXCP-50 and TXCP-50 also contain performance monitor registers. The PMON block is used to monitor DS3, E3, and J2 performance primitives while the CPPM is used to monitor PLCP and idle-cell-based primitives. The RXCP-50 is used to monitor received cell primitives, and the TXCP-50 is used to monitor transmit cell primitives. The counters in the PMON block have been sized as not to saturate if polled every second. The counters in the CPPM blocks have been sized as not to saturate if polled every 1/2 second at line rates up to 44.736 MHz. The counters in the RXCP-50 and TXCP-50 have been sized to not saturate if polled every second at line rates up to 44.736 MHz.

The DS3, E3, and J2 primitives can be accumulated independently of the PLCP and cell-based primitives. An accumulation interval is initiated by writing to one of the PMON event counter register addresses. After writing to a PMON count register, a number of RCLK clock periods (3 for J2 mode, 255 for DS3 mode, 500 for G.832 E3 mode, and 3 for G.751 E3 mode) must be allowed to elapse to permit the PMON counter values to be properly transferred. The PMON registers may then be read.

PLCP and cell-based primitives can be accumulated independent of the DS3, E3, or J2 primitives. An accumulation interval is initiated by writing to one of the CPPM event counter register addresses. After writing to a CPPM count register, a maximum of 67 RCLK clock periods must be allowed to elapse to permit all the CPPM values to be properly transferred. The CPPM registers may then be read.

The RXCP-50 and TXCP-50 accumulate cell-based primitives such as received cells, corrected cell headers, uncorrected cell headers, and transmitted cells. An accumulation interval in each block is initiated by writing to one of the RXCP-50 or TXCP-50 event counter register addresses. After writing to a count register, a maximum of 67 RCLK or TICLK clock periods must be allowed to elapse to permit all the RXCP-50 or TXCP-50 values to be properly transferred. The RXCP-50 or TXCP-50 count registers may then be read.

Writing to the S/UNI-QJET Identification, Master Reset, and Global Monitor Update register causes the PMON, CPPM, RXCP-50, and TXCP-50 performance event counters to latch and a new accumulation period to start in all four quadrants of the S/UNI-QJET. A maximum of 67 RCLK[x] clock periods

must be allowed to elapse to permit all the event count registers to be properly transferred.

12.12 Using the Internal FDL Transmitter

It is important to note that the access rate to the TDPR registers is limited by the rate of the internal high-speed system clock selected by the LINESYSCLK register bit of the S/UNI-QJET Misc. register (09BH, 19BH, 29BH, 39BH). Consecutive accesses to the TDPR Configuration, TDPR Interrupt Status/UDR Clear, and TDPR Transmit Data register should be accessed (with respect to WRB rising edge and RDB falling edge) at a rate no faster than 1/8 that of the selected TDPR high-speed system clock. This time is used by the high-speed system clock to sample the event, write the FIFO, and update the FIFO status. Instantaneous variations in the high-speed reference clock frequencies (e.g. jitter in the line clock) must be considered when determining the procedure used to read and write the TDPR registers.

Upon reset of the S/UNI-QJET, the TDPR should be disabled by setting the EN bit in the TDPR Configuration Register to logic 0 (default value). An HDLC all-ones Idle signal will be sent while in this state. The TDPR is enabled by setting the EN bit to logic 1. The FIFOCLR bit should be set and then cleared to initialize the TDPR FIFO. The TDPR is now ready to transmit.

To initialize the TDPR, the TDPR Configuration Register must be properly set. If FCS generation is desired, the CRC bit should be set to logic 1. If the block is to be used in interrupt driven mode, then interrupts should be enabled by setting the FULLE, OVRE, UDRE, and LFILLE bits in the TDPR Interrupt Enable register to logic 1. The TDPR operating parameters in the TDPR Upper Transmit Threshold and TDPR Lower Interrupt Threshold registers should be set to the desired values. The TDPR Upper Transmit Threshold sets the value at which the TDPR automatically begins the transmission of HDLC packets, even if no complete packets are in the FIFO. Transmission will continue until current packet is transmitted and the number of bytes in the TDPR FIFO falls to, or below, this threshold level. The TDPR will always transmit all complete HDLC packets (packets with EOM attached) in its FIFO. Finally, the TDPR can be enabled by setting the EN bit to logic 1. If no message is sent after the EN bit is set to logic 1, continuous flags will be sent.

The TDPR can be used in a polled or interrupt driven mode for the transfer of data. In the polled mode the processor controlling the TDPR must periodically read the TDPR Interrupt Status register to determine when to write to the TDPR Transmit Data register. In the interrupt driven mode, the processor controlling the TDPR uses the INTB output, the S/UNI-QJET Clock Activity Monitor and

Interrupt Identification register, and the S/UNI-QJET Interrupt Status register to identify TDPR interrupts which determine when writes can or must be done to the TDPR Transmit Data register.

Interrupt Driven Mode

The TDPR automatically transmits a packet once it is completely written into the TDPR FIFO. The TDPR also begins transmission of bytes once the FIFO level exceeds the programmable Upper Transmit Threshold. The CRC bit can be set to logic 1 so that the FCS is generated and inserted at the end of a packet. The TDPR Lower Interrupt Threshold should be set to such a value that sufficient warning of an underrun is given. The FULLE, LFILLE, OVRE, and UDRE bits are all set to logic 1 so an interrupt on INTB is generated upon detection of a FIFO full state, a FIFO depth below the lower limit threshold, a FIFO overrun, or a FIFO underrun. The following procedure should be followed to transmit HDLC packets:

1. Wait for data to be transmitted. Once data is available to be transmitted, then go to step 2.

2. Write the data byte to the TDPR Transmit Data register.

3. If all bytes in the packet have been sent, then set the EOM bit in the TDPR Configuration register to logic 1. Go to step 1.

4. If there are more bytes in the packet to be sent, then go to step 2.

While performing steps 1 to 4, the processor should monitor for interrupts generated by the TDPR. When an interrupt is detected, the TDPR Interrupt Routine detailed in the following text should be followed immediately.

The TDPR will force transmission of the packet information when the FIFO depth exceeds the threshold programmed with the UTHR[6:0] bits in the TDPR Upper Transmit Threshold register. Unless an error condition occurs, transmission will not stop until the last byte of all complete packets is transmitted and the FIFO depth is at or below the threshold limit. The user should watch the FULLI and LFILLI interrupts to prevent overruns and underruns.

TDPR Interrupt Routine

Upon assertion of INTB, the source of the interrupt must first be identified by reading the S/UNI-QJET Clock Activity Monitor and Interrupt Identification register (007H) and the S/UNI-QJET Interrupt Status registers (005H, 105H,

205H, 305H). Once the source of the interrupt has been identified as TDPR, then the following procedure should be carried out:

1. Read the TDPR Interrupt Status register.

2. If UDRI=1, then the FIFO has underrun and the last packet transmitted has been corrupted and needs to be retransmitted. When the UDRI bit transitions to logic 1, one Abort sequence and continuous flags will be transmitted. The TDPR FIFO is held in reset state. To reenable the TDPR FIFO and to clear the underrun, the TDPR Interrupt Status/UDR Clear register should be written with any value.

3. If OVRI=1, then the FIFO has overflowed. The packet which the last byte written into the FIFO belongs to has been corrupted and must be retransmitted. Other packets in the FIFO are not affected. Either a timer can be used to determine when sufficient bytes are available in the FIFO or the user can wait until the LFILLI interrupt is set, indicating that the FIFO depth is at the lower threshold limit.

   If the FIFO overflows on the packet currently being transmitted (packet is greater than 128 bytes long), OVRI is set, an Abort signal is scheduled to be transmitted, the FIFO is emptied, and then flags are continuously sent until there is data to be transmitted. The FIFO is held in reset until a write to the TDPR Transmit Data register occurs. This write contains the first byte of the next packet to be transmitted.

4. If FULLI=1 and FULL=1, then the TDPR FIFO is full and no further bytes can be written. When in this state, either a timer can be used to determine when sufficient bytes are available in the FIFO or the user can wait until the LFILLI interrupt is set, indicating that the FIFO depth is at the lower threshold limit.

   If FULLI=1 and FULL=0, then the TDPR FIFO had reached the FULL state earlier, but has since emptied out some of its data bytes and now has space available in its FIFO for more data.

5. If LFILLI=1 and BLFILL=1, then the TDPR FIFO depth is below its lower threshold limit. If there is more data to transmit, then it should be written to the TDPR Transmit Data register before an underrun occurs. If there is no more data to transmit, then an EOM should be set at the end of the last packet byte. Flags will then be transmitted once the last packet has been transmitted.

If LFILLI=1 and BLFILL=0, then the TDPR FIFO had fallen below the lower-threshold state earlier, but has since been refilled to a level above the lower-threshold level.

Polling Mode

The TDPR automatically transmits a packet once it is completely written into the TDPR FIFO. The TDPR also begins transmission of bytes once the FIFO level exceeds the programmable Upper Transmit Threshold. The CRC bit can be set to logic 1 so that the FCS is generated and inserted at the end of a packet. The TDPR Lower Interrupt Threshold should be set to such a value that sufficient warning of an underrun is given. The FULLE, LFILLE, OVRE, and UDRE bits are all set to logic 0 since packet transmission is set to work with a periodic polling procedure. The following procedure should be followed to transmit HDLC packets:

1. Wait until data is available to be transmitted, then go to step 2.

2. Read the TDPR Interrupt Status register.

3. If FULL=1, then the TDPR FIFO is full and no further bytes can be written. Continue polling the TDPR Interrupt Status register until either FULL=0 or BLFILL=1. Then, go to either step 4 or 5 depending on implementation preference.

4. If BLFILL=1, then the TDPR FIFO depth is below its lower threshold limit. Write the data into the TDPR Transmit Data register. Go to step 6.

5. If FULL=0, then the TDPR FIFO has room for at least 1 more byte to be written. Write the data into the TDPR Transmit Data register. Go to step 6.

6. If more data bytes are to be transmitted in the packet, then go to step 2.

7. If all bytes in the packet have been sent, then set the EOM bit in the TDPR Configuration register to logic 1. Go to step 1.

12.13 Using the Internal Data Link Receiver

It is important to note that the access rate to the RDLC registers is limited by the rate of the internal high-speed system clock selected by the LINESYSCLK register bit of the S/UNI-QJET Misc. register (09BH, 19BH, 29BH, 39BH). Consecutive accesses to the RDLC Status and RDLC Data registers should be accessed at a rate no faster than 1/10 that of the selected RDLC high-speed system clock. This time is used by the high-speed system clock to sample the

event and update the FIFO status. Instantaneous variations in the high-speed reference clock frequencies (e.g. jitter in the receive line clock) must be considered when determining the procedure used to read RDLC registers.

On power up of the system, the RDLC should be disabled by setting the EN bit in the Configuration Register to logic 0 (default state). The RDLC Interrupt Control register should then be initialized to enable the INT output and to select the FIFO buffer fill level at which an interrupt will be generated. If the INTE bit is not set to logic 1, the RDLC Status register must be continuously polled to check the interrupt status (INTR) bit.

After the RDLC Interrupt Control register has been written, the RDLC can be enabled at any time by setting the EN bit in the RDLC Configuration register to logic 1. When the RDLC is enabled, it will assume the link status is idle (all ones) and immediately begin searching for flags. When the first flag is found, an interrupt will be generated, and a dummy byte will be written into the FIFO buffer. This is done to provide alignment of link up status with the data read from the FIFO. When an abort character is received, another dummy byte and link down status is written into the FIFO. This is done to provide alignment of link down status with the data read from the FIFO. It is up to the controlling processor to check the COLS bit in the RDLC Status register for a change in the link status. If the COLS bit is set to logic 1, the FIFO must be emptied to determine the current link status. The first flag and abort status encoded in the PBS bits is used to set and clear a Link Active software flag.

When the last byte of a properly terminated packet is received, an interrupt is generated. While the RDLC Status register is being read the PKIN bit will be logic 1. This can be a signal to the external processor to empty the bytes remaining in the FIFO or to just increment a number-of-packets-received count and wait for the FIFO to fill to a programmable level. Once the RDLC Status register is read, the PKIN bit is cleared to logic 0 . If the RDLC Status register is read immediately after the last packet byte is read from the FIFO, the PBS[2] bit will be logic 1 and the CRC and non-integer byte status can be checked by reading the PBS[1:0] bits.

When the FIFO fill level is exceeded, an interrupt is generated. The FIFO must be emptied to remove this source of interrupt.

The RDLC can be used in a polled or interrupt driven mode for the transfer of frame data. In the polled mode, the processor controlling the RDLC must periodically read the RDLC Status register to determine when to read the RDLC Data register. In the interrupt driven mode, the processor controlling the RDLC uses the S/UNI-QJET INTB output, the S/UNI-QJET Clock Activity Monitor and

Interrupt Identification register, and the S/UNI-QJET Interrupt Status registers to determine when to read the RDLC Data register.

In the case of interrupt driven data transfer from the RDLC to the processor, the INTB output of the S/UNI-QJET is connected to the interrupt input of the processor. The processor interrupt service routine verifies what block generated the interrupt by reading the S/UNI-QJET Clock Activity Monitor and Interrupt Identification register, and the S/UNI-QJET Interrupt Status registers. Once it has identified that the RDLC has generated the interrupt, it processes the data in the following order:

1. RDLC Status register read. The INTR bit should be logic 1.

2. If OVR = 1, then discard last frame and go to step 1. Overrun causes a reset of FIFO pointers. Any packets that may have been in the FIFO are lost.

3. If COLS = 1, then set the EMPTY FIFO software flag.

4. If PKIN = 1, increment the PACKET COUNT. If the FIFO is desired to be emptied as soon as a complete packet is received, set the EMPTY FIFO software flag. If the EMPTY FIFO software flag is not set, FIFO emptying will delayed until the FIFO fill level is exceeded.

5. Read the RDLC Data register.

6. Read the RDLC Status register.

7. If OVR = 1, then discard last frame and go to step 1. Overrun causes a reset of FIFO pointers. Any packets that may have been in the FIFO are lost.

8. If COLS = 1, then set the EMPTY FIFO software flag.

9. If PKIN = 1, increment the PACKET COUNT. If the FIFO is desired to be emptied as soon as a complete packet is received, set the EMPTY FIFO software flag. If the EMPTY FIFO software flag is not set, FIFO emptying will delayed until the FIFO fill level is exceeded.

10. Start the processing of FIFO data. Use the PBS[2:0] packet byte status bits to decide what is to be done with the FIFO data.

    10.1) If PBS[2:0] = 001, discard data byte read in step 5 and set the LINK ACTIVE software flag.

    10.2) If PBS[2:0] = 010, discard the data byte read in step 5 and clear the LINK ACTIVE software flag.

10.3) If PBS[2:0] = 1XX, store the last byte of the packet, decrement the PACKET COUNT, and check the PBS[1:0] bits for CRC or NVB errors before deciding whether or not to keep the packet.

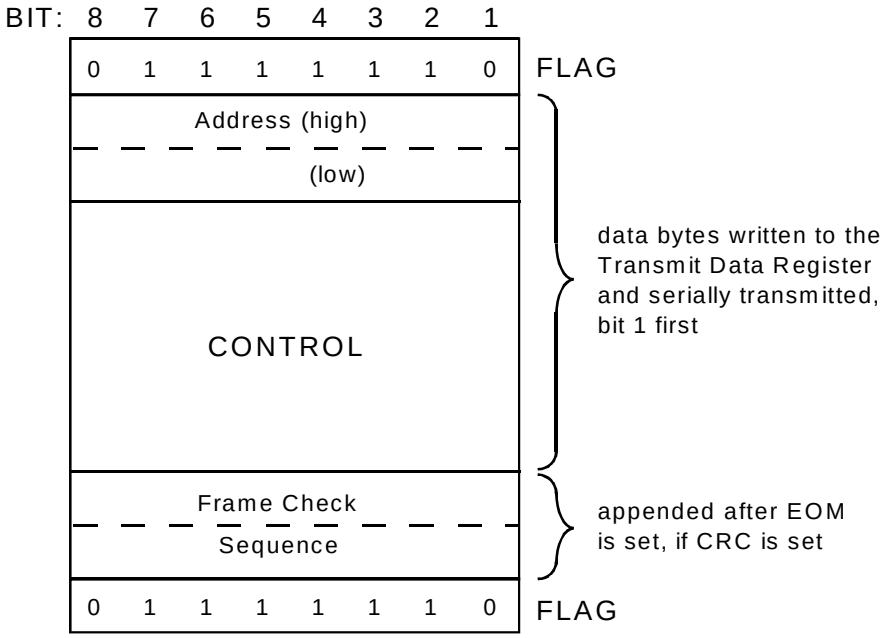
10.4) If PBS[2:0] = 000, store the packet data.

11. If FE = 0 and INTR = 1 or FE = 0 and EMPTY FIFO = 1, go to step 5 else clear the EMPTY FIFO software flag and leave this interrupt service routine to wait for the next interrupt.

The link state is typically a local software variable. The link state is inactive if the RDLC is receiving all ones or receiving bit-oriented codes which contain a sequence of eight ones. The link state is active if the RDLC is receiving flags or data.

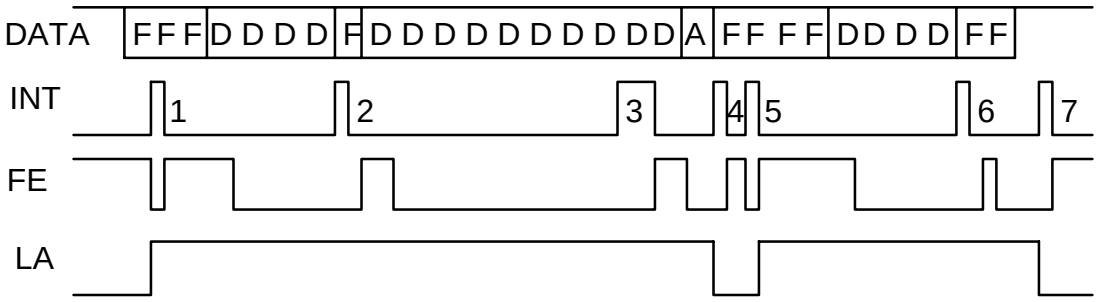
If the RDLC data transfer is operating in the polled mode, processor operation is exactly as shown above for the interrupt driven mode, except that the entry to the service routine is from a timer, rather than an interrupt.

Figure 24 - Typical Data Frame



Bit 1 is the first serial bit to be received. When enabled, the primary, secondary and universal addresses are compared with the high order packet address to determine a match.

Figure 25 - Example Multi-Packet Operational Sequence



F - flag sequence (01111110)

A - abort sequence (01111111)

D - packet data bytes

INT - active high interrupt output

FE - internal FIFO empty status

LA - state of the LINK ACTIVE software flag

Figure 25 shows the timing of interrupts, the state of the FIFO, and the state of the Data Link relative the input data sequence. The cause of each interrupt and the processing required at each point is described in the following paragraphs.

At points 1 and 5 the first flag after all ones or abort is detected. A dummy byte is written in the FIFO, FE goes low, and an interrupt goes high. When the interrupt is detected by the processor it reads the dummy byte, the FIFO becomes empty, and the interrupt is removed. The LINK ACTIVE (LA) software flag is set to logic 1.

At points 2 and 6 the last byte of a packet is detected and interrupt goes high. When the interrupt is detected by the processor, it reads the data and status registers until the FIFO becomes empty. The interrupt is removed as soon as the RDLC Status register is read since the FIFO fill level of 8 bytes has not been exceeded. It is possible to store many packets in the FIFO and empty the FIFO when the FIFO fill level is exceeded. In either case the processor should use this interrupt to count the number of packets written into the FIFO. The packet count or a software time-out can be used as a signal to empty the FIFO.

At point 3 the FIFO fill level of 8 bytes is exceeded and interrupt goes high. When the interrupt is detected by the processor it must read the data and status registers until the FIFO becomes empty and the interrupt is removed.

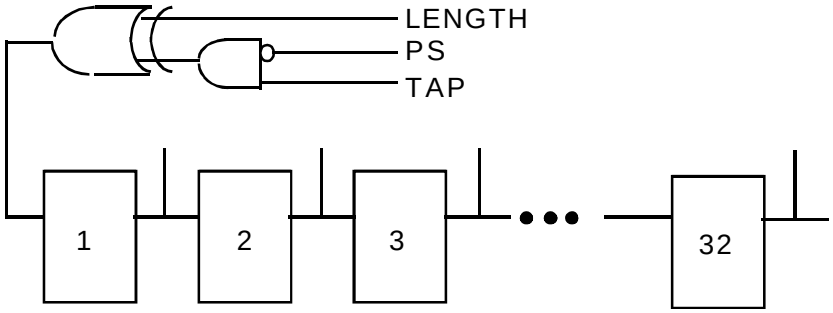
At points 4 or 7 an abort character is detected, a dummy byte is written into the FIFO, and interrupt goes high. When the interrupt is detected by the processor it must read the data and status registers until the FIFO becomes empty and the interrupt is removed. The LINK ACTIVE software flag is cleared.

12.14 PRGD Pattern Generation

A pseudo-random or repetitive pattern can be inserted/extracted in the PLCP payload (if PLCP framing is enabled) or in the DS3, E3, J2, or Arbitrary framing format payload (if PLCP framing is disabled). It cannot be inserted into the ATM cell payload.

The pattern generator can be configured to generate pseudo random patterns or repetitive patterns as shown in Figure 26 below:

Figure 26 - PRGD Pattern Generator



The pattern generator consists of a 32 bit shift register and a single XOR gate. The XOR gate output is fed into the first stage of the shift register. The XOR gate inputs are determined by values written to the length register (PL[4:0]) and the tap register (PT[4:0], when the PS bit is low). When PS is high, the pattern detector functions as a recirculating shift register, with length determined by PL[4:0].

12.14.1 Generating and detecting repetitive patterns

When a repetitive pattern (such as 1-in-8) is to be generated or detected, the PS bit must be set to logic 1. The pattern length register must be set to (N-1), where N is the length of the desired repetitive pattern. Several examples of

programming for common repetitive sequences are given below in the Common Test Patterns section.

For pattern generation, the desired pattern must be written into the PRGD Pattern Insertion registers. The repetitive pattern will then be continuously generated. The generated pattern will be inserted in the output data stream, but the phase of the pattern cannot be guaranteed.

For pattern detection, the PRGD will determine if a repetitive pattern of the length specified in the pattern length register exists in the input stream. It does so by loading the first N bits from the data stream, and then monitoring to see if the pattern loaded repeats itself error free for the subsequent 48 bit periods. It will repeat this process until it finds a repetitive pattern of length N, at which point it begins counting errors (and possibly re-synchronizing) in the same way as for pseudo-random sequences. Note that the PRGD does NOT look for the pattern loaded into the Pattern Insertion registers, but rather automatically detects any repetitive pattern of the specified length. The precise pattern detected can be determined by initiating a PRGD update, setting PDR[1:0] = 00 in the PRGD Control register, and reading the Pattern Detector registers (which will then contain the 32 bits detected immediately prior to the strobe).

12.14.2 Common Test Patterns

The PRGD can be configured to monitor the standardized pseudo random and repetitive patterns described in ITU-T O.151. The register configurations required to generate these patterns and others are indicated in the two tables below:

Table 37 - Pseudo Random Pattern Generation (PS bit = 0)

Pattern Type	TR	LR	IR#1	IR#2	IR#3	IR#4	TINV	RINV
2^3 -1	00	02	FF	FF	FF	FF	0	0
2^4 -1	00	03	FF	FF	FF	FF	0	0
2^5-1	01	04	FF	FF	FF	FF	0	0
2^6 -1	04	05	FF	FF	FF	FF	0	0
2^7 -1	00	06	FF	FF	FF	FF	0	0
2^7 -1 (Fractional T1 LB Activate)	03	06	FF	FF	FF	FF	0	0

2^7 -1 (Fractional T1 LB Deactivate)	03	06	FF	FF	FF	FF	1	1
2^9 -1 (O.153)	04	08	FF	FF	FF	FF	0	0
2^{10} -1	02	09	FF	FF	FF	FF	0	0
2^{11} -1 (O.152, O.153)	08	0A	FF	FF	FF	FF	0	0
2^{15} -1 (O.151)	0D	0E	FF	FF	FF	FF	1	1
2^{17} -1	02	10	FF	FF	FF	FF	0	0
2^{18} -1	06	11	FF	FF	FF	FF	0	0
2^{20} -1 (O.153)	02	13	FF	FF	FF	FF	0	0
2^{20} -1 (O.151 QRSS bit=1)	10	13	FF	FF	FF	FF	0	0
2^{21} -1	01	14	FF	FF	FF	FF	0	0
2^{22} -1	00	15	FF	FF	FF	FF	0	0
2^{23} -1 (O.151)	11	16	FF	FF	FF	FF	1	1
2^{25} -1	02	18	FF	FF	FF	FF	0	0
2^{28} -1	02	1B	FF	FF	FF	FF	0	0
2^{29} -1	01	1C	FF	FF	FF	FF	0	0
2^{31} -1	02	1E	FF	FF	FF	FF	0	0

Table 38 - Repetitive Pattern Generation (PS bit = 1)

Pattern Type	TR	LR	IR#1	IR#2	IR#3	IR#4	TINV	RINV
All ones	00	00	FF	FF	FF	FF	0	0
All zeros	00	00	FE	FF	FF	FF	0	0
Alternating ones/zeros	00	01	FE	FF	FF	FF	0	0
Double alternating ones/zeros	00	03	FC	FF	FF	FF	0	0
3 in 24	00	17	22	00	20	FF	0	0

1 in 16	00	0F	01	00	FF	FF	0	0
1 in 8	00	07	01	FF	FF	FF	0	0
1 in 4	00	03	F1	FF	FF	FF	0	0
Inband loopback activate	00	04	F0	FF	FF	FF	0	0
Inband loopback deactivate	00	02	FC	FF	FF	FF	0	0

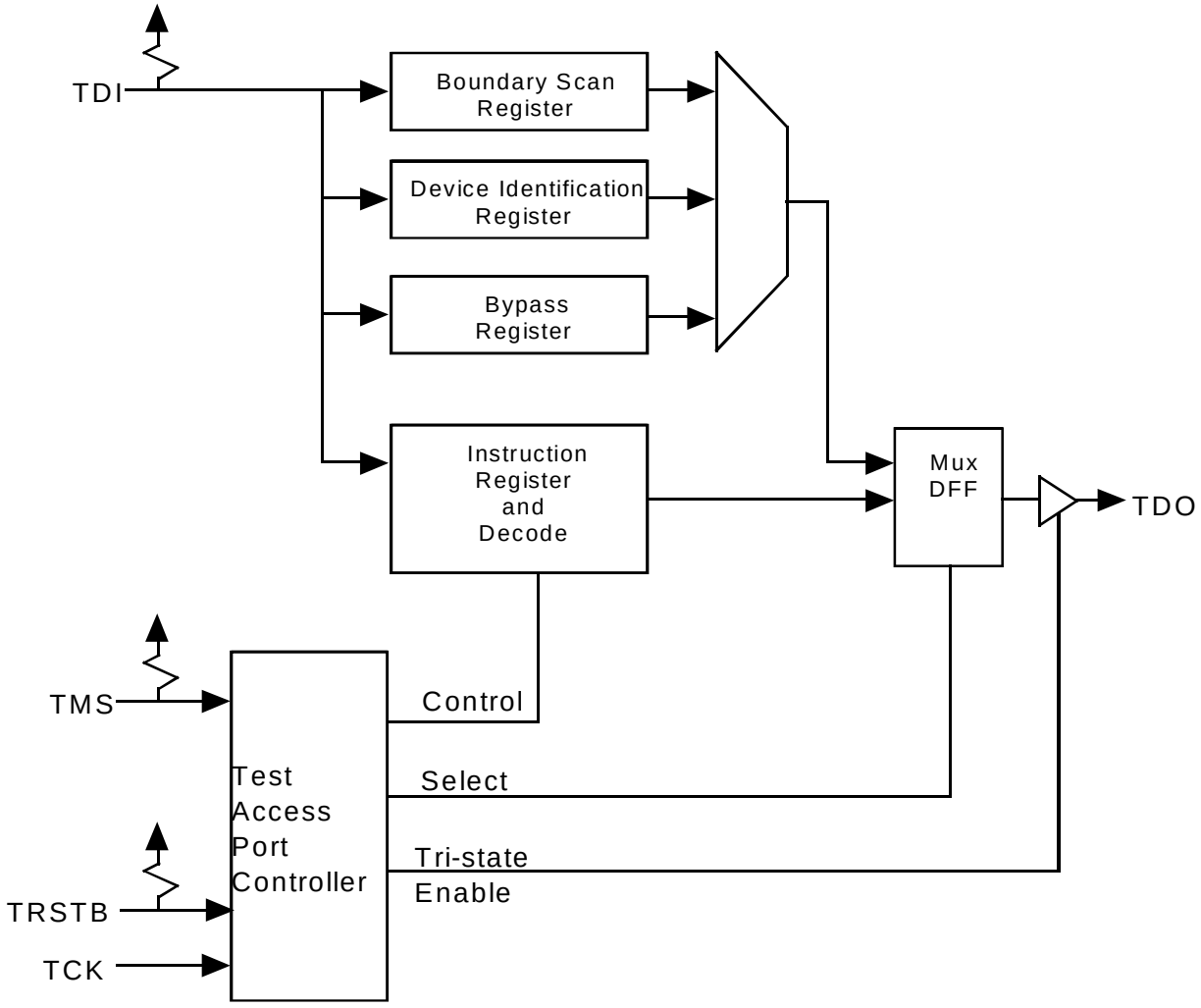
Notes for the Pseudo Random and Repetitive Pattern Generation Tables

1. The PS bit and the QRSS bit are contained in the TDPR Control register
2. TR = TDPR Tap Register
3. LR = TDPR Length Register
4. IR#1 = TDPR Pattern Insertion #1 Register
5. IR#2 = TDPR Pattern Insertion #2 Register
6. IR#3 = TDPR Pattern Insertion #3 Register
7. IR#4 = TDPR Pattern Insertion #4 Register
8. The TINV bit and the RINV bit are contained in the TDPR Control register

12.15 JTAG Support

The S/UNI-QJET supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown below.

Figure 27 - Boundary Scan Architecture



The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

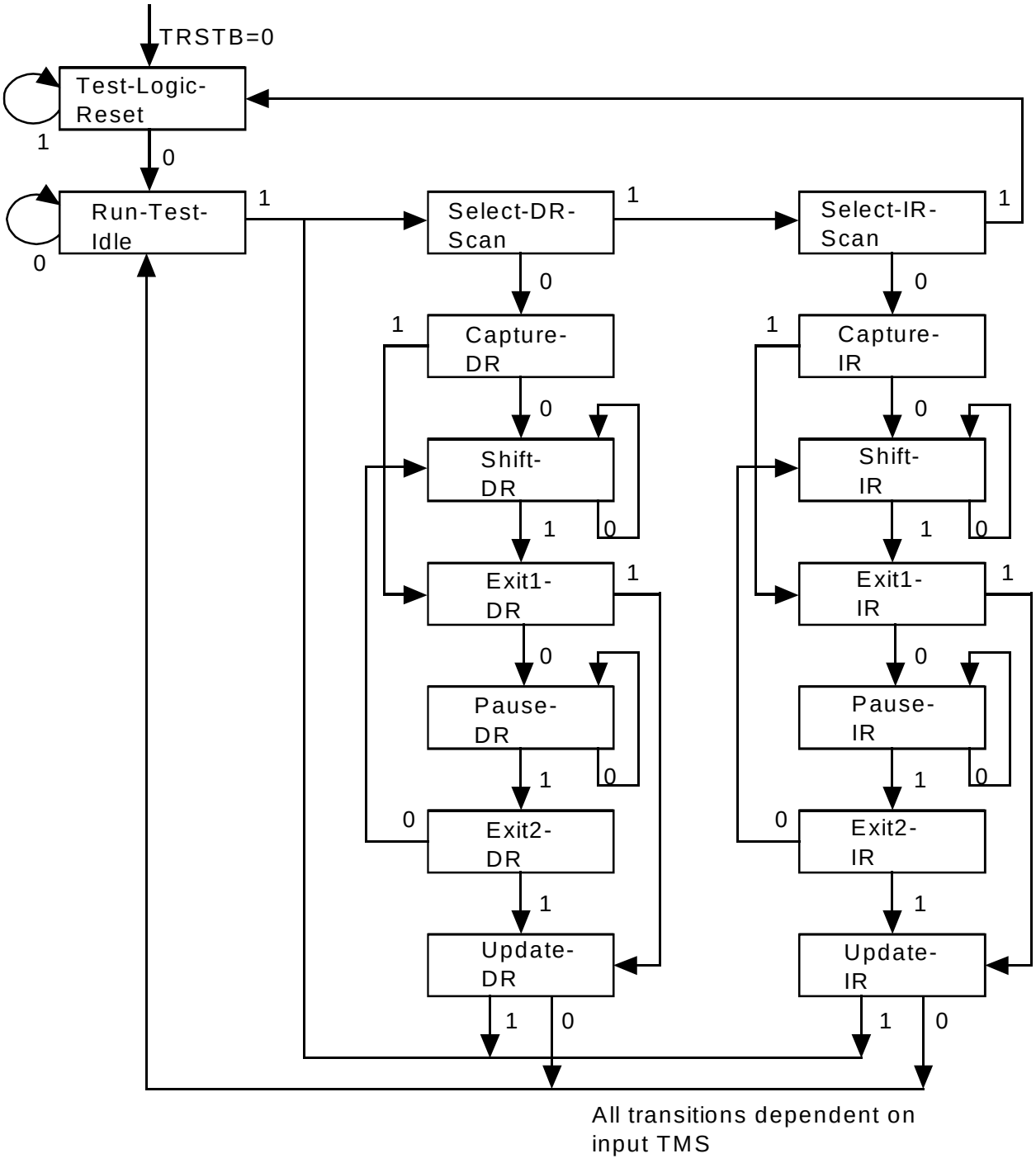
The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register place in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be

sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described below.

Figure 28 - TAP Controller Finite State Machine



Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

Boundary Scan Instructions

The following is an description of the standard instructions. Each instruction selects an serial test data register path between input, TDI and output, TDO.

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is place between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

Boundary Scan Cell Description

In the following diagrams, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the center of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the Boundary Scan Register table located in the TEST FEATURES DESCRIPTION - JTAG Test Port section.

Figure 29 - Input Observation Cell (IN_CELL)

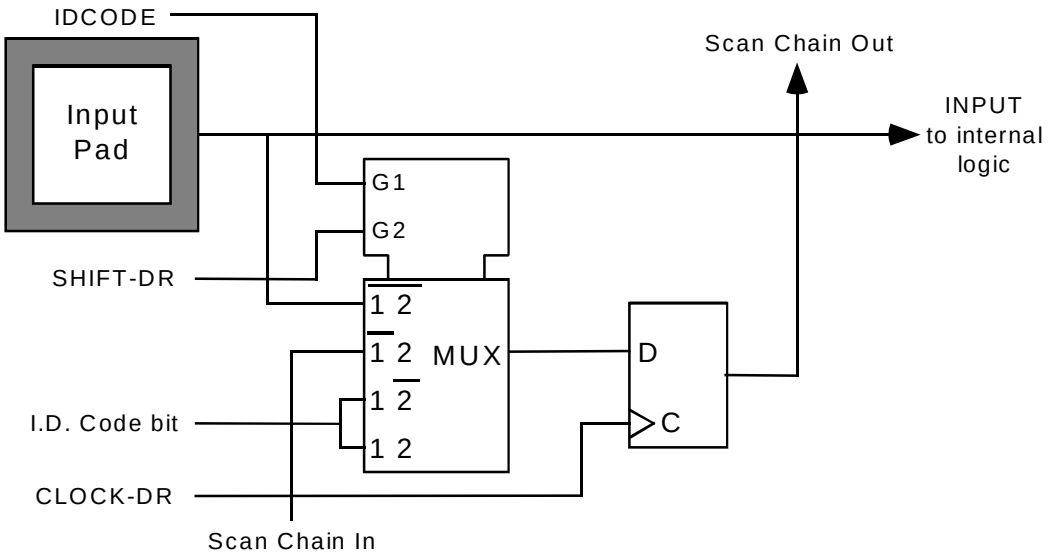


Figure 30 - Output Cell (OUT_CELL)

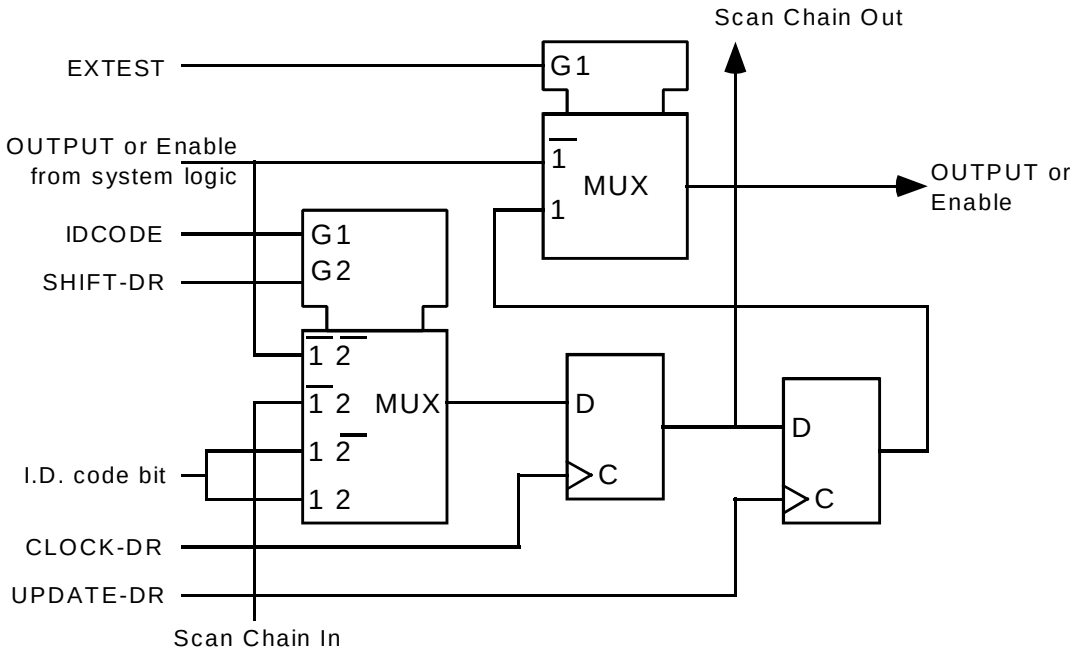


Figure 31 - Bi-directional Cell (IO_CELL)

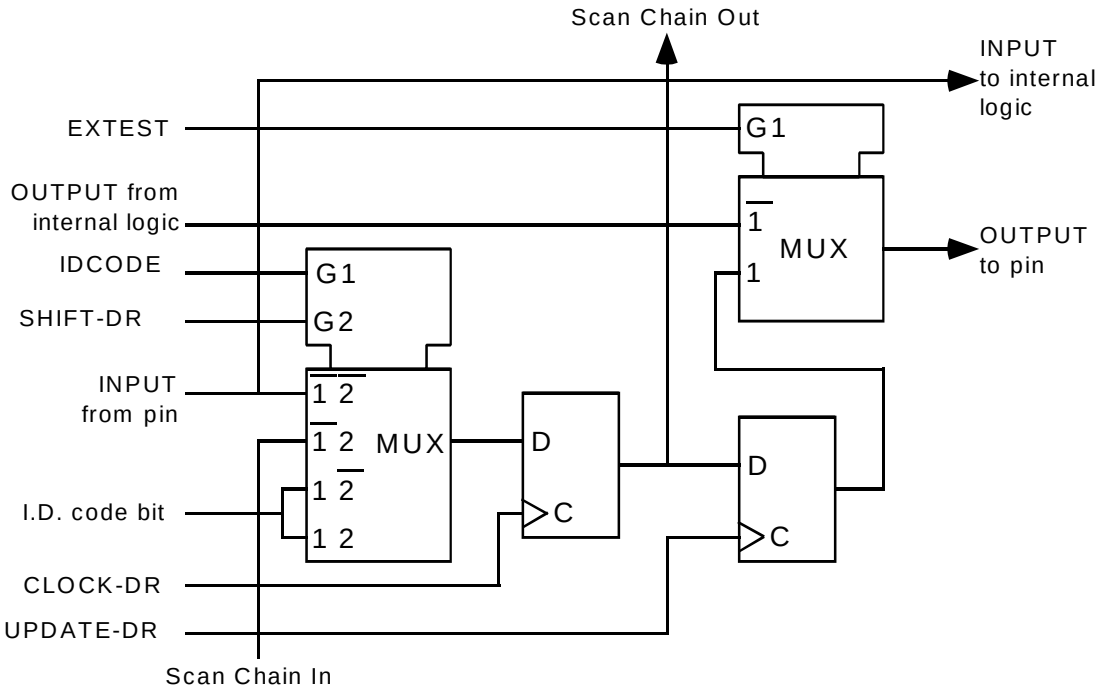
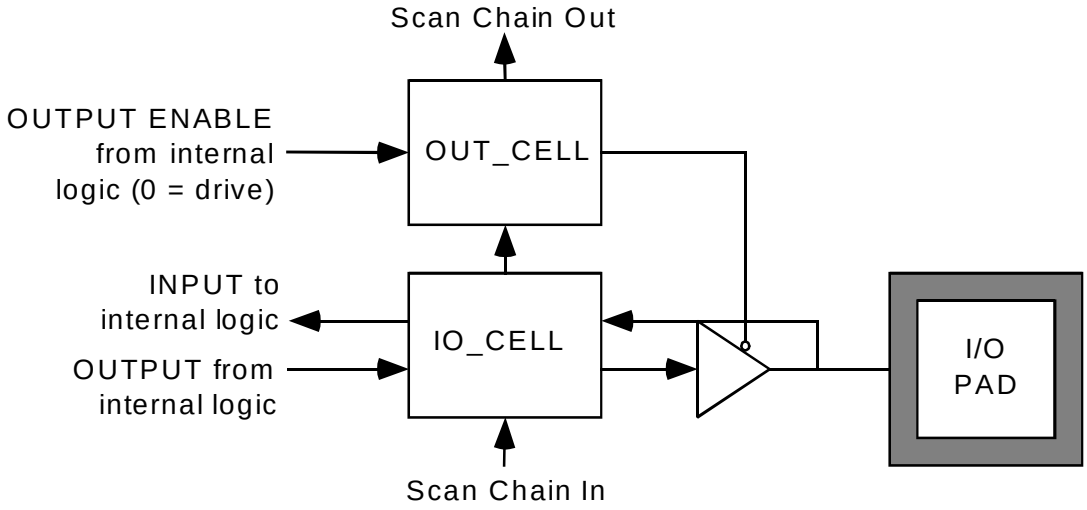


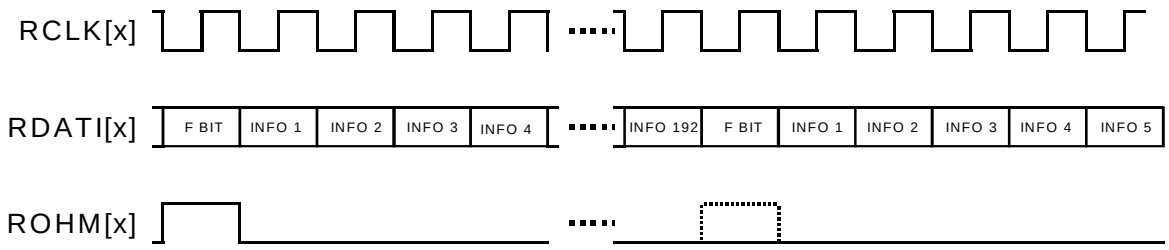
Figure 32 - Layout of Output Enable and Bi-directional Cells



13 FUNCTIONAL TIMING

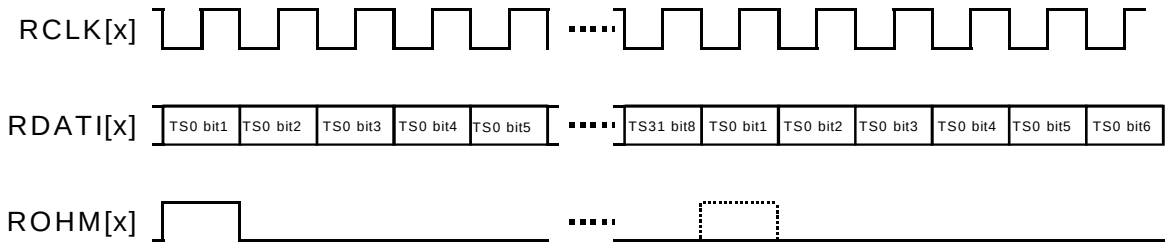
All functional timing diagrams assume that polarity control is not being applied to input and output data and clock lines (i.e. polarity control bits in the S/UNI-QJET registers are set to their default states).

Figure 33 - Receive DS1 Stream



The Receive DS1 Stream diagram (Figure 33) shows the expected DS1 overhead indicators on ROHM[x] when the S/UNI-QJET is configured for DS1 PLCP or DS1 direct-mapped frame formats. Frame pulses on ROHM[x] are not required to be present. Once internally synchronized by a pulse on ROHM[x], the S/UNI-QJET can use its internal timeslot counter for DS1 overhead bit identification. The ATM cell stream is contained in RDATI[x], along with a framing bit placeholder every 193 bit periods. An upstream DS1 framer (such as the PM4341A T1XC or PM4344 TQUAD) must be used to identify the DS1 framing bit position.

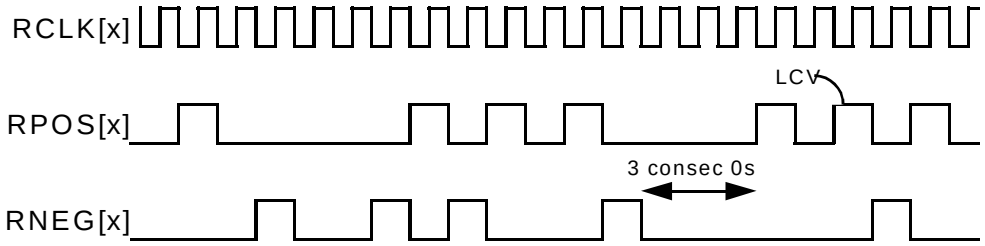
Figure 34 - Receive E1 Stream



The expected Receive E1 Stream for direct-mapped or PLCP applications is shown in Figure 34. Frame pulses on ROHM[x] are not required to be present every frame. Once internally synchronized by a pulse on ROHM[x], the S/UNI-QJET can use its internal timeslot counter for E1 overhead bit identification. The ATM cell stream is contained in RDATI[x], along with a framing bit placeholder every 256 bit periods. An upstream E1 framer (such as the

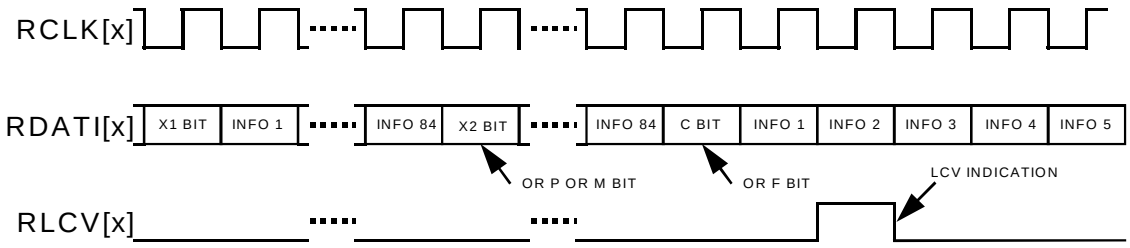
PM6341A E1XC or PM6344 EQUAD) must be used to identify the E1 framing bit position.

Figure 35 - Receive Bipolar DS3 Stream



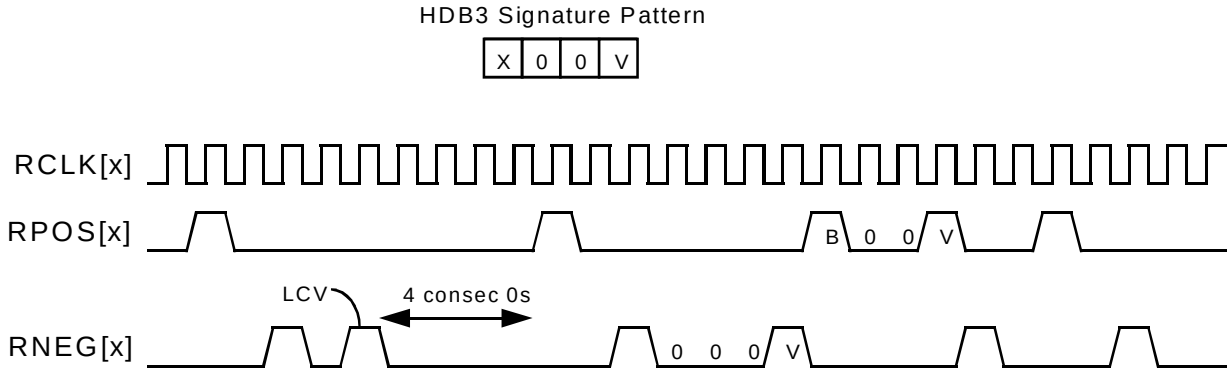
The Receive Bipolar DS3 Stream diagram (Figure 35) shows the operation of the S/UNI-QJET while processing a B3ZS encoded DS3 stream on inputs RPOS[x] and RNEG[x]. It is assumed that the first bipolar violation (on RNEG[x]) illustrated corresponds to a valid B3ZS signature. A line code violation is declared upon detection of three consecutive zeros in the incoming stream, or upon detection of a bipolar violation which is not part of a valid B3ZS signature.

Figure 36 - Receive Unipolar DS3 Stream



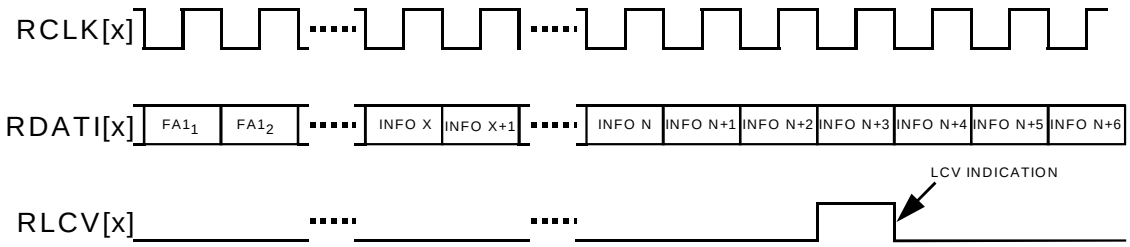
The Receive Unipolar DS3 Stream diagram (Figure 36) shows the complete DS3 receive signal on the RDATI[x] input. Line code violation indications, detected by an upstream B3ZS decoder, are indicated on input RLCV[x]. RLCV[x] is sampled each bit period. The PMON Line Code Violation Event Counter is incremented each time a logic 1 is sampled on RLCV[x].

Figure 37 - Receive Bipolar E3 Stream



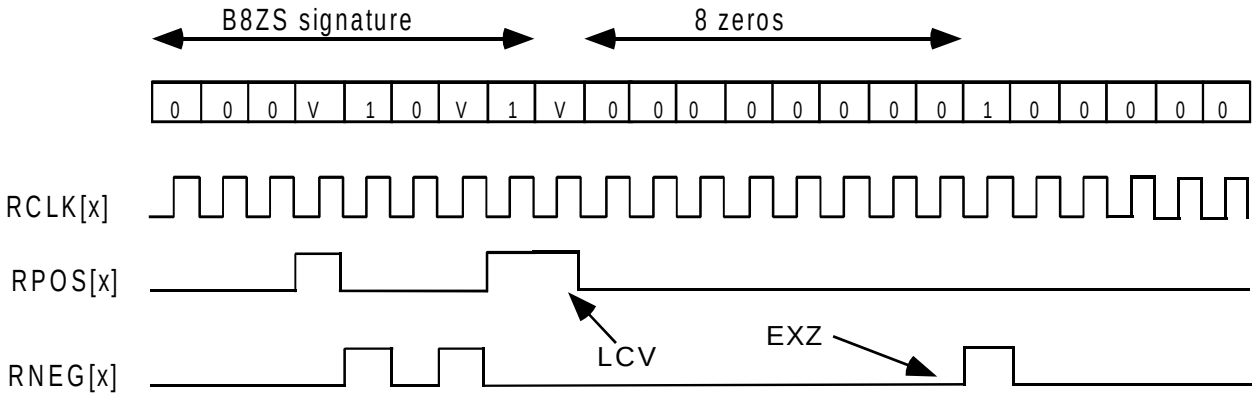
The Receive Bipolar E3 Stream diagram (Figure 37) shows the operation of the S/UNI-QJET while processing an HDB3-encoded E3 stream on inputs RPOS[x] and RNEG[x]. It is assumed that the first bipolar violation (on RNEG[x]) illustrated corresponds to a valid HDB3 signature. A line code violation is declared upon detection of four consecutive zeros in the incoming stream, or upon detection of a bipolar violation which is not part of a valid HDB3 signature.

Figure 38 - Receive Unipolar E3 Stream



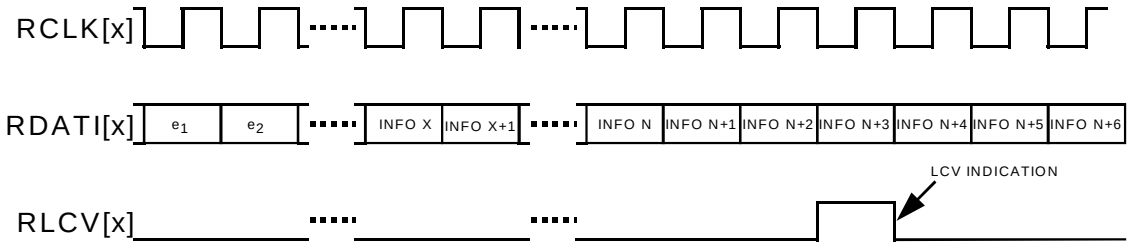
The Receive Unipolar E3 Stream diagram (Figure 38) shows the unipolar E3 receive signal on the RDATI[x] input. Line code violation indications, detected by an upstream HDB3 decoder, are indicated on input RLCV. RLCV is sampled each bit period. The PMON Line Code Violation Event Counter is incremented each time a logic 1 is sampled on RLCV.

Figure 39 - Receive Bipolar J2 Stream



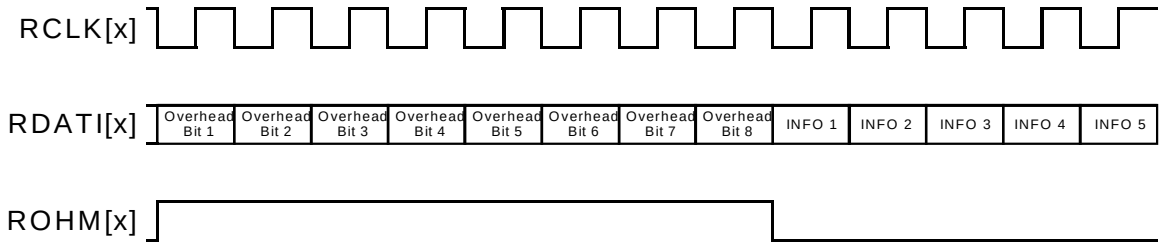
The Receive Bipolar J2 Stream diagram (Figure 39) shows the operation of the S/UNI-QJET while processing a B8ZS-encoded J2 stream on inputs RPOS and RNEG. It is assumed that the first bipolar violation (on RNEG) illustrated corresponds to a valid B8ZS signature. A line code violation is declared upon detection of a bipolar violation which is not part of a valid B8ZS signature. An excessive zeros indication is given when 8 or more consecutive zeros are detected.

Figure 40 - Receive Unipolar J2 Stream



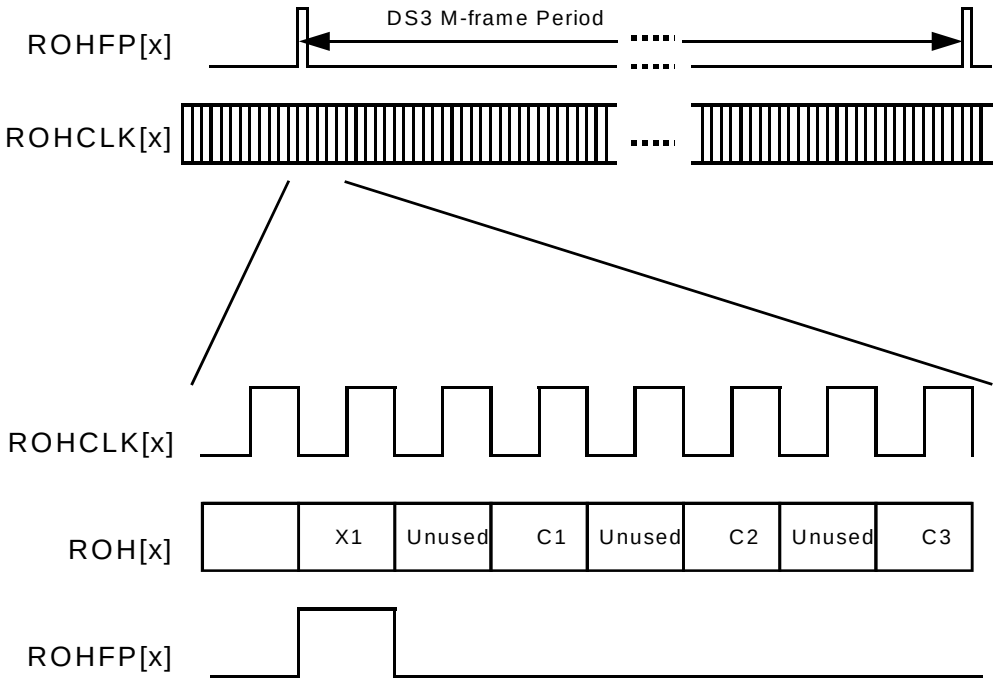
The Receive Unipolar J2 Stream diagram (Figure 40) shows the unipolar J2 receive signal on the RDATI[x] input. Line code violation indications, detected by an upstream B8ZS decoder, are indicated on input RLCV. RLCV is sampled each bit period. The PMON Line Code Violation Event Counter is incremented each time a logic 1 is sampled on RLCV.

Figure 41 - Generic Receive Stream



The generic receive stream diagram (Figure 41) illustrates how ROHM is used to mark the location of the transmission system overhead bits in the RDATI[x] stream. RDATI[x] and ROHM[x] are both sampled on the rising edge of RCLK[x].

Figure 42 - Receive DS3 Overhead



The Receive DS3 Overhead diagram (Figure 42) shows the extraction of the DS3 overhead bits on the ROH output, along with overhead clock (ROHCLK), and

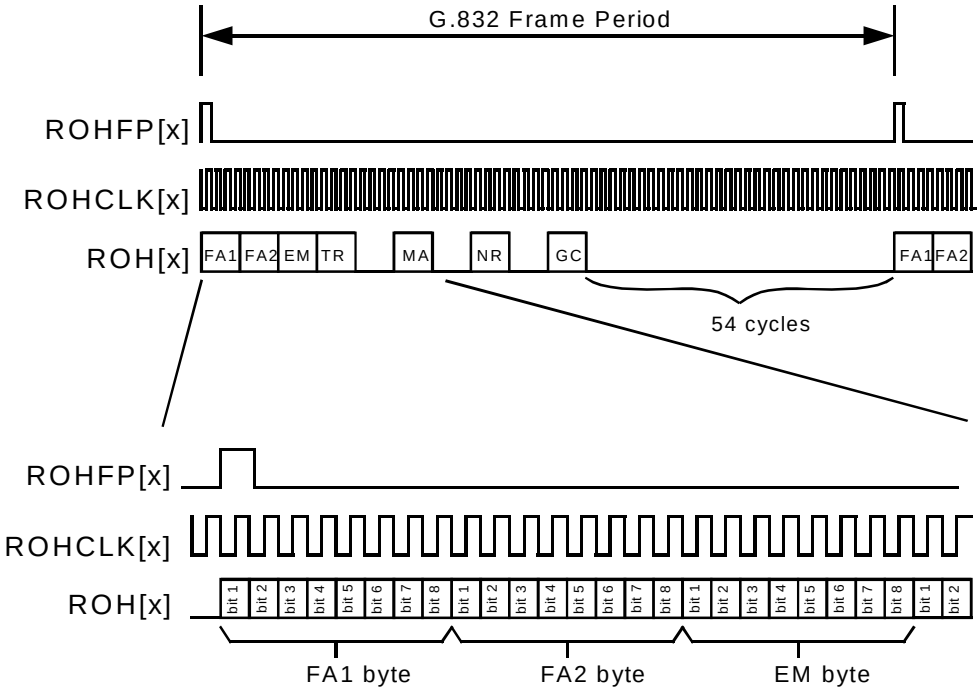
M-frame position indicator (ROHFP). The DS3 M-frame can be divided into seven M-subframes, with each subframe containing eight overhead bits. The table below illustrates the overhead bit order on ROH:

Table 39 - DS3 Receive Overhead Bits

M-subframe	DS3 Overhead Bits							
	1	2	3	4	5	6	7	8
1	X_1	N/U	C_1	N/U	C_2	N/U	C_3	N/U
2	X_2	N/U	C_1	N/U	C_2	N/U	C_3	N/U
3	P_1	N/U	C_1	N/U	C_2	N/U	C_3	N/U
4	P_2	N/U	C_1	N/U	C_2	N/U	C_3	N/U
5	M_1	N/U	C_1	N/U	C_2	N/U	C_3	N/U
6	M_2	N/U	C_1	N/U	C_2	N/U	C_3	N/U
7	M_3	N/U	C_1	N/U	C_2	N/U	C_3	N/U

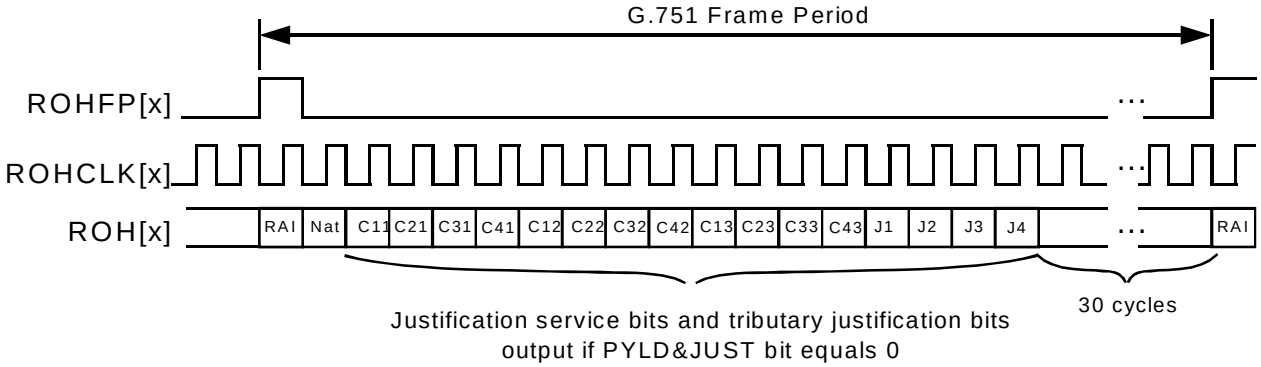
The DS3 framing bits (F-bits) are not extracted on the overhead port. The bit positions corresponding to the F-bits in the extracted stream are marked N/U in the above table. The ROH stream is invalid when the DS3 frame alignment is lost.

Figure 43 - Receive G.832 E3 Overhead



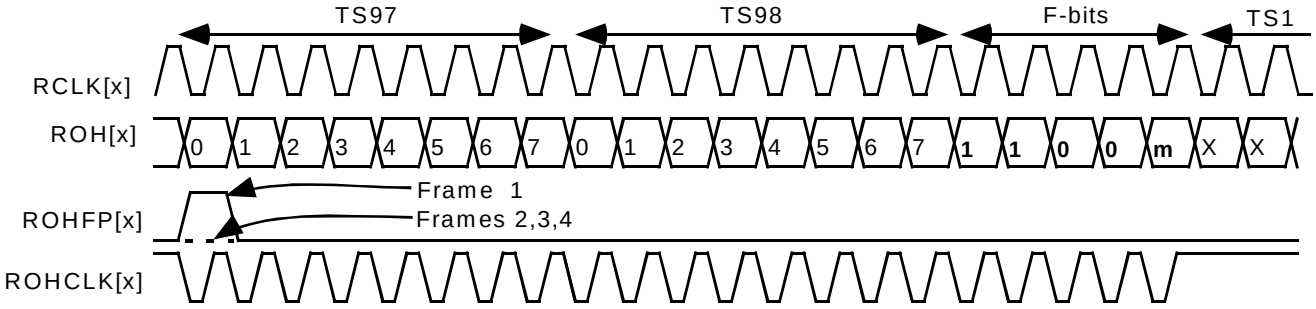
The Receive G.832 E3 Overhead diagram (Figure 43) shows the extraction of the G.832 E3 overhead bits on the ROH output, along with overhead clock (ROHCLK), and frame position indicator (ROHFP).

Figure 44 - Receive G.751 E3 Overhead



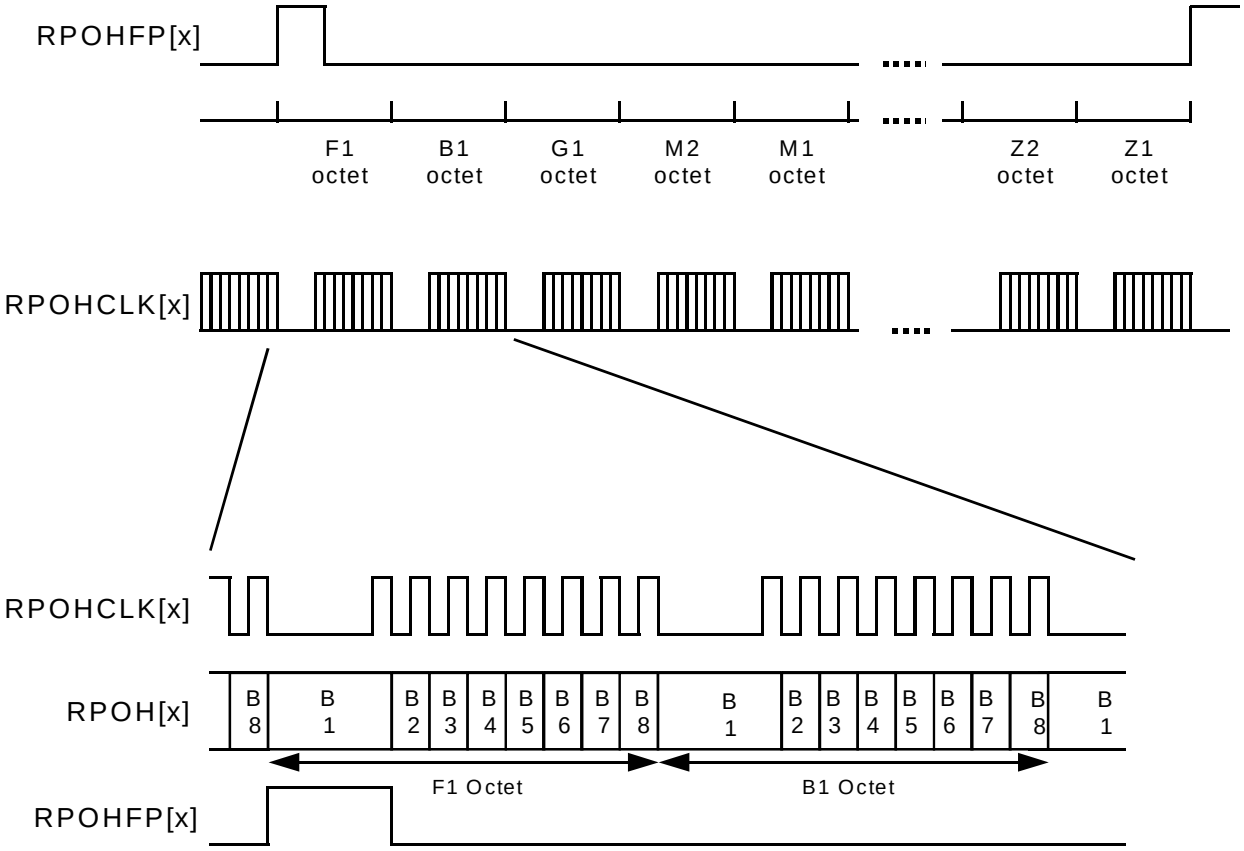
The Receive G.751 E3 Overhead diagram (Figure 44) shows the extraction of the G.751 E3 overhead bits on the ROH output, along with overhead clock (ROHCLK), and frame position indicator (ROHFP). The justification indication bits (C_{jk}) along with the justification opportunity bits (J_1-J_4) are extracted when they are treated as overhead (PYLD&JUST bit in the E3 FRMR Maintenance Options register set to logic 0).

Figure 45 - Receive J2 Overhead



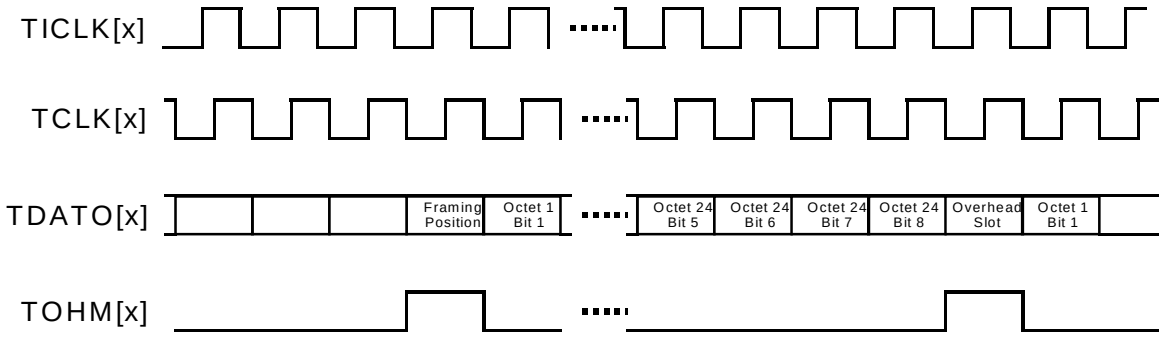
The Receive J2 Overhead diagram (Figure 45) shows the extraction of the J2 overhead bits on the ROH output, along with overhead clock (ROHCLK), and frame position indicator (ROHFP). ROHCLK is a gapped clock with a maximum instantaneous rate equal to the RCLK frequency. ROHFP pulses on the first bit of TS97 in the first frame of each J2 multiframe.

Figure 46 - Receive PLCP Overhead



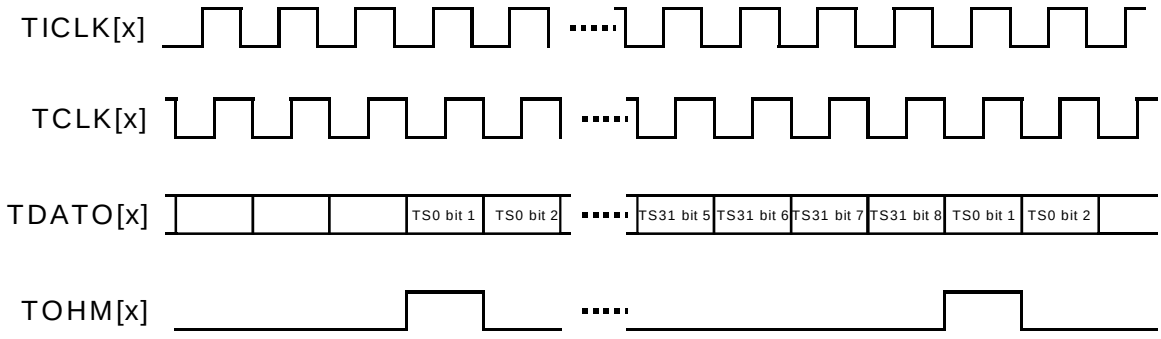
The Receive PLCP Overhead diagram (Figure 46) shows the extraction of the PLCP path overhead bits on the RPOH output, along with overhead clock (RPOHCLK), and PLCP frame position indicator (RPOHFP). The path overhead octets are shifted out in order with the most significant bit (bit 1) of each octet first. The number of growth octets (Zn) in the PLCP frame varies according to the selected PLCP frame format (DS3, DS1, G.751 E3, or E1). The PLCP frame position indicator (RPOHFP) is set high once per PLCP frame period, during bit 1 of the F1 octet, and indicates the 8 kHz receive PLCP frame timing.

Figure 47 - Transmit DS1 Stream



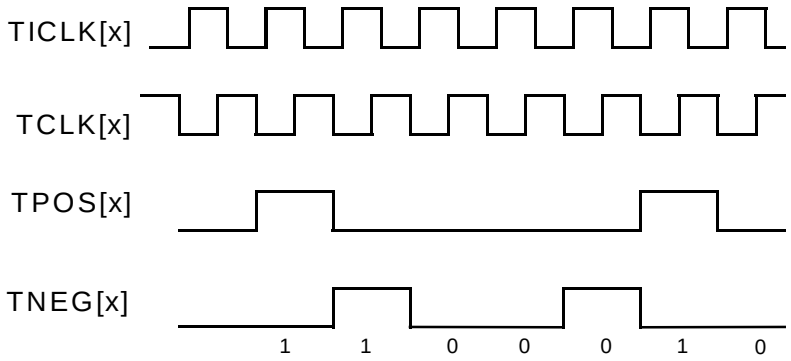
The Transmit DS1 Stream diagram (Figure 47) illustrates the generation of DS1 overhead indicators on TOHM when the S/UNI-QJET is configured for DS1 PLCP or non-PLCP frame formats. The S/UNI-QJET flywheels using its internal timeslot counter to generate TOHM. The ATM cell stream is inserted in TDATO, along with a framing bit placeholder every 193 bit periods. An upstream DS1 framer (such as the PM4341A T1XC or PM4344 TQUAD) must be used to insert the appropriate DS1 framing pattern. Note that TCLK is a flow through version of TICLK; a variable propagation delay exists between these two signals.

Figure 48 - Transmit E1 Stream



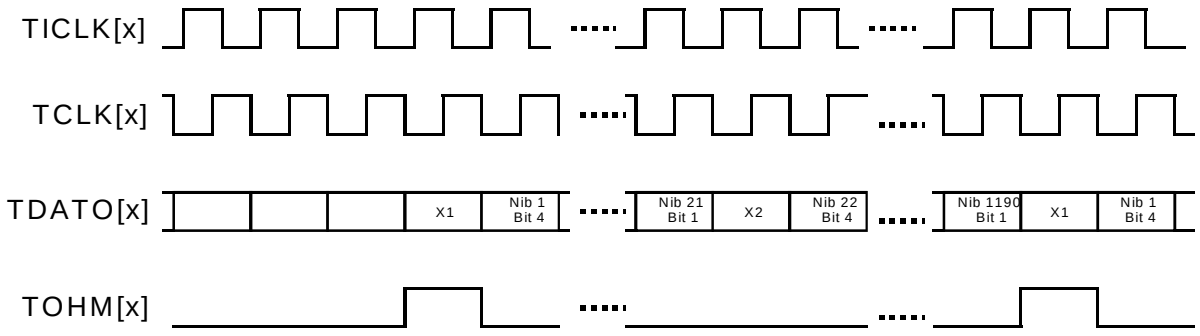
The Transmit E1 Stream diagram (Figure 48) illustrates the generation of E1 frame alignment indicators on TOHM when the S/UNI-QJET is configured for E1 PLCP or non-PLCP frame formats. The S/UNI-QJET flywheels using its internal timeslot counter to generate TOHM. The ATM cell stream is inserted in TDATO, along with a framing bit placeholder every 256 bit periods. An upstream E1 framer (such as the PM6341A E1XC or PM6344 EQUAD) must be used to insert the appropriate E1 framing pattern. Note that TCLK is a flow through version of TICLK; a variable propagation delay exists between these two signals.

Figure 49 - Transmit Bipolar DS3 Stream



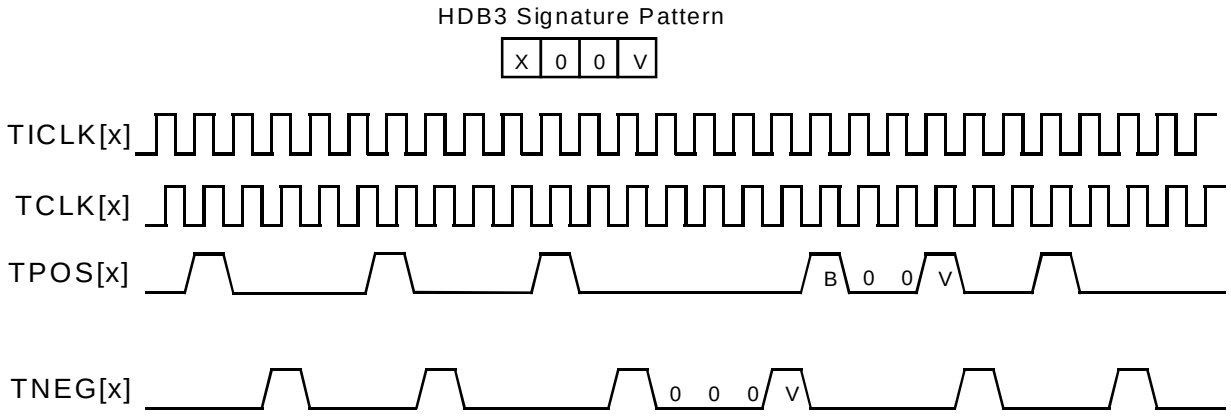
The Transmit Bipolar DS3 Stream diagram (Figure 49) illustrates the generation of a bipolar DS3 stream. The B3ZS encoded DS3 stream is present on TPOS and TNEG. These outputs, along with the transmit clock, TCLK, can be directly connected to a DS3 line interface unit. Note that TCLK is a flow through version of TICLK; a variable propagation delay exists between these two signals.

Figure 50 - Transmit Unipolar DS3 Stream



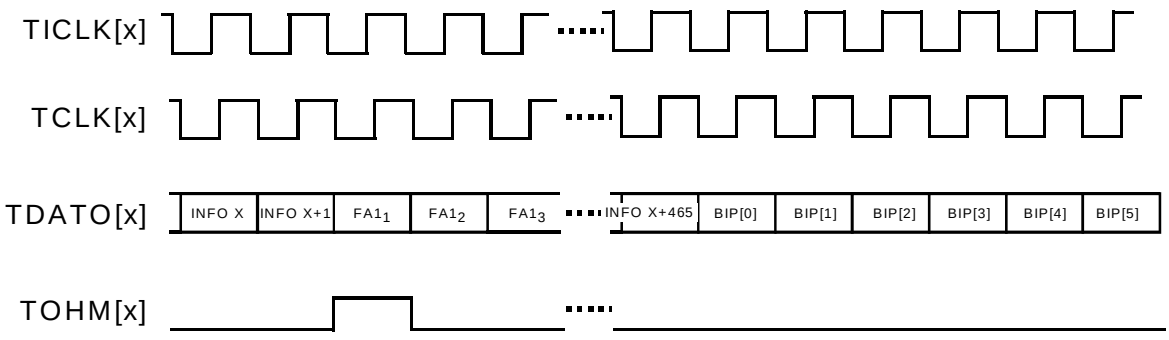
The Transmit Unipolar DS3 Stream diagram (Figure 50) illustrates the unipolar DS3 stream generation. The ATM cell stream, along with valid DS3 overhead bits is contained in TDATO. The TOHM output marks the M-frame boundary (the X1 bit) in the transmit stream. Note that TCLK is a flow through version of TICLK; a variable propagation delay exists between these two signals.

Figure 51 - Transmit Bipolar E3 Stream



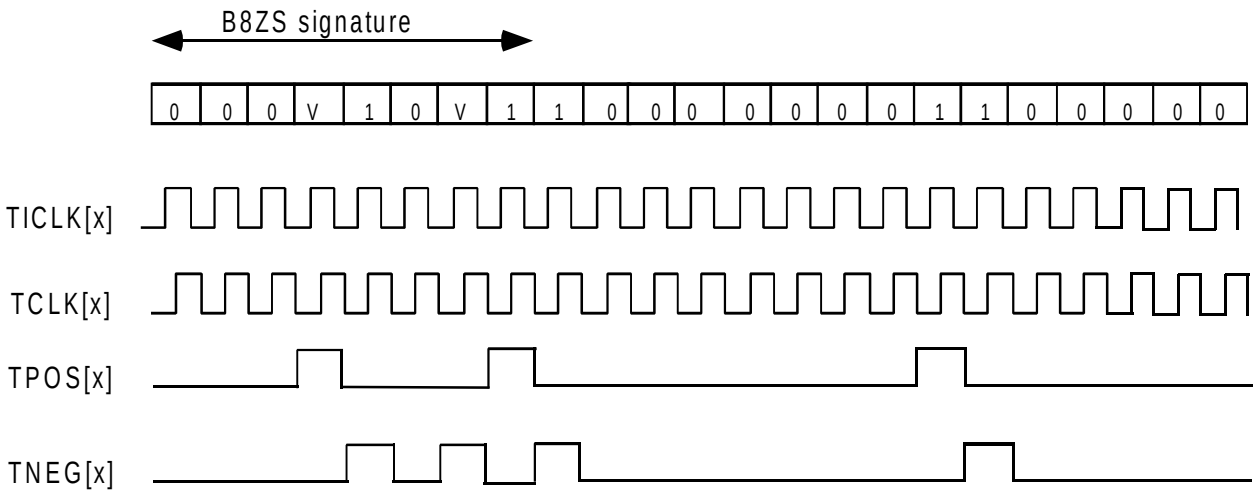
The Transmit Bipolar E3 Stream diagram (Figure 51) illustrates the generation of a bipolar E3 stream. The HDB3 encoded E3 stream is present on TPOS and TNEG. These outputs, along with the transmit clock, TCLK, can be directly connected to a E3 line interface unit. Note that TCLK is a flow through version of TICLK; a variable propagation delay exists between these two signals.

Figure 52 - Transmit Unipolar E3 Stream



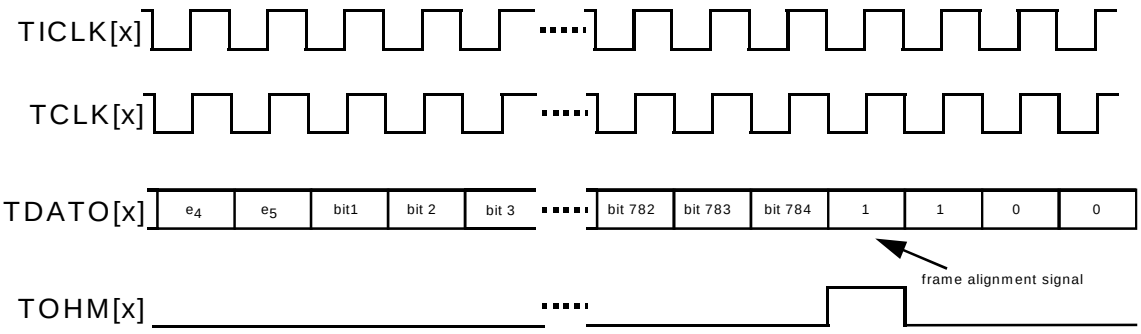
The Transmit Unipolar E3 Stream diagram (Figure 52) illustrates the unipolar E3 stream generation. The ATM cell stream, along with valid E3 overhead bits is contained in TDATO. The TOHM output shown marks the G.832 frame boundary (the first bit of the FA1 frame alignment byte) in the transmit stream. Note that TCLK is a flow through version of TICLK; a variable propagation delay exists between these two signals.

Figure 53 - Transmit Bipolar J2 Stream



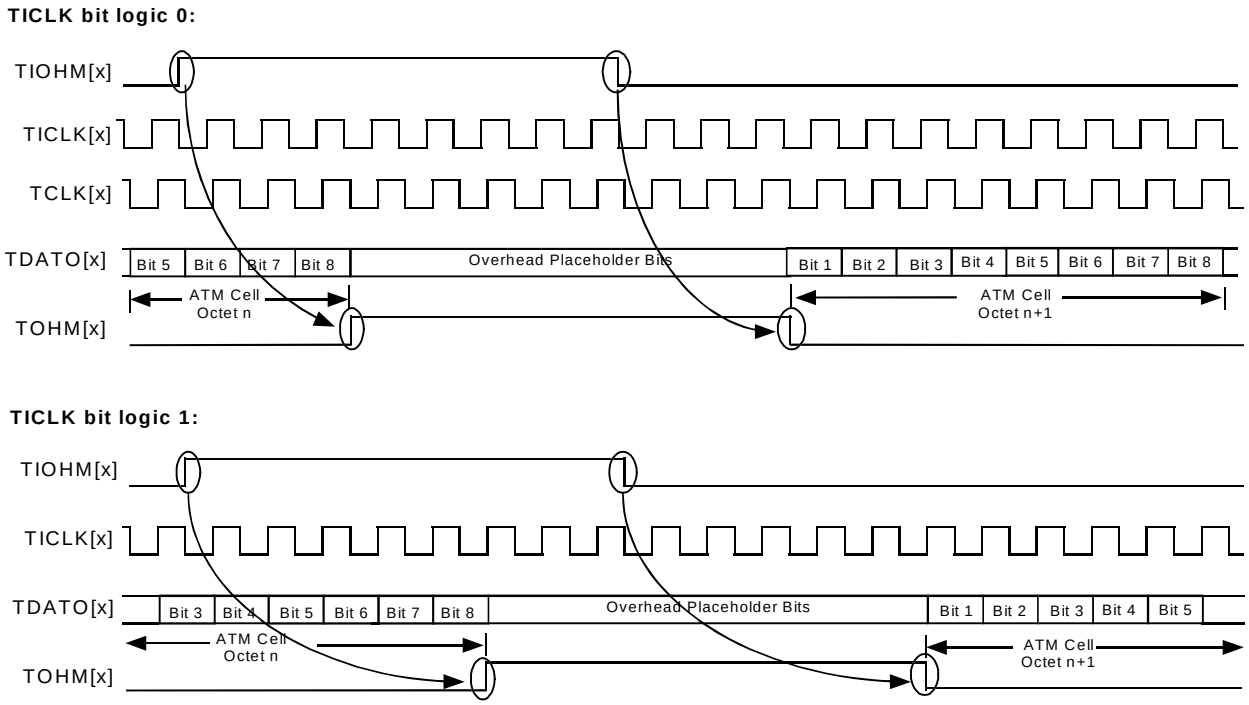
The Transmit Bipolar J2 Stream diagram (Figure 53) illustrates the generation of a bipolar J2 stream. The B8ZS encoded J2 stream is present on TPOS and TNEG. These outputs, along with the transmit clock, TCLK, can be directly connected to a J2 line interface unit. Note that TCLK is a flow through version of TICLK; a variable propagation delay exists between these two signals.

Figure 54 - Transmit Unipolar J2 Stream



The Transmit Unipolar J2 Stream diagram (Figure 54) illustrates the unipolar J2 stream generation. The ATM cell stream, along with valid J2 overhead bits is contained in TDATO. The TOHM output shown marks the J2 multi-frame boundary (the first frame-alignment bit of each J2 multi-frame) in the transmit stream. Note that TCLK is a flow through version of TICLK; a variable propagation delay exists between these two signals.

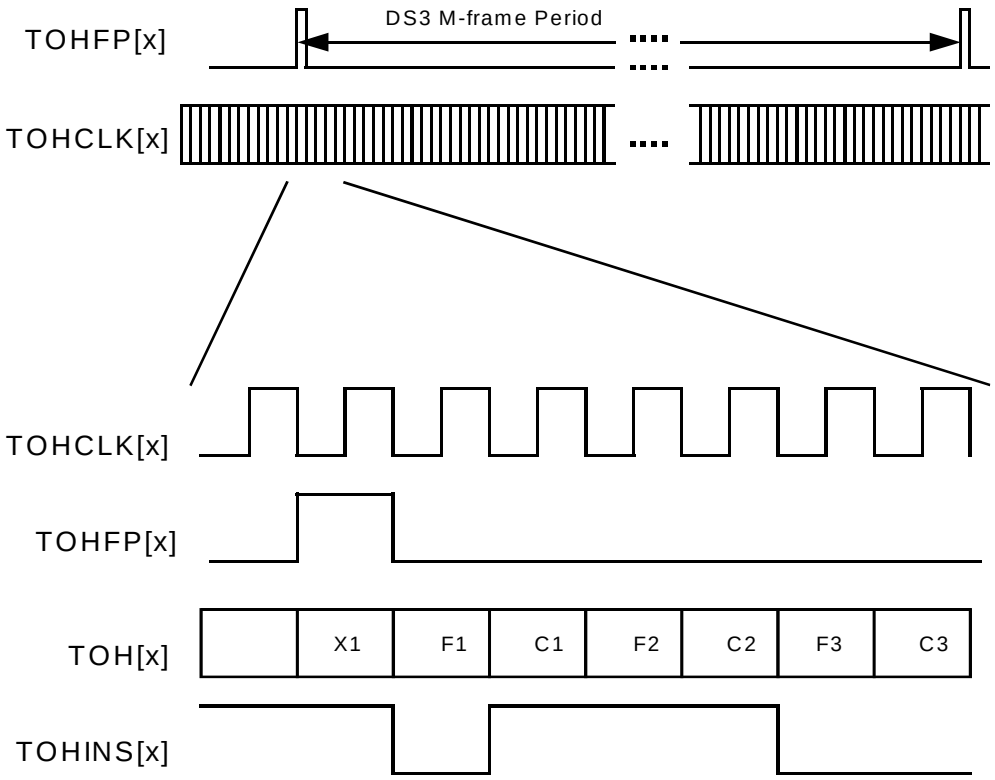
Figure 55 - Generic Transmit Stream



The Generic Transmit Stream diagram (Figure 55) illustrates overhead indication positions when interfacing to a non-PLCP based transmission system not supported by the SUNI-QJET. The overhead bit placeholder positions are indicated using the TIOHM input. The ATM cells presented in the TDATO transmit stream are held off to include the overhead placeholders. The location of these placeholder positions is indicated by TOHM. A downstream framer inserts the correct overhead information in the placeholder positions.

The delay between TIOHM and TOHM is dependent on the state of the TICLK bit of the S/UNI-QJET Transmit Configuration register. If the TICLK bit is a logic zero, TOHM is updated on the falling TCLK edge. TCLK is a flow-through version of TICLK and the propagation delay between TICLK and TCLK may vary depending on specific configurations. If the TICLK bit is a logic one, TOHM is presented on the fifth rising edge of TICLK after the rising edge which samples TIOHM.

Figure 56 - Transmit DS3 Overhead



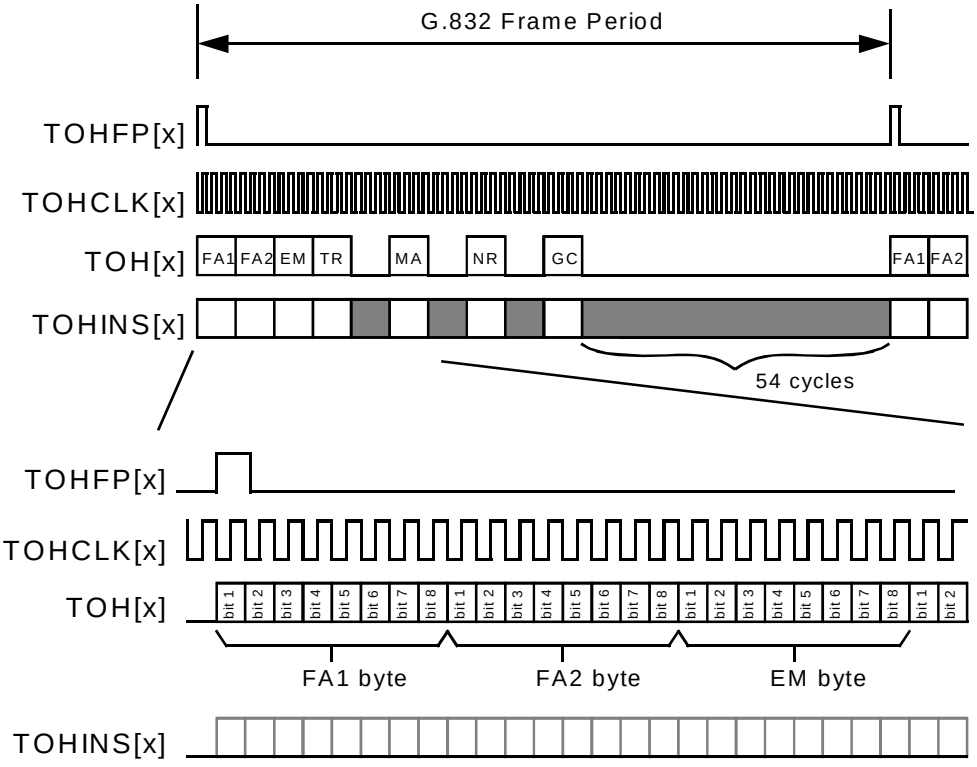
The Transmit DS3 Overhead diagram (Figure 56) shows the insertion of DS3 overhead bits using the TOH input, along with the overhead insertion enable input, TOHINS. The TOHFP output is set to logic 1 once per DS3 M-frame period (during the X1 bit position). In Figure 56, the data sampled on TOH during the X1, C1, F2, and C2 bit positions is inserted into the DS3 overhead bits in the transmit stream. The F1, F3, and C3 overhead bits are internally generated by the S/UNI-QJET. The table below illustrates the overhead bit order on TOH:

Table 40 - DS3 Transmit Overhead Bits

M-subframe	DS3 Overhead Bits							
	1	2	3	4	5	6	7	8
1	X_1	F_1	C_1	F_2	C_2	F_3	C_3	F_4
2	X_2	F_1	C_1	F_2	C_2	F_3	C_3	F_4
3	P_1	F_1	C_1	F_2	C_2	F_3	C_3	F_4

M-subframe	DS3 Overhead Bits							
	1	2	3	4	5	6	7	8
4	P_2	F_1	C_1	F_2	C_2	F_3	C_3	F_4
5	M_1	F_1	C_1	F_2	C_2	F_3	C_3	F_4
6	M_2	F_1	C_1	F_2	C_2	F_3	C_3	F_4
7	M_3	F_1	C_1	F_2	C_2	F_3	C_3	F_4

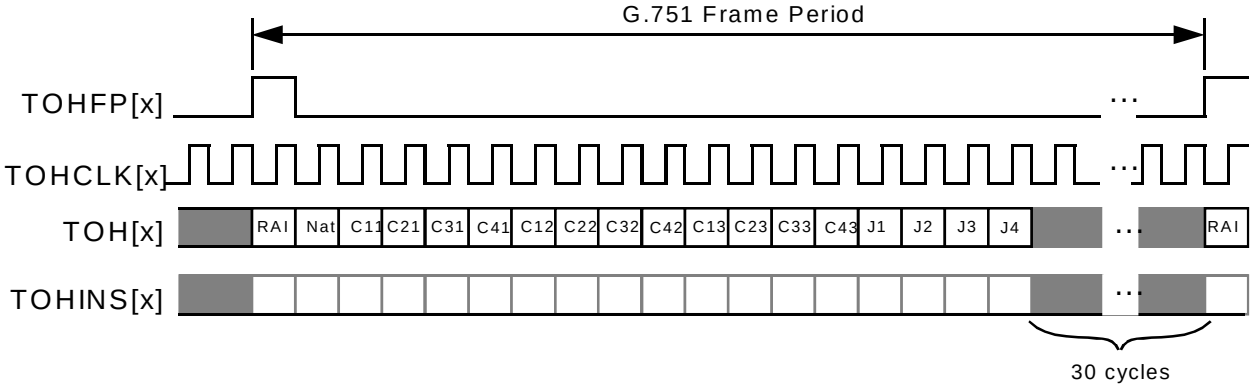
Figure 57 - Transmit G.832 E3 Overhead



The Transmit G.832 E3 Overhead diagram (Figure 57) shows the insertion of G.832 E3 overhead bits using the TOH input, along with the overhead insertion enable input, TOHINS. The TOHFP output is set to logic 1 once per G.832 frame period (during the first bit position of the FA1 byte). In Figure 57, the bit data sampled on TOH during each byte position while TOHINS is logic 1 is inserted into the G.832 E3 overhead bits in the transmit stream. Note that if an entire byte is to be replaced with data from the TOH stream, TOHINS must be held logic 1 for the duration of that byte position. Also note that the EM byte behaves as an

error mask, that is the binary value sampled on TOH in the EM byte location is not inserted directly into the transmit overhead but, rather, the value is XORed with the calculated BIP-8 and inserted in the transmit overhead. Asserting TOHINS during the “gaps” in the TOH stream has no effect.

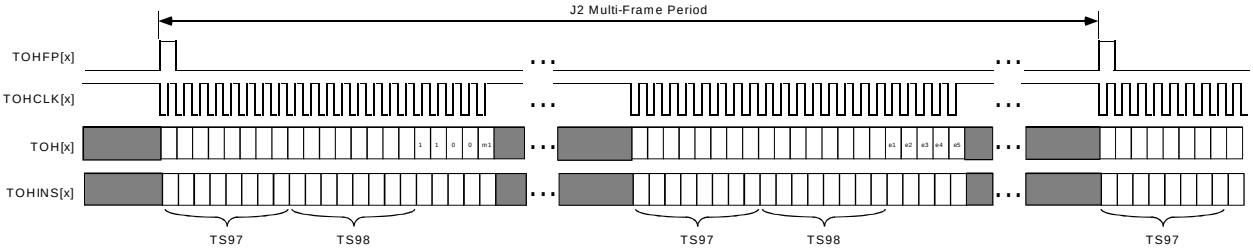
Figure 58 - Transmit G.751 E3 Overhead



The Transmit G.751 E3 Overhead diagram (Figure 58) shows the insertion of G.751 overhead bits RAI, the National Use Bit, and the stuff indication and opportunity bits using the TOH input, along with the overhead insertion enable input, TOHINS. The TOHFP output is set to logic 1 once per G.751 E3 frame period (during the RAI bit position). In Figure 58, the data sampled on TOH during the RAI, National Use, or stuff bit positions while TOHINS is logic 1 is inserted into the G.751 E3 overhead bits in the transmit stream.

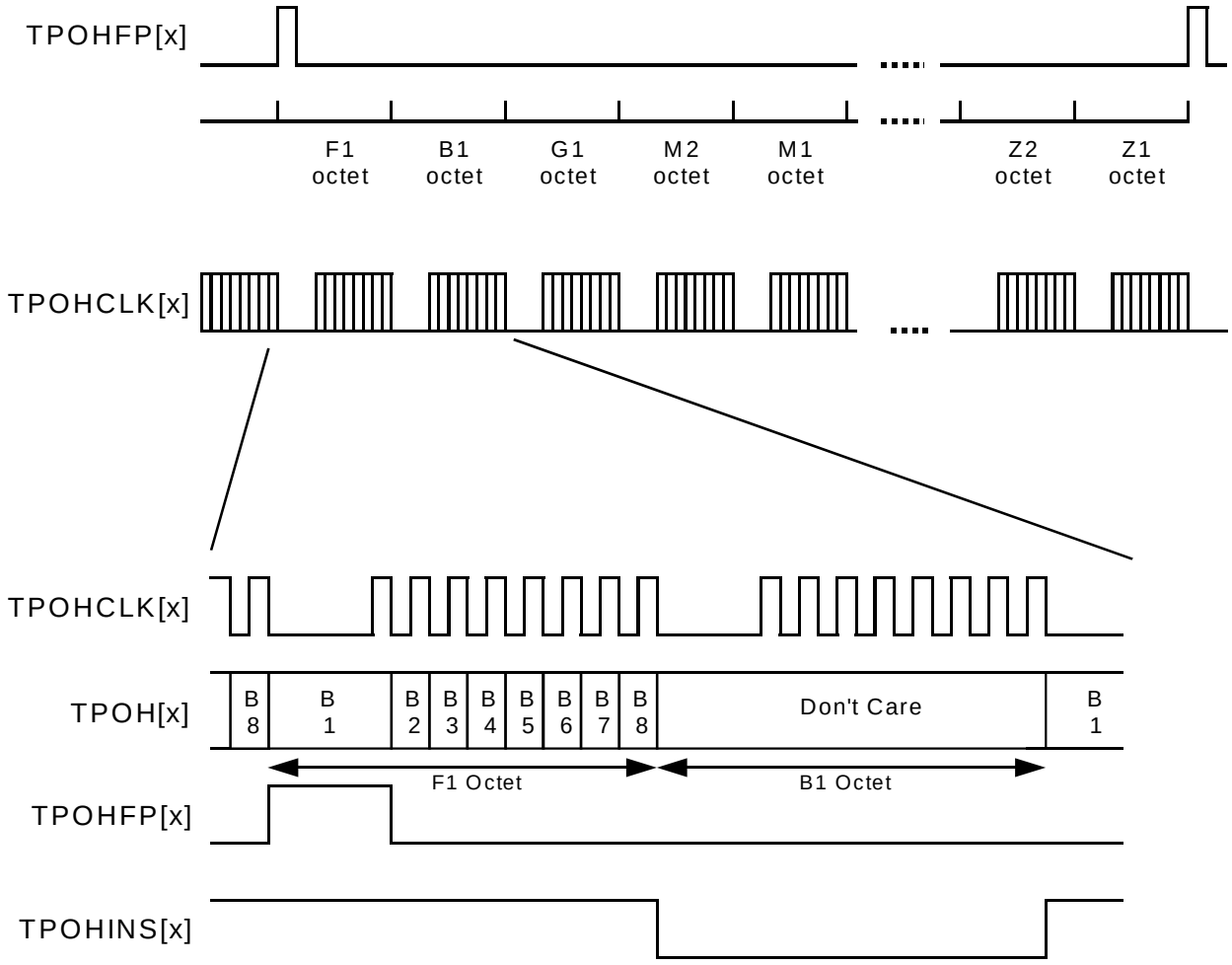
The PYLD&JUST bit in the E3 TRAN Status and Diagnostics Options register has no affect on the insertion of the justification service and the tributary justification bits through the TOH and the TOHINS inputs.

Figure 59 - Transmit J2 Overhead



The Transmit J2 Overhead diagram (Figure 59) shows the insertion of J2 overhead bits using the TOH and TOHINS inputs. The TOHFP output is set to logic 1 once per J2 multiframe (for the first bit of TS97 in the first frame of the J2 multiframe). TOHCLK is a gapped clock which will pulse at a maximum instantaneous rate equal to the TICLK frequency. When TOHINS is a logic 1, the TOH input pin state replaces that generated within the J2 TRAN block. TOH and TOHINS are sampled on the rising TOHCLK clock edge.

Figure 60 - Transmit PLCP Overhead



The Transmit PLCP Overhead diagram (Figure 60) shows the insertion of the PLCP path overhead bits using the TPOH input, along with overhead clock (TPOHCLK), and PLCP frame position indicator (TPOHFP). The path overhead octets are shifted in order with the most significant bit (bit 1) of each octet first. The number of growth octets (Zn) in the PLCP frame varies according to the

selected PLCP frame format (DS3, DS1, G.751 E3, or E1). The PLCP frame position indicator (TPOHFP) is set high once per PLCP frame period, during bit 1 of the F1 octet, and indicates the transmit PLCP frame timing. TPOH and TPOHINS are sampled using the rising edge of TPOHCLK. The bit presented on TPOH is only inserted into the path overhead if TPOHINS is asserted during the bit in question, or if the appropriate bit is set in the SPLT Control Register. The timing diagram above assumes that the SRCB1 bit in the SPLT Control Register is programmed to logic 0, thereby selecting internal insertion of that octet.

Figure 61 - Framer Mode DS3 Transmit Input Stream

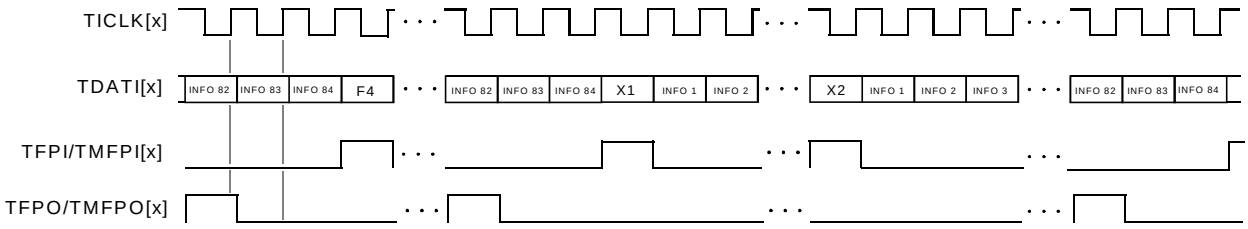
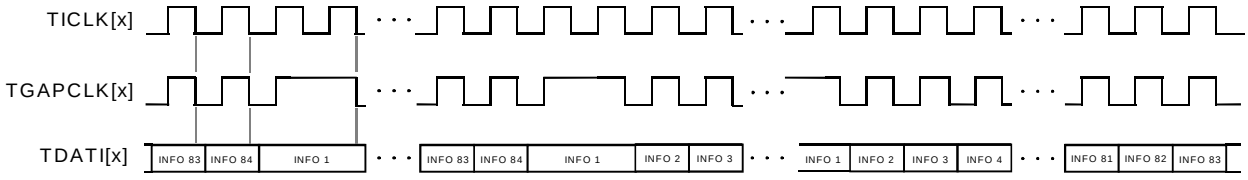


Figure 62 - Framer Mode DS3 Transmit Input Stream With TGAPCLK



The Framer Mode DS3 Transmit Input Stream diagrams (Figure 61 and Figure 62) show the expected format of the inputs TDATI and TFPI/TMFPI along with TICLK and the output TFPO/TMFPO when the FRMRONLY bit in the S/UNI-QJET Configuration 1 register is set, and the S/UNI-QJET is configured for the DS3 transmit format. If the TXMFPI register bit is logic 0, then TFPI is valid, and the S/UNI-QJET will expect TFPI to pulse for every DS3 overhead bit with alignment to TDATI. If the TXMFPI register bit is logic 1, then TMFPI is valid, and the S/UNI-QJET will expect TMFPI to pulse once every DS3 M-frame with alignment to TDATI. If the TXMFPO register bit is logic 0, then TFPO is valid, and the S/UNI-QJET will pulse TFPO once every 85 TICLK cycles, providing upstream equipment with a reference DS3 overhead pulse. If the TXMFPO register bit is logic 1, then TMFPO is valid and the S/UNI-QJET will pulse TMFPO once every 4760 TICLK cycles, providing upstream equipment with a reference M-frame pulse. The alignment of TFPO or TMFPO is arbitrary. There is no set relationship between TFPO/TMFPO and TFPI/TMFPI. The TGAPCLK output is available in place of TFPO/TMFPO when the TXGAPEN bit in the S/UNI-QJET

Configuration 2 register is set to logic 1, as in Figure 62. TGAPCLK remains high during the overhead bit positions. TDATI is sampled on the falling edge of TGAPCLK.

Figure 63 - Framer Mode DS3 Receive Output Stream

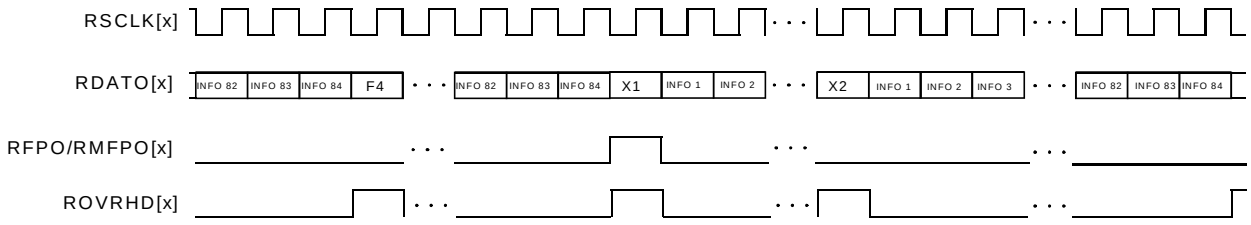
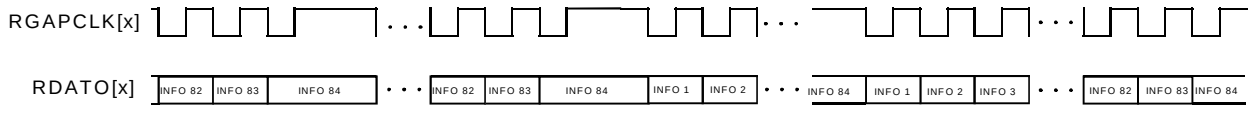


Figure 64 - Framer Mode DS3 Receive Output Stream with RGAPCLK



The Framer Mode DS3 Receive Output Stream diagrams (Figure 63 and Figure 64) show the format of the outputs RDATO, RFPO/RMFPO, RSCLK (and RGAPCLK), and ROVRHD when the FRMRONLY bit in the S/UNI-QJET Configuration 1 register is set. Figure 63 shows the data streams when the S/UNI-QJET is configured for the DS3 receive format. If the RXMFPO and 8KREFO register bits are logic 0, RFPO is valid and will pulse high for one RSCLK cycle on first bit of each M-subframe with alignment to the RDATO data stream. If the RXMFPO register bit is a logic 1 (as shown in Figure 63) and the 8KREFO register bit is logic 0, RMFPO is valid and will pulse high on the X1 bit of the RDATO data output stream. ROVRHD will be high for every overhead bit position on the RDATO data stream. As shown in Figure 64 the RGAPCLK output is available in place of RSCLK when the RXGAPEN bit in the S/UNI-QJET Configuration 2 register is set to logic 1. RGAPCLK remains high during the overhead bit positions and RDATO does not change.

Figure 65 - Framer Mode G.751 E3 Transmit Input Stream

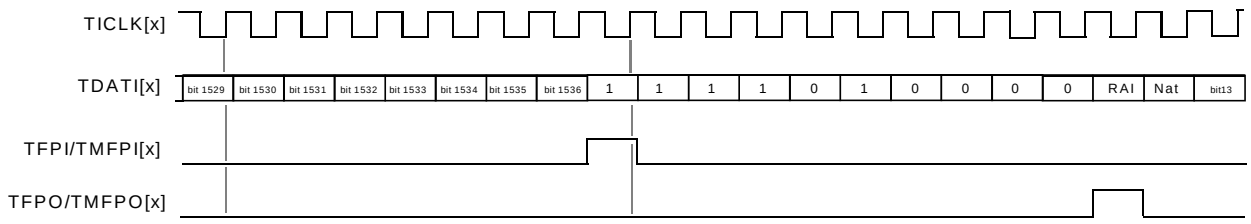
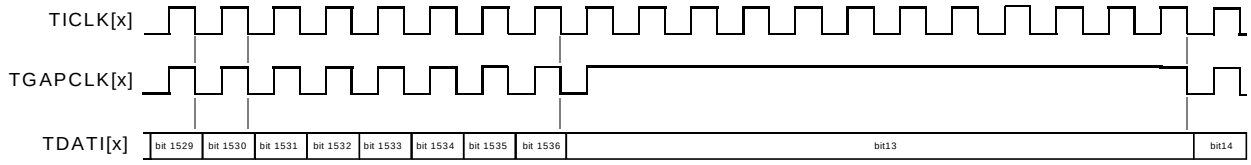


Figure 66 - Framer Mode G.751 E3 Transmit Input Stream With TGAPCLK



The Framer Mode G.751 E3 Transmit Input Stream diagrams (Figure 65 and Figure 66) show the expected format of the inputs TDATI, TFPI/TMFPI, and TICLK and the output TFPO/TMFPO (and TGAPCLK) when the FRMRONLY bit in the S/UNI-QJET Configuration 1 register is set, and the S/UNI-QJET is configured for the E3 G.751 transmit format. TFPI or TMFPI pulses high for one TICLK cycle and is aligned to the first bit of the frame alignment signal in the G.751 E3 input data stream on TDATI. TFPO or TMFPO will pulse high for one out of every 1536 TICLK cycles, providing upstream equipment with a reference frame pulse. The alignment of TFPO or TMFPO is arbitrary. There is no set relationship between TFPO/TMFPO and TFPI/TMFPI. The TGAPCLK output is available in place of TFPO/TMFPO when the TXGAPEN bit in the S/UNI-QJET Configuration 2 register is set to logic 1, as in Figure 66. TGAPCLK remains high during the overhead bit positions. TDATI is sampled on the falling edge of TGAPCLK.

Figure 67 - Framer Mode G.751 E3 Receive Output Stream

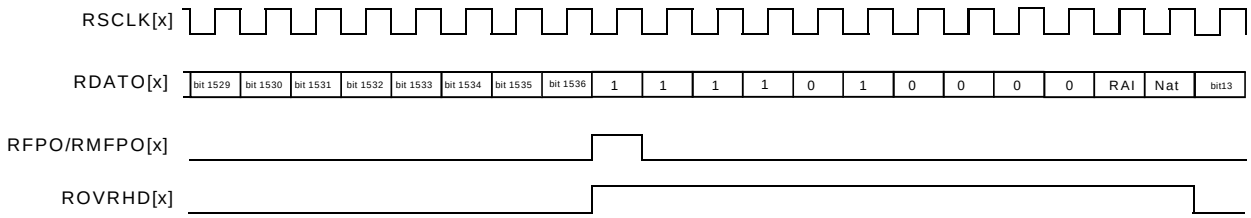
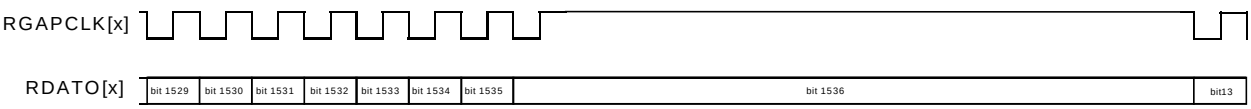


Figure 68 - Framer Mode G.751 E3 Receive Output Stream with RGAPCLK



The Framer Mode G.751 E3 Receive Output Stream diagrams (Figure 67 and Figure 68) show the format of the outputs RDATO, RFPO/RMFPO, RSCLK (and RGAPCLK), and ROVRHD when the FRMRONLY and the 8KREFO bits in the

S/UNI-QJET Configuration 1 register are set to logic 1 and logic 0 respectively. Figure 67 shows the data streams when the S/UNI-QJET is configured for the E3 G.751 receive format. RFPO or RMFPO pulses high for one RSCLK cycle and is aligned to the first bit of the framing alignment signal in the G.751 E3 output data stream on RDATO. ROVRHD will be high for every overhead bit position on the RDATO data stream. If the PYLD&JUST register bit in the E3 FRMR Maintenance Options register is set to logic 0, the C_{jk} and P_k bits in the RDATO stream will be marked as overhead bits. If the PYLD&JUST register bit is set to logic 1, the C_{jk} and P_k bits in the RDATO stream will be marked as payload. The RGAPCLK output is available in place of RSCLK when the RXGAPEN bit in the S/UNI-QJET Configuration 2 register is set to logic 1. RGAPCLK remains high during the overhead bit positions as shown in Figure 68.

Figure 69 - Framer Mode G.832 E3 Transmit Input Stream

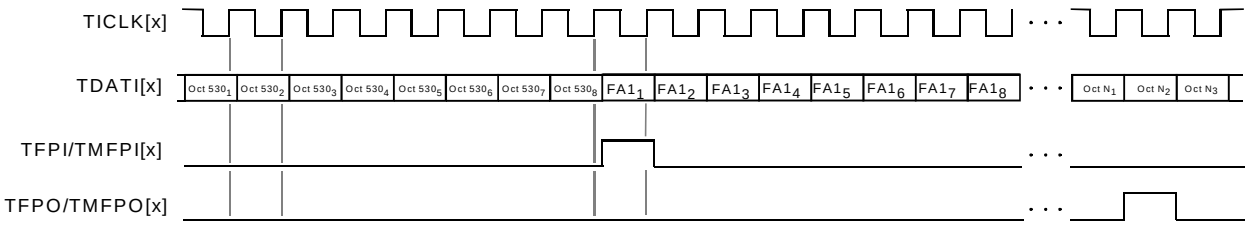
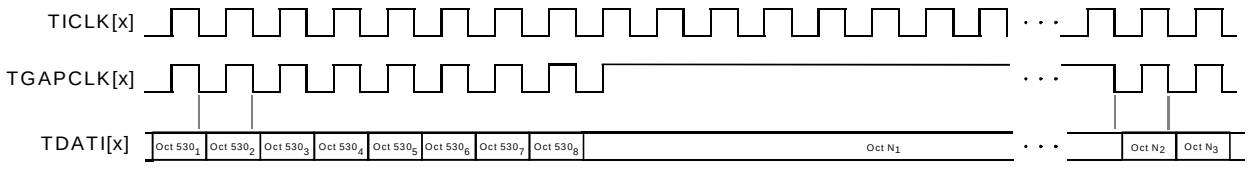


Figure 70 - Framer Mode G.832 E3 Transmit Input Stream With TGAPCLK



The Framer Mode G.832 E3 Transmit Input Stream diagrams (Figure 69 and Figure 70) show the expected format of the inputs TDATI, TFPI/TMFPI, and TICLK and the output TFPO/TMFPO (and TGAPCLK) when the FRMRONLY bit in the S/UNI-QJET Configuration 1 register is set, and the S/UNI-QJET is configured for the E3 G.832 transmit format. TFPI or TMFPI pulses high for one TICLK cycle and is aligned to the first bit of the FA1 byte in the G.832 E3 input data stream on TDATI. TFPO or TMFPO will pulse high for one out of every 4296 TICLK cycles, providing upstream equipment with a reference frame pulse. The alignment of TFPO or TMFPO is arbitrary. There is no set relationship between TFPO/TMFPO and TFPI/TMFPI. The TGAPCLK output is available in place of TFPO/TMFPO when the TXGAPEN bit in the S/UNI-QJET Configuration 2

register is set to logic 1, as in Figure 70. TGAPCLK remains high during the overhead bit positions. TDATI is sampled on the falling edge of TGAPCLK.

Figure 71 - Framer Mode G.832 E3 Receive Output Stream

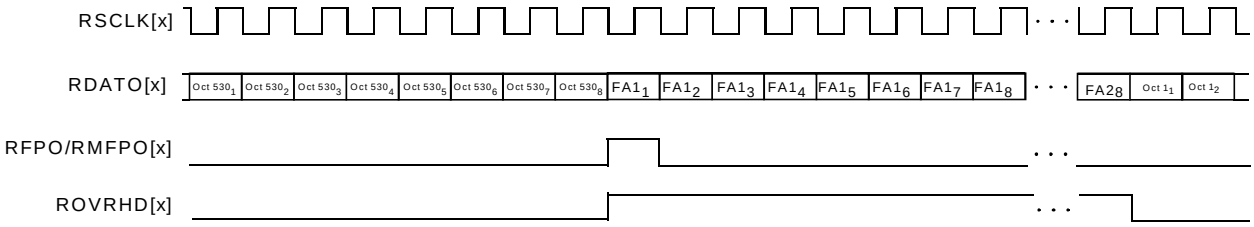
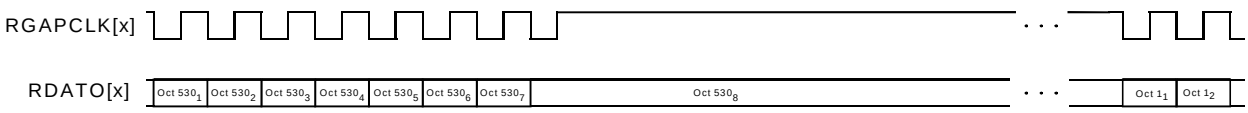


Figure 72 - Framer Mode G.832 E3 Receive Output Stream with RGAPCLK



The Framer Mode G.832 E3 Receive Output Stream diagrams (Figure 71 and Figure 72) show the format of the outputs RDATO, RFPO/RMFPO, RSCLK (and RGAPCLK), and ROVRHD when the FRMRONLY bit in the S/UNI-QJET Configuration 1 register is set. Figure 71 shows the data streams when the S/UNI-QJET is configured for the E3 G.832 receive format. RFPO or RMFPO pulses high for one RSCLK cycle and is aligned to the first bit of the FA1 byte in the G.832 E3 output data stream on RDATO. ROVRHD will be high for every overhead bit position on the RDATO data stream. The RGAPCLK output is available in place of RSCLK when the RXGAPEN bit in the S/UNI-QJET Configuration 2 register is set to logic 1. RGAPCLK remains high during the overhead bit positions as shown in Figure 72.

Figure 73 - Framer Mode J2 Transmit Input Stream

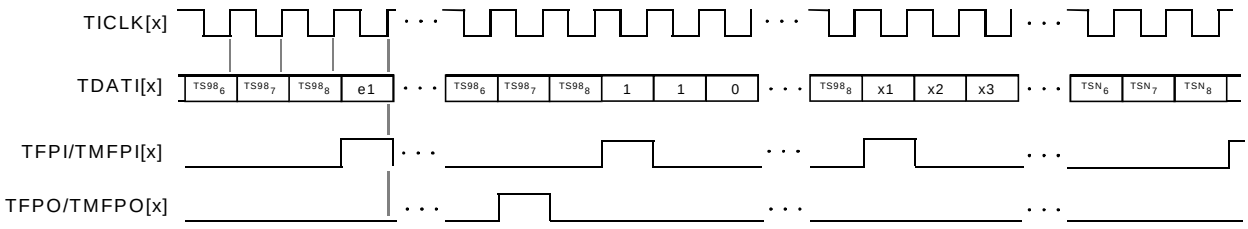
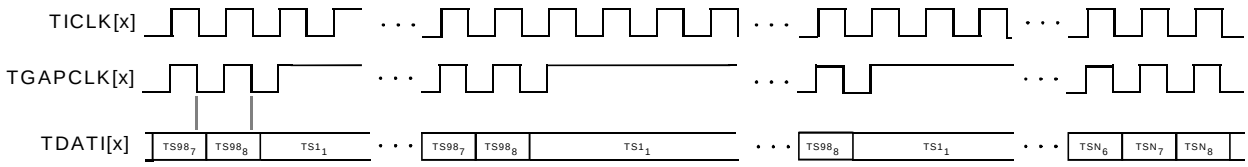


Figure 74 - Framer Mode J2 Transmit Input Stream With TGAPCLK



The Framer Mode J2 Transmit Input Stream diagrams (Figure 73 and Figure 74) show the expected format of the inputs TDATI, TFPI/TMFPI, and TICLK and the output TFPO/TMFPO (and TGAPCLK) when the FRMRONLY bit in the S/UNI-QJET Configuration 1 register is set, and the S/UNI-QJET is configured for the J2 transmit format. If the TXMFPI register bit is logic 0, then TFPI is valid (as shown in Figure 73). The S/UNI-QJET will expect TFPI to pulse once every J2 frame with alignment to the first frame alignment bit on TDATI. If the TXMFPI register bit is logic 1, then TMFPI is valid. The S/UNI-QJET will expect TMFPI to pulse once every J2 multi-frame with alignment to the first frame alignment bit on TDATI. If the TXMFPO register bit is logic 0, then TFPO is valid. The S/UNI-QJET will pulse TFPO once every 789 TICLK cycles, providing upstream equipment with a reference frame pulse. If the TXMFPO register bit is logic 1, then TMFPO is valid and the S/UNI-QJET will pulse TMFPO once every 3156 TICLK cycles, providing upstream equipment with a reference multi-frame pulse. The alignment of TFPO or TMFPO is arbitrary. There is no set relationship between TFPO/TMFPO and TFPI/TMFPI. The TGAPCLK output is available in place of TFPO/TMFPO when the TXGAPEN bit in the S/UNI-QJET Configuration 2 register is set to logic 1, as in Figure 74. TGAPCLK remains high during the overhead bit positions. TDATI is sampled on the falling edge of TGAPCLK.

Figure 75 - Framer Mode J2 Receive Output Stream

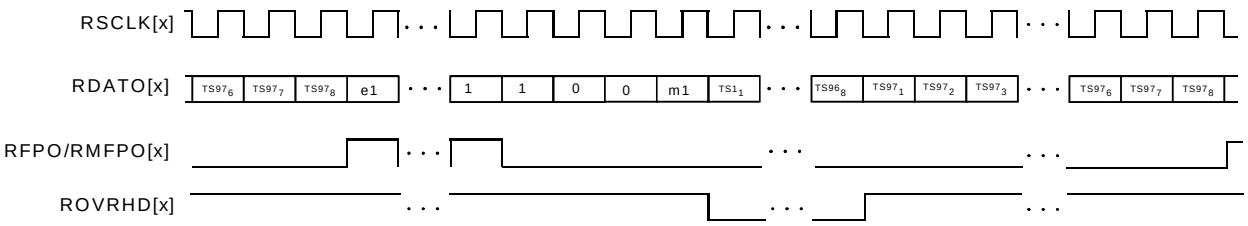
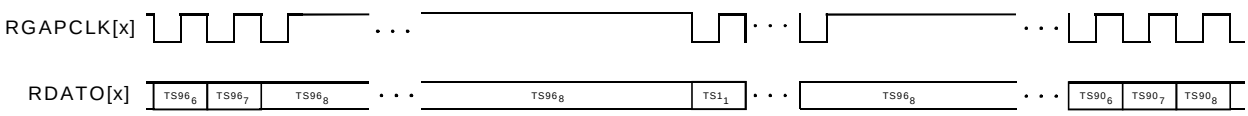


Figure 76 - Framer Mode J2 Receive Output Stream with RGAPCLK



The Framer Mode J2 Receive Output Stream diagrams (Figure 75 and Figure 76) show the format of the outputs RDATO, RFPO/RMFPO, RSCLK (and RGAPCLK), and ROVRHD when the FRMRONLY bit in the S/UNI-QJET Configuration 1 register is set. Figure 75 shows the data streams when the S/UNI-QJET is configured for the J2 receive format. If the RXMFPO register bit is a logic 0, RFPO is valid and will pulse high for one RSCLK cycle once each J2 frame with alignment to the first frame alignment bit on the RDATO data stream (as shown in Figure 75). If the RXMFPO register bit is a logic 1, RMFPO is valid and will pulse high once each J2 multi-frame aligned to the first frame alignment bit on the RDATO data output stream. ROVRHD will be high for every overhead bit position on the RDATO data stream. The RGAPCLK output is available in place of RSCLK when the RXGAPEN bit in the S/UNI-QJET Configuration 2 register is set to logic 1. RGAPCLK remains high during the overhead bit positions as shown in Figure 76.

Figure 77 - Multi-PHY Polling and Addressing Transmit Cell Interface

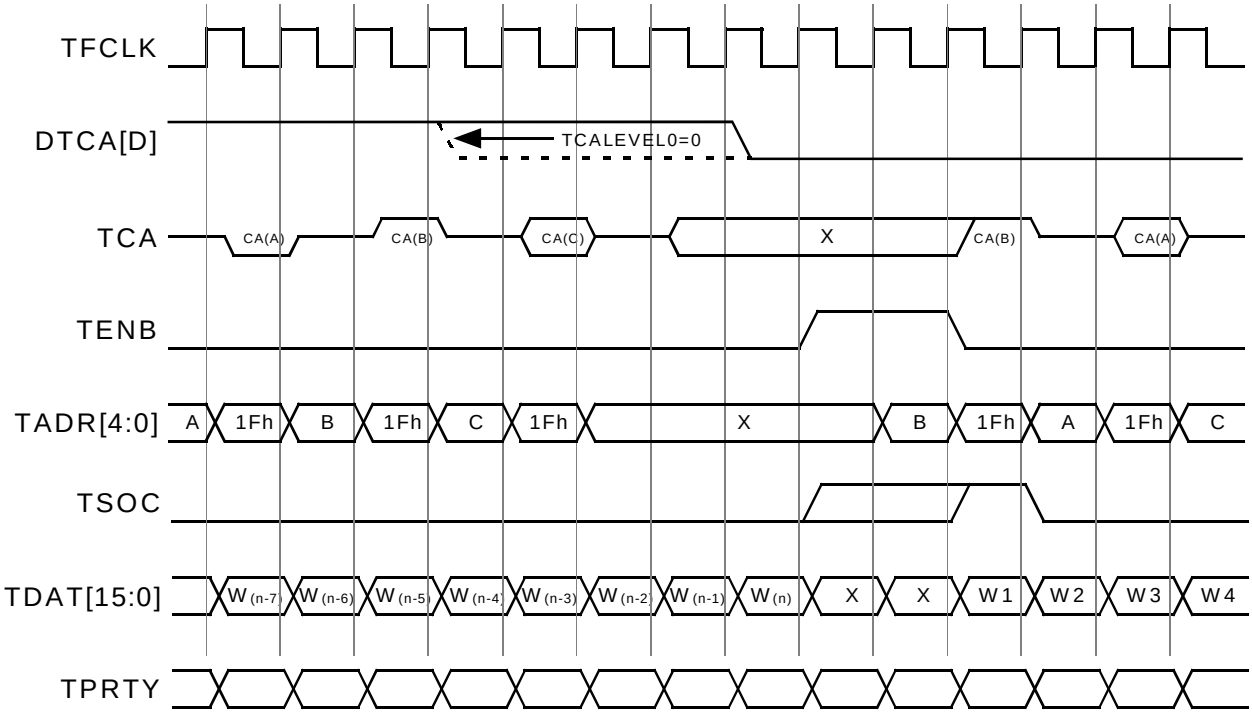


Figure 77 is an example of the multi-PHY polling and selection sequence supported by the S/UNI-QJET. "A", "B", "C", and “D” represent any arbitrary address values of PHY devices which may be occupied by the S/UNI-QJET. The ATM Layer device is not restricted in its polling order. Initially PHY “D” is accepting a cell and the direct TCA for that PHY is shown as DTCA[D]. The effect

of TCALEVEL0 is indicated with a dashed line in the figure. The PHY associated with address "A" indicates it cannot accept a cell, but PHY "B" indicates it is willing to accept a cell. As a result, the ATM Layer places address "B" on TADR[4:0] the cycle before TENB is asserted to select PHY "B" as the next cell destination. In this example, the PHY "C" status is ignored. The ATM Layer device is not constrained to select the latest PHY polled. As soon as the cell transfer is started, the polling process may be restarted. The data on TDAT (W1, W2, ...) may be 8-bit or 16-bits wide, depending on the setting of the ATM8 input.

During multi-PHY operation, several PHY layer devices share the TCA signal. As a result, this signals must be tri-stated in all PHY devices which have not been selected for polling by the ATM Layer. The value of TADR[4:0] selects the PHY being polled for the TCA signal, and all devices not corresponding to this address must tri-state its TCA output. This multi-PHY operation is directly supported by the S/UNI-QJET.

Figure 78 - Multi-PHY Polling and Addressing Receive Cell Interface

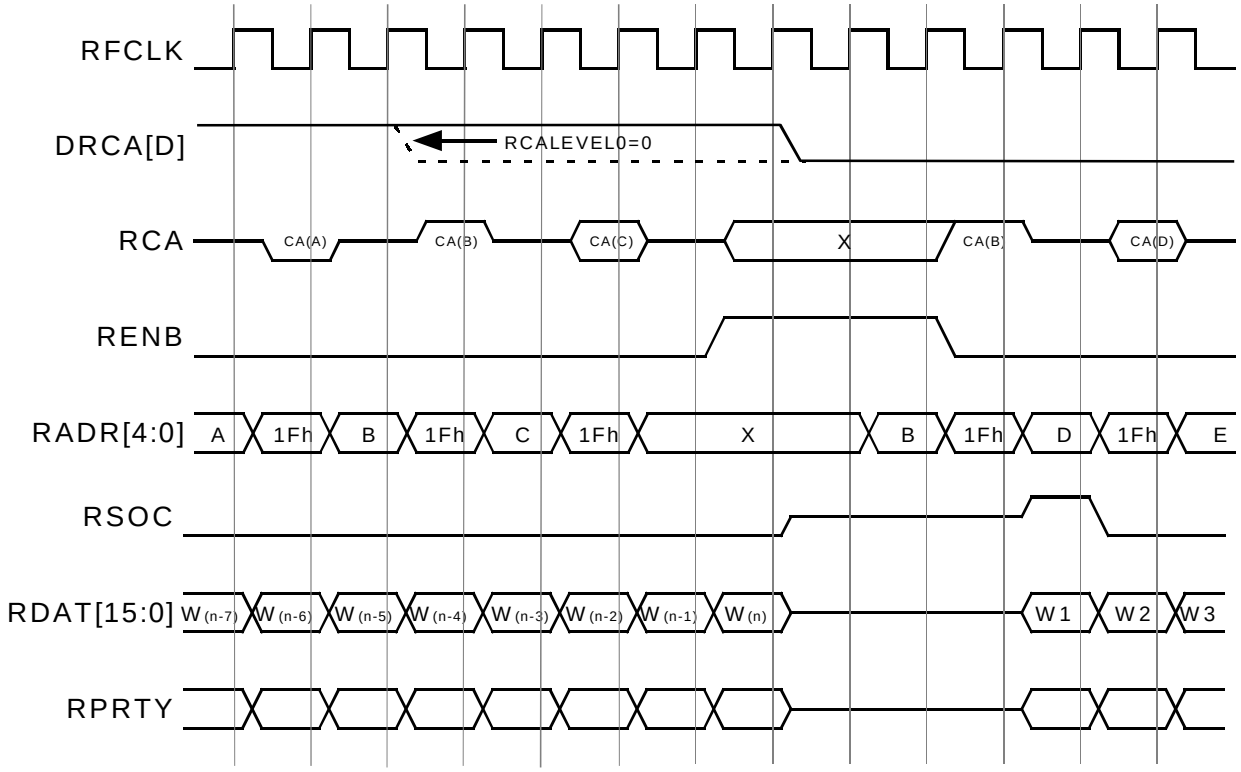


Figure 78 shows an example of the multi-PHY polling and selection sequence supported by the S/UNI-QJET. "A", "B", "C", "D", and "E" represent any arbitrary address values which may be occupied by the S/UNI-QJET. Initially cell data is

being received from PHY “D,” and the DRCA[D] signal shows how the DRCA[x] signals behave based on the value of the RCALEVEL0 register bit(s). The ATM Layer device is not restricted in its polling order. The PHY associated with address "A" indicates it does not have a cell available, but PHY "B" indicates that it does. As a result, the ATM Layer places address "B" on RADR[4:0] the cycle before RENB is asserted to select PHY "B" as the next cell source. In this example, PHY "C"s status is ignored. The ATM Layer device is not constrained to select the latest PHY polled. As soon as the cell transfer is started, the polling process may be restarted. The data on RDAT (W1, W2, ...) may be 8-bit or 16-bits wide, depending on the setting of the ATM8 input.

During multi-PHY operation, several PHY layer devices share the RDAT[15:0], RSOC, RPRTY, and RCA signals. As a result, these signals must be tri-stated in all PHY devices which have not been selected for reading or polling by the ATM Layer. Selection of which PHY layer device is being read is made by the value on RADR[4:0] the cycle before RENB is asserted and affects the RDAT[15:0], RSOC, and RPRTY signals. The value of RADR[4:0] selects the PHY being polled for the RCA signal, and all devices not corresponding to this address must tri-state its RCA output. These multi-PHY operations are directly supported by the S/UNI-QJET.

14 ABSOLUTE MAXIMUM RATINGS

Table 41 - Absolute Maximum Ratings

Ambient Temperature under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Supply VDD with respect to GND	-0.3V to 4.6V
Voltage on BIAS with respect to GND	VDD - 0.3V to 5.5V
Voltage on Any Pin	-0.3 V to BIAS +0.3 V
Static Discharge Voltage	±1000 V
Latch-Up Current	±100 mA
DC Input Current	±20 mA
Lead Temperature	+230°C
Absolute Maximum Junction Temperature	+150°C

15 D.C. CHARACTERISTICS

T_C = -40°C to +85°C, V_{DD} = 3.3V ±10%, V_{DD} < BIAS < 5.5V

(Typical Conditions: T_C = 25°C, V_{DD} = 3.3V, V_{BIAS} = 5V)

Table 42 - DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Power Supply	2.97	3.3	3.63	Volts	
BIAS	5V Tolerant Bias	VDD	5.0	5.5	Volts	
I_{BIAS}	Current into 5V Bias		6.0		µA	V_{BIAS} = 5.5V
V_{IL}	Input Low Voltage	0		0.8	Volts	Guaranteed Input Low voltage.
V_{IH}	Input High Voltage	2.0		BIAS	Volts	Guaranteed Input High voltage.
V_{OL}	Output or Bi-directional Low Voltage		0.23	0.4	Volts	Guaranteed output Low voltage at VDD=2.97V and I_{OL}=maximum rated for pad. [4, 5, 6]
V_{OH}	Output or Bi-directional High Voltage	2.4	2.93		Volts	Guaranteed output High voltage at VDD=2.97V and I_{OH}=maximum rated current for pad. [4, 5, 6]
V_{T-}	Reset Input Low Voltage			0.8	Volts	Applies to RSTB, TRSTB, TICLK[4:1], RCLK[4:1], TFCLK, RFCLK, TCK, TDI, TMS, and REF8KI.
V_{T+}	Reset Input High Voltage	2.0			Volts	Applies to RSTB, TRSTB, TICLK[4:1], RCLK[4:1], TFCLK, RFCLK, TCK, TDI, TMS, and REF8KI.
V_{TH}	Reset Input Hysteresis Voltage		0.5		Volts	Applies to RSTB, TRSTB, TICLK[4:1], RCLK[4:1], TFCLK, RFCLK, TCK, TDI, TMS, and REF8KI.
I_{ILPU}	Input Low Current	-100	-60	-10	µA	V_{IL} = GND. [1, 3]
I_{IHPU}	Input High Current	-10	0	+10	µA	V_{IH} = V_{DD}. [1, 3]
I_{IL}	Input Low Current	-10	0	+10	µA	V_{IL} = GND. [2, 3]
I_{IH}	Input High Current	-10	0	+10	µA	V_{IH} = V_{DD}. [2, 3]
C_{IN}	Input Capacitance		6		pF	t_A=25°C, f = 1 MHz
C_{OUT}	Output Capacitance		6		pF	t_A=25°C, f = 1 MHz

Symbol	Parameter	Min	Typ	Max	Units	Conditions
C_{IO}	Bi-directional Capacitance		6		pF	t_A=25°C, f = 1 MHz
I_{DDOP1}	Operating Current		299.1	375	mA	V_{DD} = 3.63V, Outputs Unloaded (DS3/PLCP mode)
I_{DDOP2}	Operating Current		12.2	30	mA	V_{DD} = 3.63V, Outputs Unloaded (T1/E1 PLCP mode)
I_{DDOP3}	Operating Current		301.3	375	mA	V_{DD} = 3.63V, Outputs Unloaded (DS3 ATM mode)
I_{DDOP4}	Operating Current		284.9	350	mA	V_{DD} = 3.63V, Outputs Unloaded (E3 ATM mode)
I_{DDOP5}	Operating Current		43.6	75	mA	V_{DD} = 3.63V, Outputs Unloaded (J2 ATM mode)
I_{DDOP6}	Operating Current		258.3	330	mA	V_{DD} = 3.63V, Outputs Unloaded (52 Mbit/s arbitrary framing format with ATM direct mapping)
I_{DDOP7}	Operating Current		268.3	330	mA	V_{DD} = 3.63V, Outputs Unloaded (DS3 framer only)
I_{DDOP8}	Operating Current		259.9	330	mA	V_{DD} = 3.63V, Outputs Unloaded (E3 framer only)
I_{DDOP9}	Operating Current		37.1	75	mA	V_{DD} = 3.63V, Outputs Unloaded (J2 framer only)

Notes on D.C. Characteristics:

1. Input pin or bi-directional pin with internal pull-up resistor.
2. Input pin or bi-directional pin without internal pull-up resistor
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).
4. The Utopia interface outputs, RDAT[15:0], RPRTY, RCA, DRCA[4:1], RSOC, TCA, and DTCA[4:1], have 12 mA drive capability.
5. The outputs TCLK[4:1], TPOS/TDATO[4:1], TNEG/TOHM[4:1], TPOHFP/TFPO/TMFPO/TGAPCLK[4:1], LCD/RDATO[4:1], RPOH/ROVRHD[4:1], RPOHCLK/RSCLK/RGAPCLK[4:1], and REF8KO/RPOHFP/RFPO/RMFPO[4:1] have 6 mA drive capability.
6. The data bus outputs, D[7:0], and all outputs not specified above have 3 mA drive capability.

7. RFCLK and TFCLK are 3.3 V only input pins – they are **not** 5 V tolerant. Connecting a 5 V signal to these inputs may result in damage to the part.

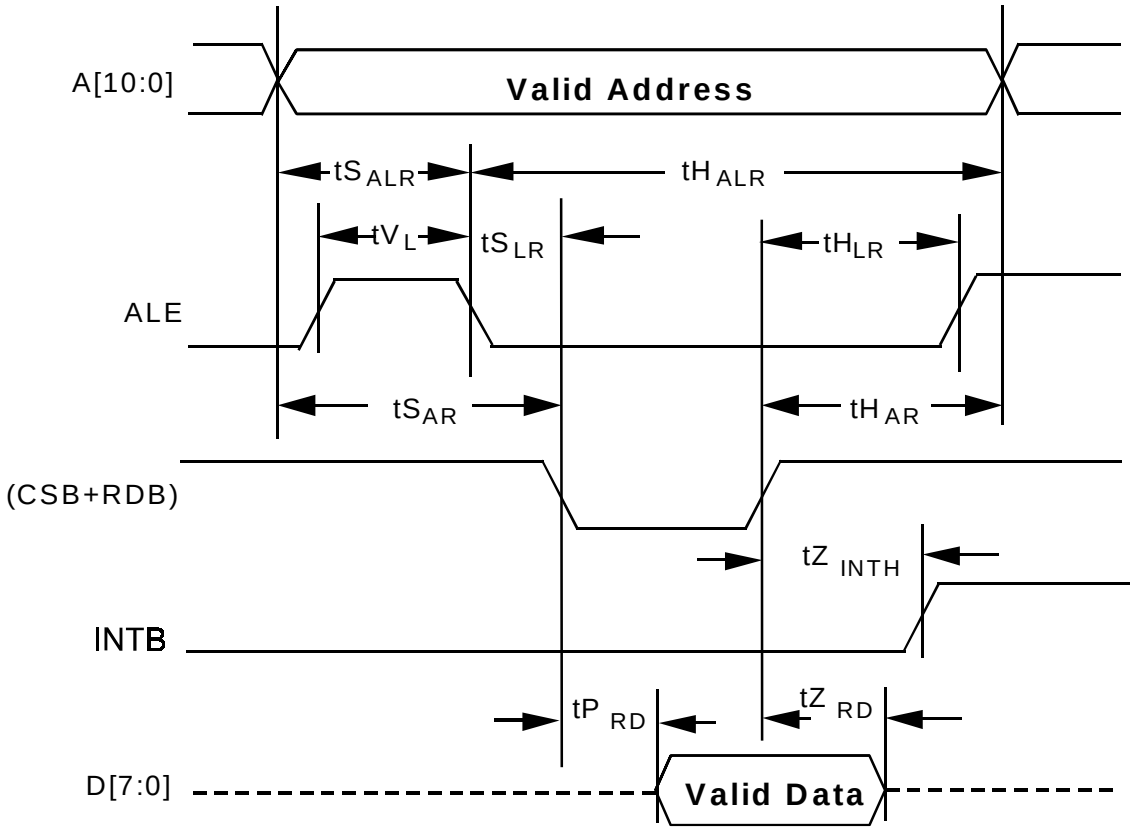
16 MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

(T_C = -40°C to +85°C, V_{DD} = 3.3V ±10%)

Table 43 - Microprocessor Interface Read Access (Figure 79)

Symbol	Parameter	Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	10		ns
tH_{AR}	Address to Valid Read Hold Time	5		ns
tS_{ALR}	Address to Latch Set-up Time	10		ns
tH_{ALR}	Address to Latch Hold Time	10		ns
tV_L	Valid Latch Pulse Width	5		ns
tS_{LR}	Latch to Read Set-up	0		ns
tH_{LR}	Latch to Read Hold	5		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		70	ns
tZ_{RD}	Valid Read Negated to Output Tri-state		20	ns
tZ_{INTH}	Valid Read Negated to Output Tri-state		50	ns

Figure 79 - Microprocessor Interface Read Timing



Notes on Microprocessor Interface Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[7:0]).

3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.

4. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALR}, tH_{ALR}, tV_L, tS_{LR}, and tH_{LR} are not applicable.

5. Parameter tH_{AR} is not applicable if address latching is used.

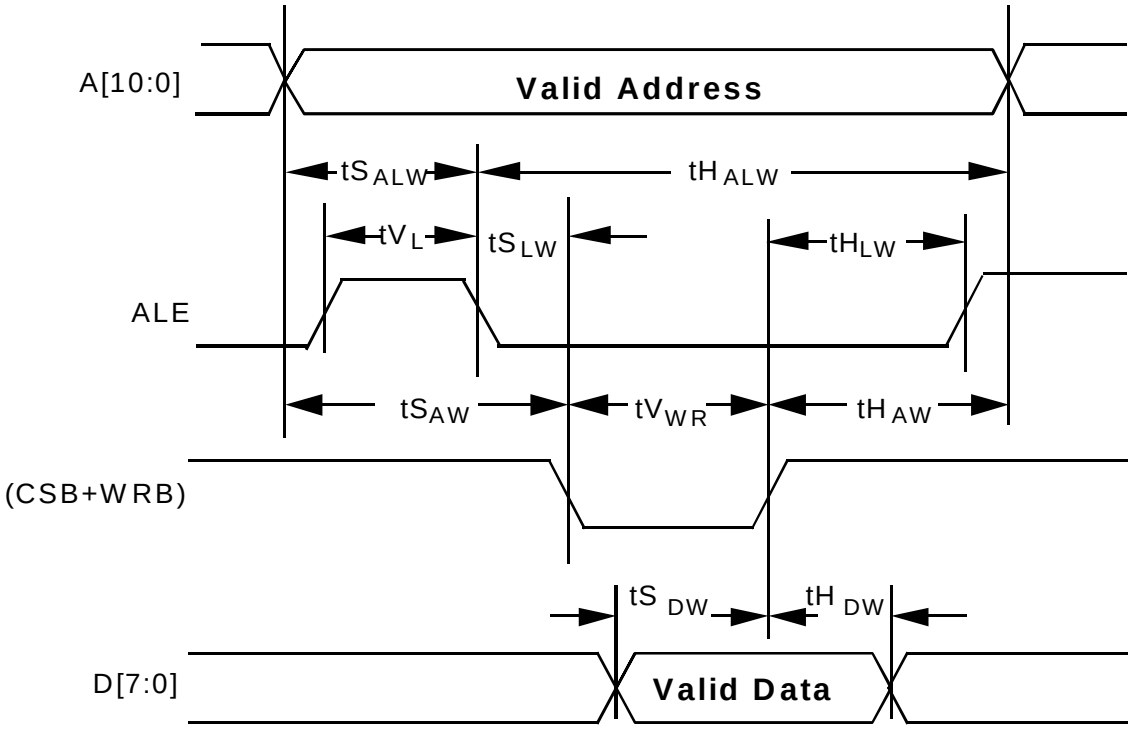
6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Table 44 - Microprocessor Interface Write Access (Figure 80)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	10		ns
tS_{DW}	Data to Valid Write Set-up Time	20		ns
tS_{ALW}	Address to Latch Set-up Time	10		ns
tH_{ALW}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	5		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	5		ns
tH_{DW}	Data to Valid Write Hold Time	5		ns
tH_{AW}	Address to Valid Write Hold Time	5		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Figure 80 - Microprocessor Interface Write Timing



Notes on Microprocessor Interface Write Timing:

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.

2. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALW}, tH_{ALW}, tV_L, tS_{LW}, and tH_{LW} are not applicable.

3. Parameter tH_{AW} is not applicable if address latching is used.

4. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

5. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

17 A.C. TIMING CHARACTERISTICS

(T_C = -40°C to +85°C, V_{DD} = 3.3V ±10%)

Table 45 - RSTB Timing (Figure 81)

Symbol	Description	Min	Typical	Max	Units
tV_{RSTB}	RSTB Pulse Width[4]		100		ns

Figure 81 - RSTB Timing

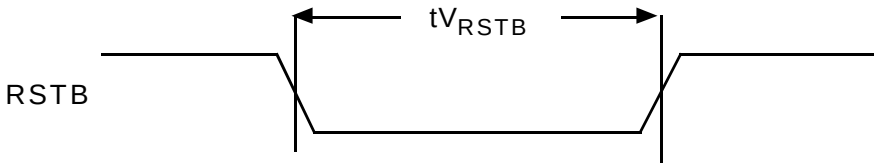


Table 46 - Transmit ATM Cell Interface Timing (Figure 82)

Symbol	Description	Min	Max	Units
f_{TFCLK}	TFCLK Frequency		52	MHz
D_{TFCLK}	TFCLK Duty Cycle	40	60	%
tS_{TFCLK}	TENB, TADR[4:0], TDAT[15:0], TPRTY, and TSOC Set-up time to TFCLK	3		ns
tH_{TFCLK}	TENB, TADR[4:0], TDAT[15:0], TPRTY, and TSOC Hold time to TFCLK	1		ns
tP_{TCA}	TFCLK High to DTCA[4:1] and TCA Valid	1	12	ns
tZ_{TCA}	TFCLK High to TCA Tri-state	1	10	ns
tZB_{TCA}	TFCLK High to TCA Driven	1		ns

Figure 82 - Transmit ATM Cell Interface Timing

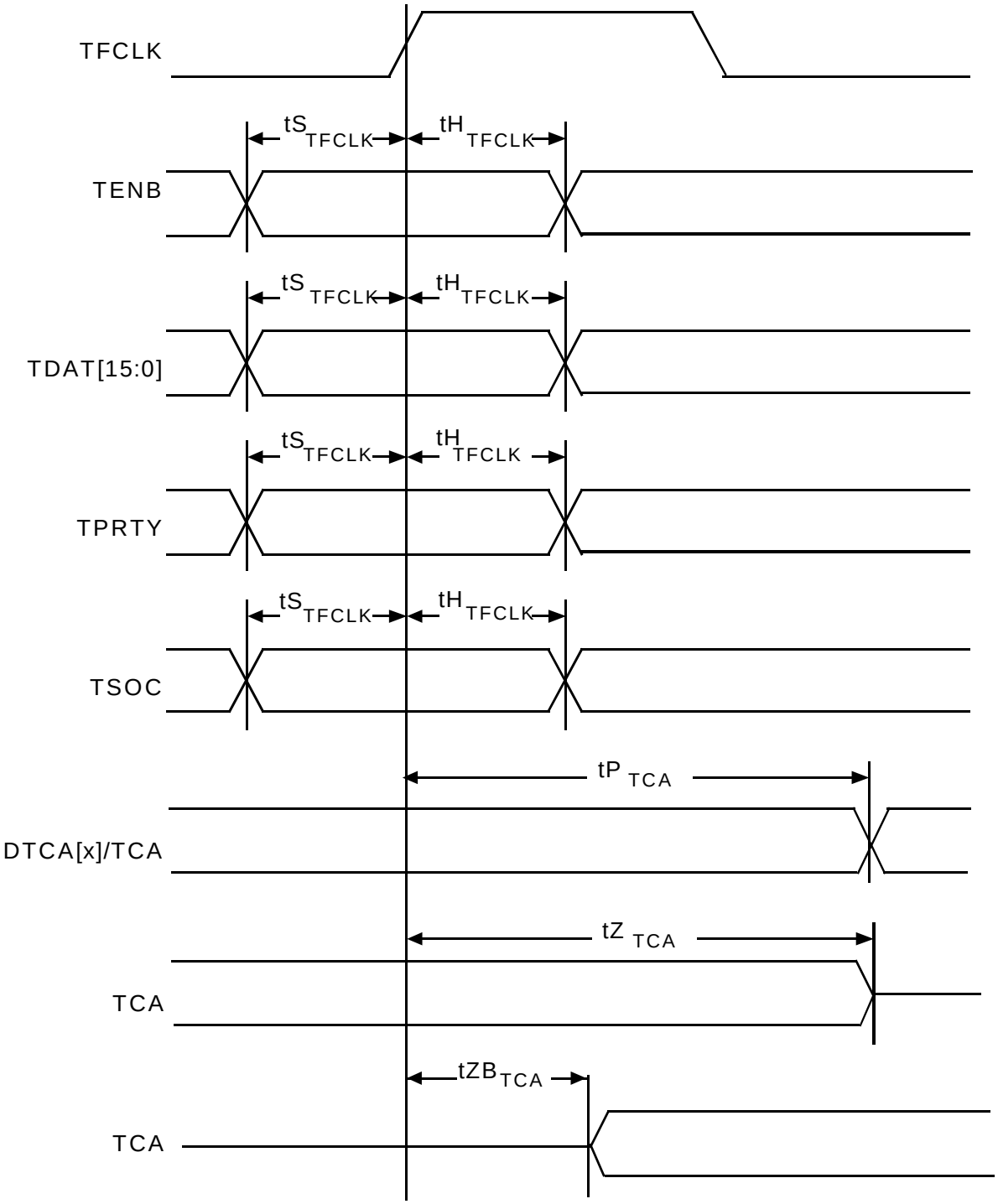
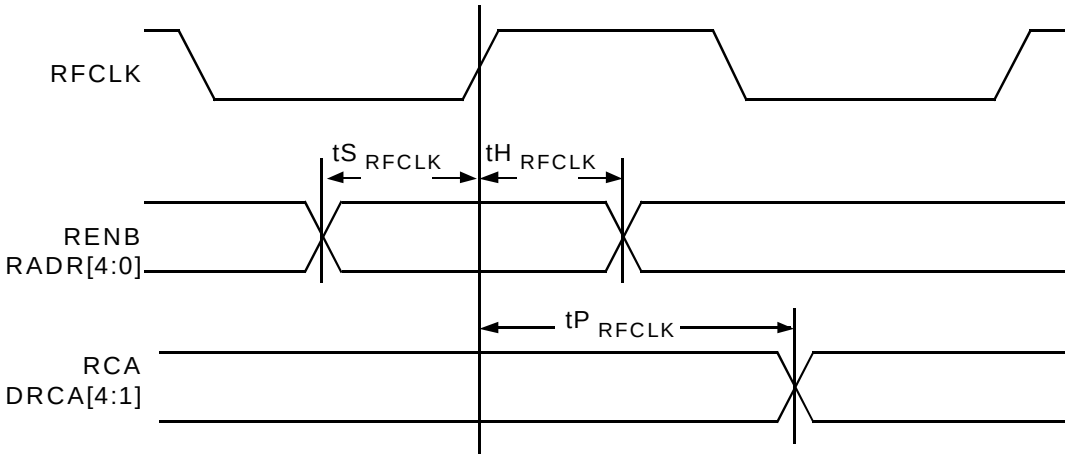


Table 47 - Receive ATM Cell Interface Timing (Figure 83)

Symbol	Description	Min	Max	Units
f_{RFCLK}	RFCLK Frequency		52	MHz
D_{RFCLK}	RFCLK Duty Cycle	40	60	%
tS_{RFCLK}	RENB and RADR[4:0] Set-up time to RFCLK	3		ns
tH_{RFCLK}	RENB and RADR[4:0] Hold time to RFCLK	1		ns
tP_{RFCLK}	RFCLK High to Output Valid	1	12	ns
tZ_{RFCLK}	RFCLK High to Output Tri-state	1	12	ns
tZB_{RFCLK}	RFCLK High to Output Driven	1		ns

Figure 83 - Receive ATM Cell Interface Timing



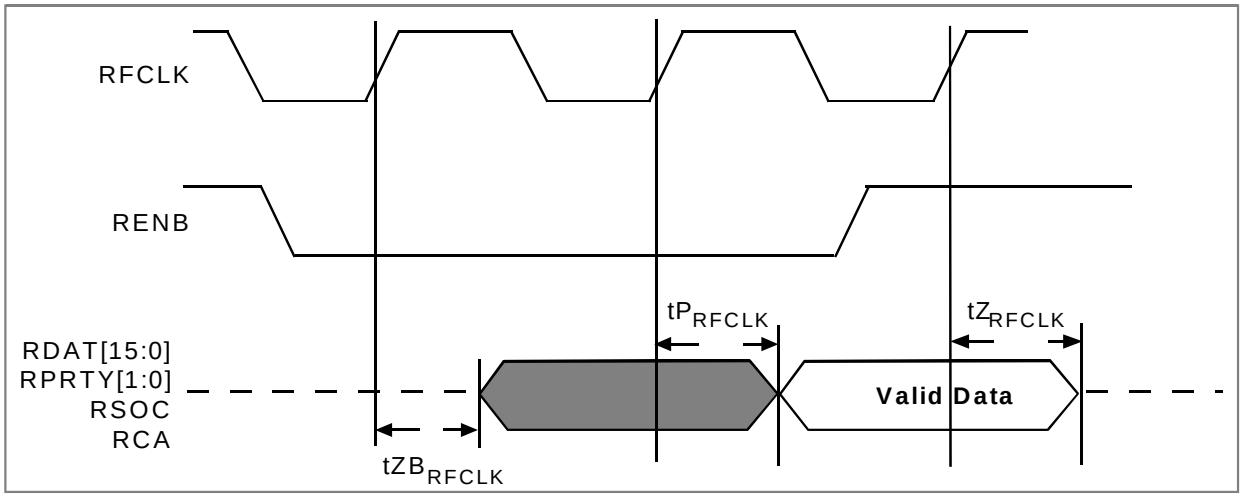


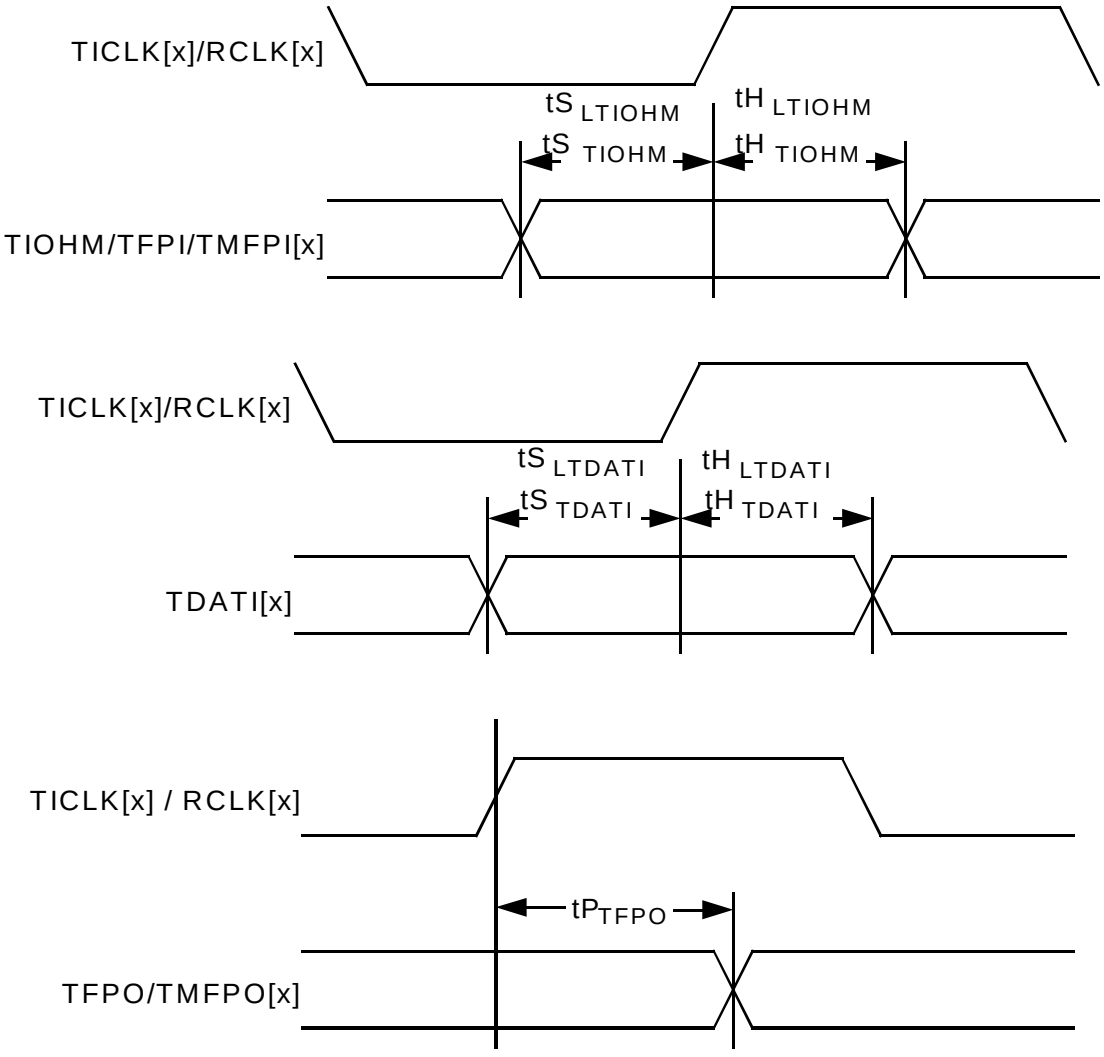
Table 48 - Transmit Interface Timing (Figure 84)

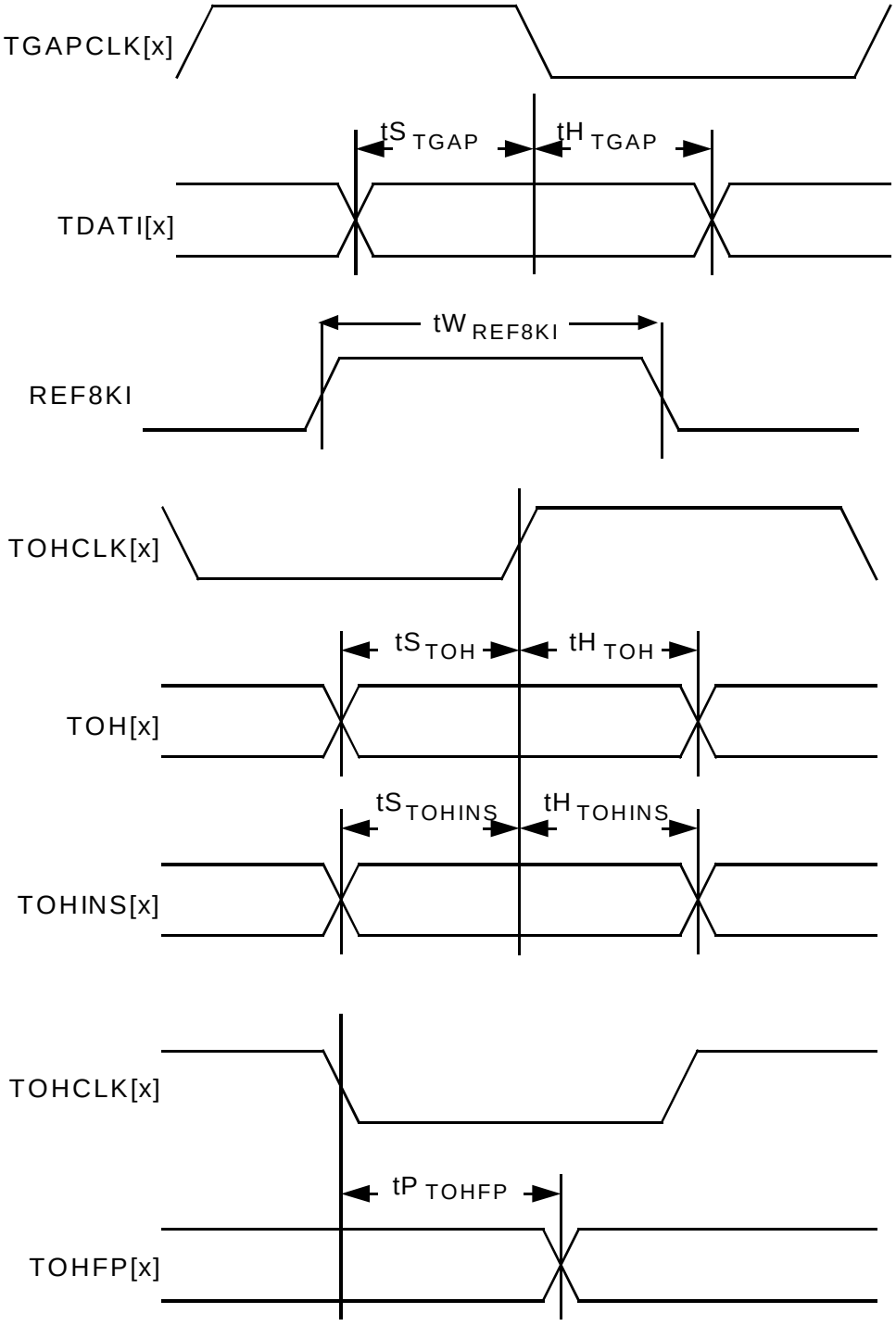
Symbol	Description	Min	Typ	Max	Units
f_{TICLK}	TICLK[x] Frequency: DS3 Framer (TFRM[1:0] = 00) E3 Framer (TFRM[1:0] = 01) J2 Framer (TFRM[1:0] = 10) framer bypass (TFRM[1:0] = 11)			 52 35 7 52	MHz
$t0_{TICLK}$	TICLK[x] minimum pulse width low: DS3 Framer (TFRM[1:0] = 00) E3 Framer (TFRM[1:0] = 01) J2 Framer (TFRM[1:0] = 10) framer bypass (TFRM[1:0] = 11)	 7.7 11 57 7.7			ns
$t1_{TICLK}$	TICLK[x] minimum pulse width high: DS3 Framer (TFRM[1:0] = 00) E3 Framer (TFRM[1:0] = 01) J2 Framer (TFRM[1:0] = 10) framer bypass (TFRM[1:0] = 11)	 7.7 11 57 7.7			ns
tS_{TIOHM}	TIOHM/TFPI/TMFPI[x] to TICLK[x] Set-up Time	5			ns
tH_{TIOHM}	TIOHM/TFPI/TMFPI[x] to TICLK[x] Hold Time	1			ns
tS_{TDATI}	TDATI[x] to TICLK[x] Set-up Time	5			ns
tH_{TDATI}	TDATI[x] to TICLK[x] Hold Time	1			ns
tS_{LTIOHM}	TIOHM/TFPI/TMFPI[x] to RCLK[x] Set-up Time (LOOPT=1)	5			ns
tH_{LTIOHM}	TIOHM/TFPI/TMFPI[x] to RCLK[x] Hold Time (LOOPT=1)	1			ns
tS_{LTDATI}	TDATI[x] to RCLK[x] Set-up Time (LOOPT=1)	5			ns

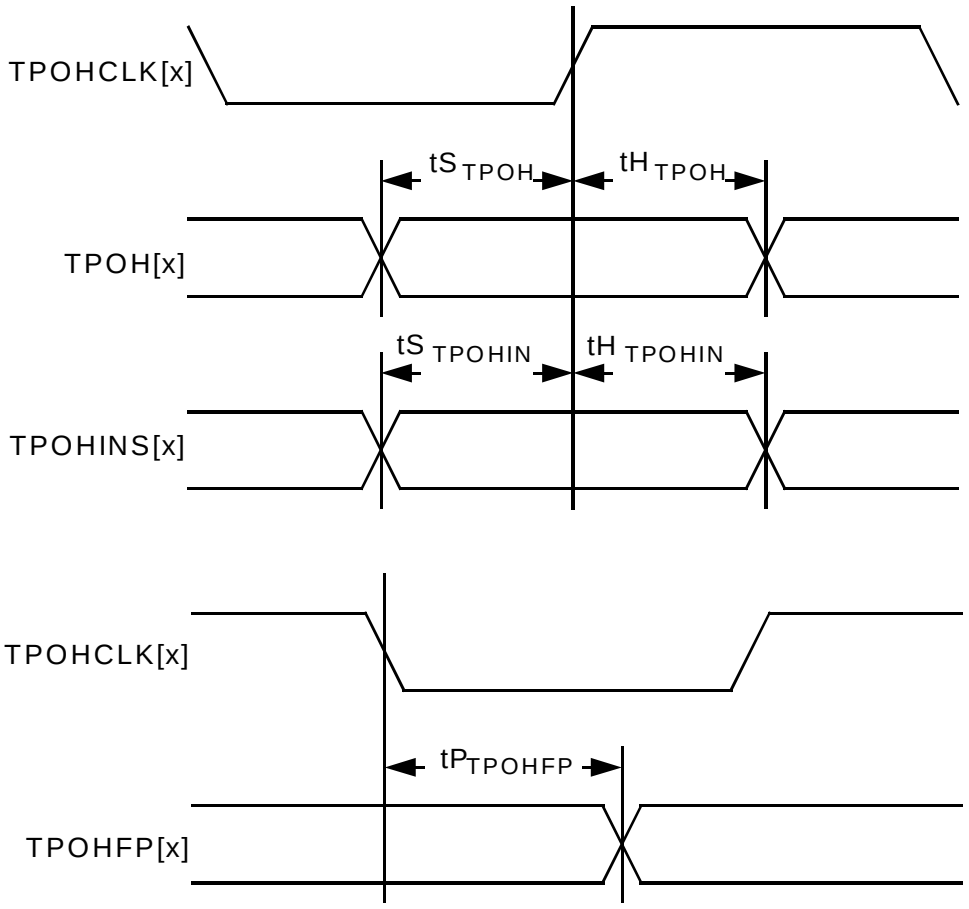
Symbol	Description	Min	Typ	Max	Units
tH_{LTDATI}	TDATI[x] to RCLK[x] Hold Time (LOOPT=1)	1			ns
tP_{TFPO}	TICLK[x] to TFPO/TMFPO[x] Prop Delay, or RCLK[x] to TFPO/TMFPO[x] Prop Delay when loop timing is used.	2		16	ns
tS_{TGAP}	TDATI[x] to TGAPCLK[x] Set-up Time	3			ns
tH_{TGAP}	TDATI[x] to TGAPCLK[x] Hold Time	2			ns
tW_{REF8KI}	REF8KI pulse width[4]		15		ns
tS_{TOH}	TOH[x] to TOHCLK[x] Set-Up Time	20			ns
tH_{TOH}	TOH[x] to TOHCLK[x] Hold Time	20			ns
tS_{TOHINS}	TOHINS[x] to TOHCLK[x] Set-Up Time	20			ns
tH_{TOHINS}	TOHINS[x] to TOHCLK[x] Hold Time	20			ns
tP_{TOHFP}	TOHCLK[x] to TOHFP[x] Prop Delay	-15		20	ns
tS_{TPOH}	TPOH[x] to TPOHCLK[x] Set-Up Time	20			ns
tH_{TPOH}	TPOH[x] to TPOHCLK[x] Hold Time	20			ns
tS_{TPOHIN}	TPOHINS[x] to TPOHCLK[x] Set-Up Time	20			ns
tH_{TPOHIN}	TPOHINS[x] to TPOHCLK[x] Hold Time	20			ns
tP_{TPOHFP}	TPOHCLK[x] to TPOHFP[x] Prop Delay	-15		20	ns
tP_{TPOS}	TCLK[x] Edge to TPOS/TDATO[x] Prop Delay	-1		4.5	ns
tP_{TNEG}	TCLK[x] Edge to TNEG/TOHM[x] Prop Delay	-1		4.5	ns
tP_{TPOS2}	TICLK[x] High to TPOS/TDATO[x] Prop Delay	2		13	ns

Symbol	Description	Min	Typ	Max	Units
tP_{TNEG2}	TICLK[x] High to TNEG/TOHM[x] Prop Delay	2		13	ns

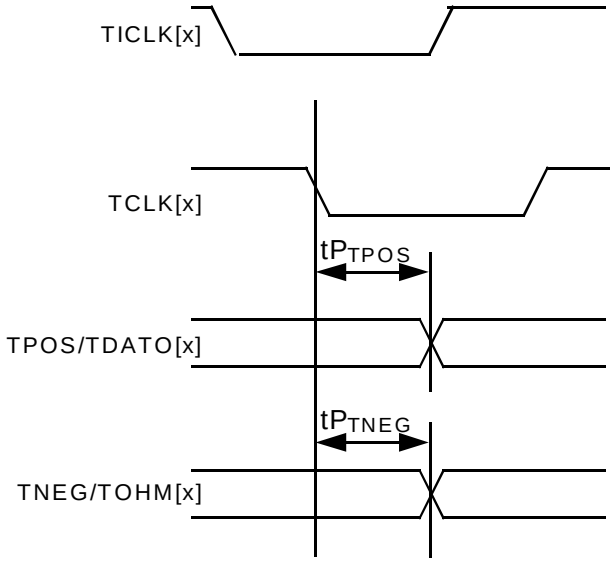
Figure 84 - Transmit Interface Timing



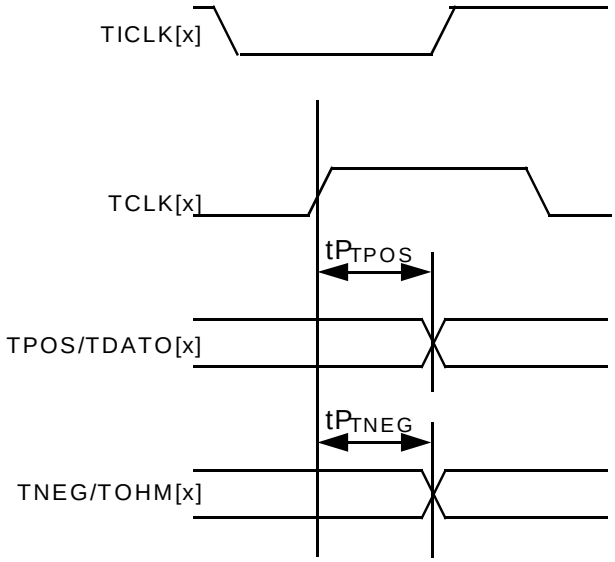

TGAPCLK[x]
tS TGAP
tH TGAP
TDATI[x]
tW REF8KI
REF8KI
TOHCLK[x]
tS TOH
tH TOH
TOH[x]
tS TOHINS
tH TOHINS
TOHINS[x]
TOHCLK[x]
tP TOHFP
TOHFP[x]


TPOHCLK[x]
tS TPOH
tH TPOH
TPOH[x]
tS TPOHIN
tH TPOHIN
TPOHINS[x]
TPOHCLK[x]
tP TPOHFP
TPOHFP[x]

TICLK=0, TCLKINV=0



TICLK=0, TCLKINV=1



TICLK=1, TCLKINV=X

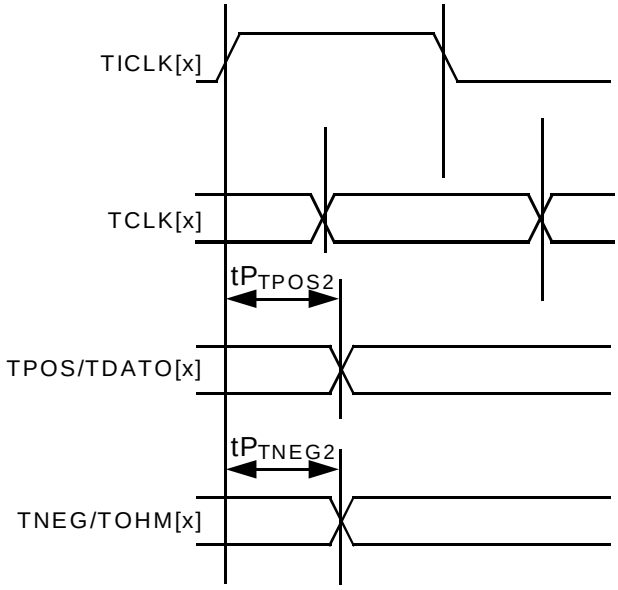
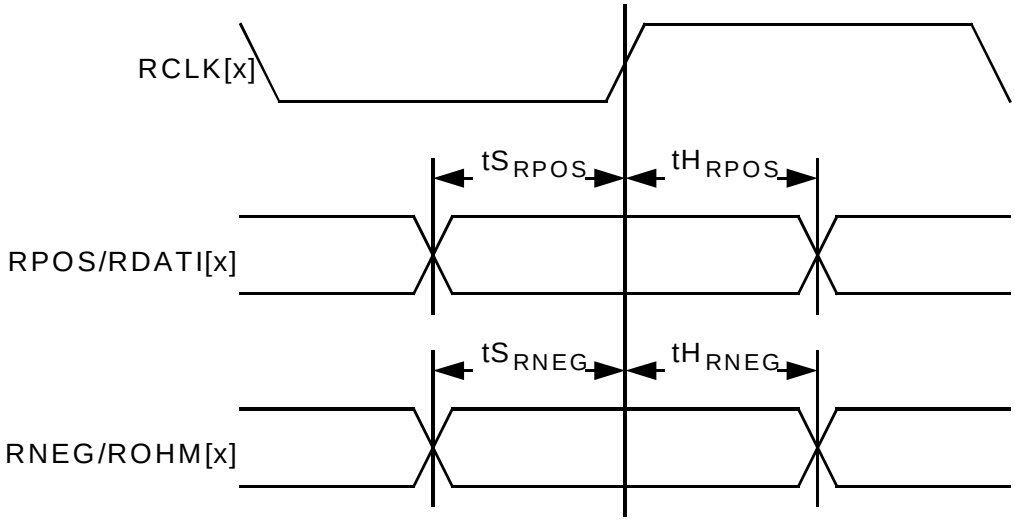


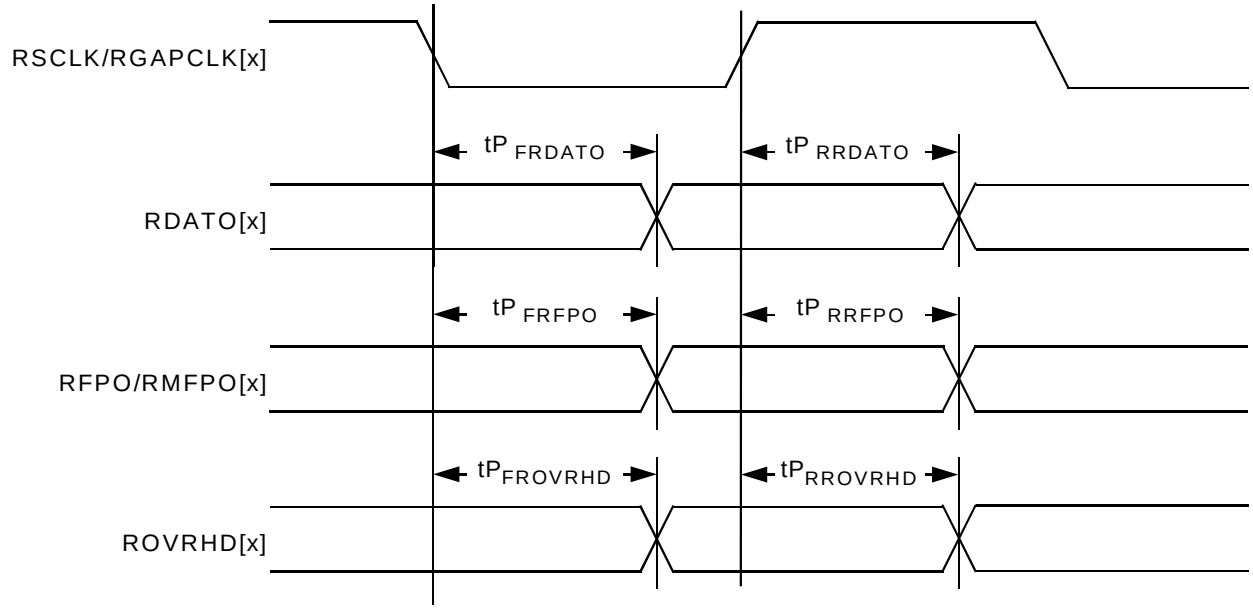
Table 49 - Receive Interface Timing (Figure 85)

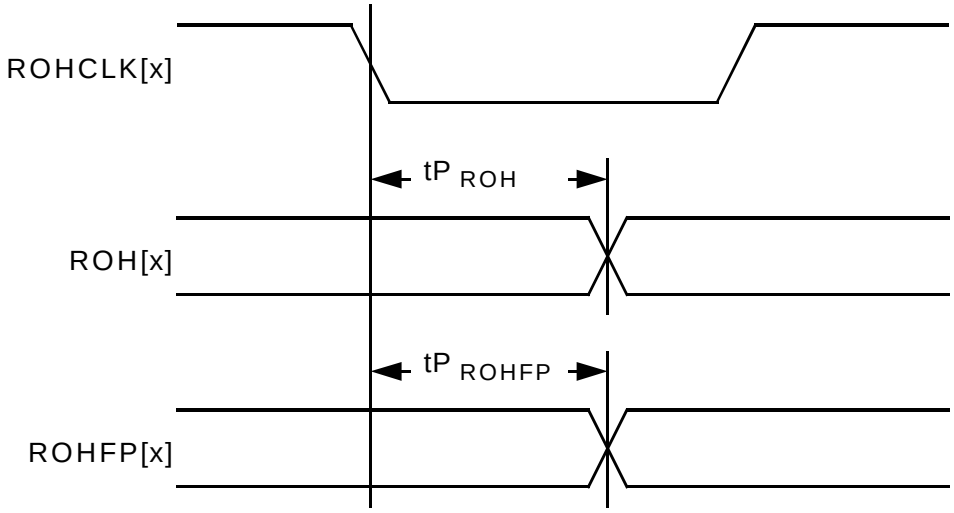
Symbol	Description	Min	Max	Units
f_{RCLK}	RCLK[x] Frequency:			
	DS3 Framer (RFRM[1:0] = 00)		52	MHz
	E3 Framer (RFRM[1:0] = 01)		35	
	J2 Framer (RFRM[1:0] = 10)		7	
	framer bypass (RFRM[1:0] = 11)		52	MHz
$t0_{RCLK}$	RCLK[x] minimum pulse width low:			
	DS3 Framer (RFRM[1:0] = 00)	7.7		ns
	E3 Framer (RFRM[1:0] = 01)	11		
	J2 Framer (RFRM[1:0] = 10)	57		
	framer bypass (RFRM[1:0] = 11)	7.7		
$t1_{RCLK}$	RCLK[x] minimum pulse width high:			
	DS3 Framer (RFRM[1:0] = 00)	7.7		ns
	E3 Framer (RFRM[1:0] = 01)	11		
	J2 Framer (RFRM[1:0] = 10)	57		
	framer bypass (RFRM[1:0] = 11)	7.7		
tS_{RPOS}	RPOS/RDATI Set-up Time	4		ns
tH_{RPOS}	RPOS/RDATI Hold Time	1		ns
tS_{RNEG}	RNEG/ROHM Set-Up Time	4		ns
tH_{RNEG}	RNEG/ROHM Hold Time	1		ns
tP_{RRDATO}	RSCLK[x]/RGAPCLK[x] rising edge to RDATO[x] Prop Delay	2	13	ns
tP_{RRFPO}	RSCLK[x] rising edge to RFPO/RMFPO[x] Prop Delay	1	13	ns
$tP_{RROVRHD}$	RSCLK[x] rising edge to ROVRHD[x] Prop Delay	1	13	ns
tP_{FRDATO}	RSCLK[x]/RGAPCLK[x] falling edge to RDATO[x] Prop Delay	-2	10	ns

Symbol	Description	Min	Max	Units
tP_{FRFPO}	RSCLK[x] falling edge to RFPO/RMFPO[x] Prop Delay	-2	10	ns
$tP_{FROVRHD}$	RSCLK[x] falling edge to ROVRHD[x] Prop Delay	-2	10	ns
tP_{ROH}	ROHCLK[x] Low to ROH[x] Prop Delay	-15	20	ns
tP_{ROHFP}	ROHCLK[x] Low to ROHFP[x] Prop Delay	-15	20	ns
tP_{RPOH}	RPOHCLK[x] Low to RPOH[x] Prop Delay	-15	20	ns
tP_{RPOHFP}	RPOHCLK[x] Low to RPOHFP[x] Prop Delay	-15	20	ns

Figure 85 - Receive Interface Timing




RSCLK/RGAPCLK[x]
tP FRDATO
tP RRDATO
RDATO[x]
tP FRFPO
tP RRFPO
RFPO/RMFPO[x]
tPFROVRHD
tPRROVRHD
ROVRHD[x]


ROHCLK[x]
tP ROH
ROH[x]
tP ROHFP
ROHFP[x]

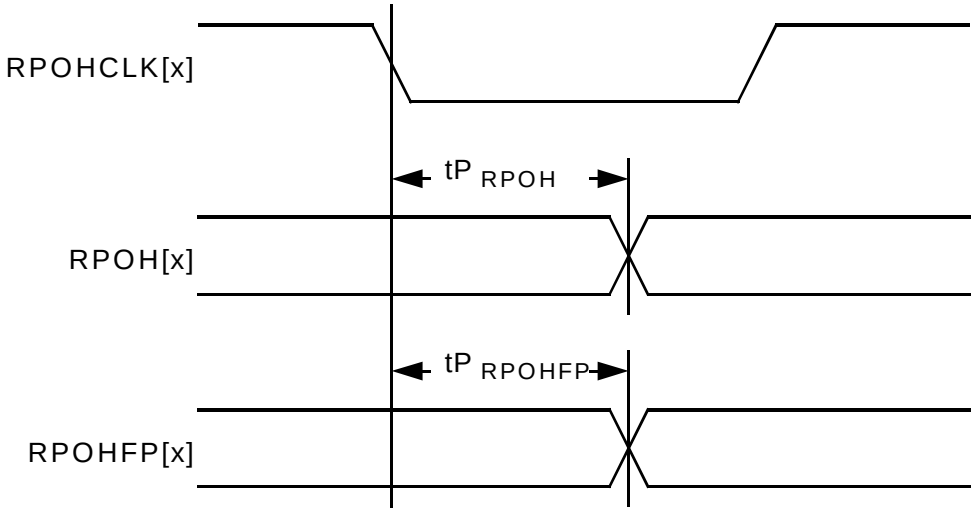
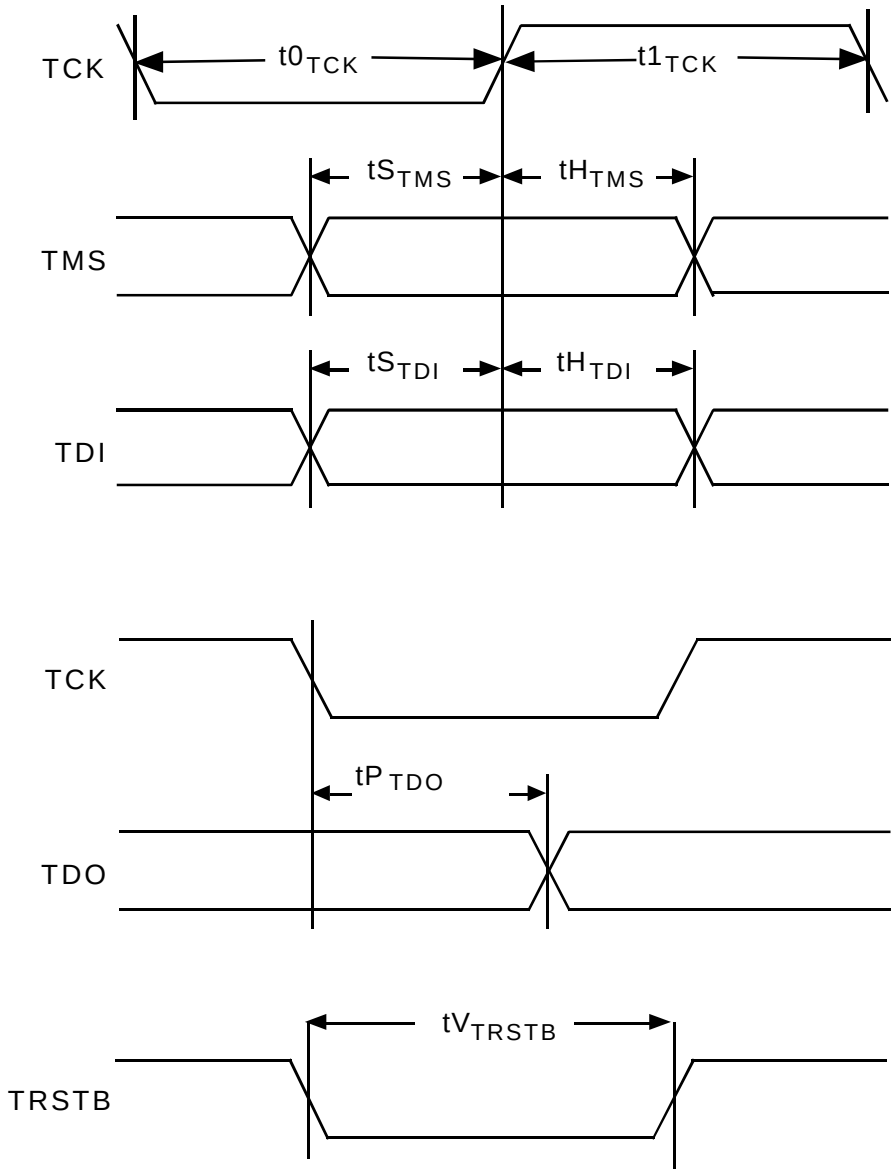

RPOHCLK[x]
tP RPOH
RPOH[x]
tP RPOHFP
RPOHFP[x]

Table 50 - JTAG Port Interface (Figure 86)

Symbol	Description	Min	Typical	Max	Units
$t1_{TCK}$	TCK high pulse width[5]				ns
$t0_{TCK}$	TCK low pulse width[5]	100			ns
tS_{TMS}, tS_{TDI}	TMS and TDI Set-up time to TCK[1]	50			ns
TH_{TMS}, TH_{TDI}	TMS and TDI Hold time to TCK[2]	50			ns
TP_{TDO}	TCK Low to TDO Valid[6,7]	2		50	ns
TV_{TRSTB}	TRSTB minimum pulse width[4,5]		100		ns

Figure 86 - JTAG Port Interface Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

3. It is recommended that the load on TGAPCLK[x] be kept less than 50pF. A larger load on these pins may result in functional failures.

4. This parameter is guaranteed by design. No production tests are done on this parameter.

5. High pulse width is measured from the 1.4 Volt points of the rise and fall ramps. Low pulse width is measured from the 1.4 Volt points of the fall and rise ramps.

Notes on Output Timing:

6. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

7. Maximum and minimum output propagation delays are measured with a 50 pF load on the outputs.

18 ORDERING AND THERMAL INFORMATION

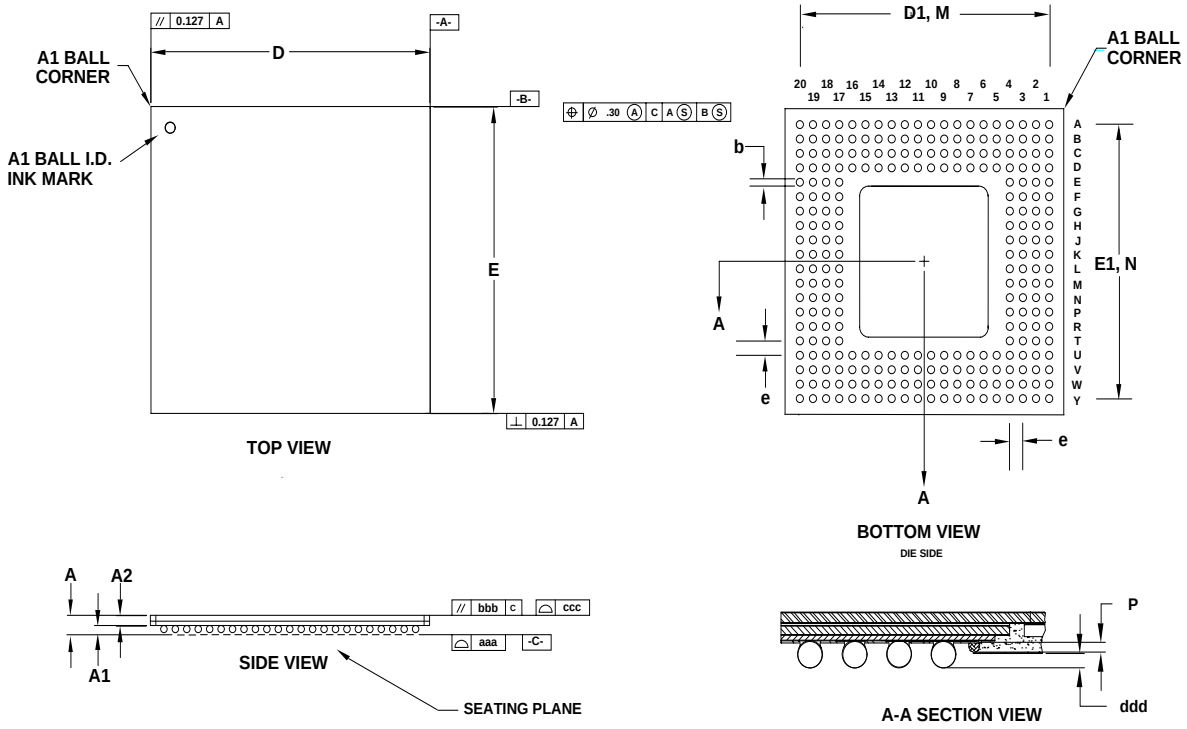
Table 51 - Packaging Information

PART NO	DESCRIPTION
PM7346	256-pin Ball Grid Array (SBGA)

Table 52 - Thermal Information

PART NO.	CASE TEMPERATURE	Theta Ja	Theta Jc
PM7346	-40°C to 85°C	19 °C/W	5 °C/W

19 MECHANICAL INFORMATION



Notes: 1) ALL DIMENSIONS IN MILLIMETER.

2) DIMENSION aaa DENOTES COPLANARITY

3) DIMENSION bbb DENOTES PARALLEL

4) DIMENSION ccc DENOTES FLATNESS

PACKAGE TYPE: 256 PIN THERMAL BALL GRID ARRAY															
BODY SIZE: 27 x 27 x 1.45 MM															
Dim.	A	A1	A2	D	D1	E	E1	M,N	e	b	aaa	bbb	ccc	ddd	P
Min.	1.32	0.56	0.76	26.90	24.03	26.90	24.03			0.60				0.15	0.20
Nom.	1.45	0.63	0.82	27.00	24.13	27.00	24.13	20x20	1.27	0.75				0.33	0.30
Max.	1.58	0.70	0.88	27.10	24.23	27.10	24.23			0.90	0.15	0.15	0.20	0.50	0.35

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Application Information: apps@pmc-sierra.com

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