PLESSEY
Semiconductors

NJ88C31

MF/VHF SYNTHESISER

The NJ88C31 contains all the logic needed for an MF/VHF PLL synthesiser and is fabricated on Plessey high performance small geometry CMOS. The circuit contains a reference oscillator and divider, a two modulus prescaler and 4-bit control register, a 12-bit programmable divider, a phase comparator and the necessary data input and control logic, and a 4.5MHz μP clock drive output.

FEATURES

- Low Power CMOS
- Easy To Use
- Low Cost
- Single Chip Synthesiser
- Lock Detect Output
- 4.5MHzμP Clock Output
- MF Band Prescaler Bypass Function
- Front End Disable for Very Low Power Standby
- Band Output to Switch Radio Between MF and VHF

APPLICATIONS

- AM/FM Radios
- Car Radios

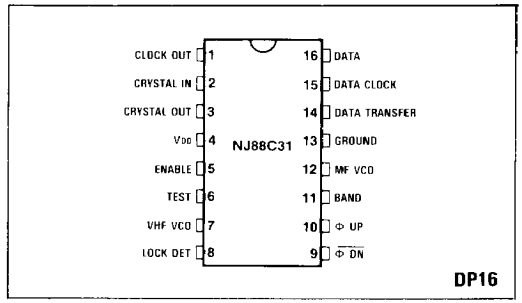

Fig.1 Pin connections (plastic DIL - top view)

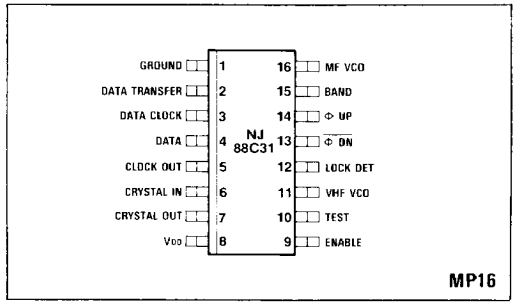

Fig.2 Pin connections (miniature plastic DIL - top view)

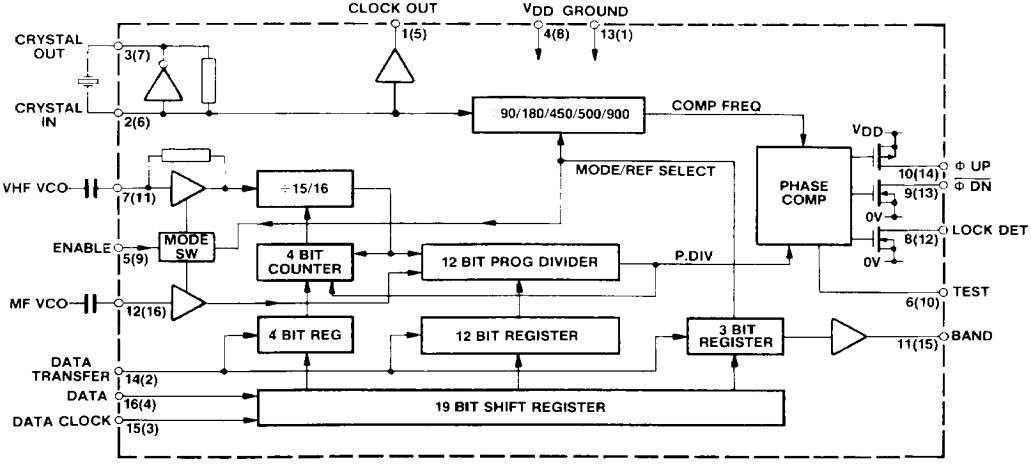

Fig.3 Functional block diagram. Pin numbers for MP package are shown in brackets.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = -30°C to +70°C, V_{DD} = 5V ± 0.5V

ABSOLUTE MAXIMUM RATINGS

V_{DD}	-0.3V to +6V
Voltage on any pin	-0.3V to V_{DD} +0.3V
Operating temperature	-30°C to +70°C
Storage temperature	-55°C to +125°C

Characteristic	Pin MP16	Pin DP16	Value Min.	Value Typ.	Value Max.	Units	Conditions
Supply							
Supply current	8	4		4	7	mA	1V rms VHF VCO input at 120MHz and f_{XTAL} = 4.5MHz
Supply current (Standby mode)					2	mA	f_{XTAL} = 4.5MHz, Enable low
Crystal oscillator							
Frequency	6,7	2,3		4.5	15	MHz	Parallel resonant, fundamental crystal
External input level	6	2	1			V rms	AC coupled
High level	6	2	V_{DD}-1			V	DC coupled
Low level	6	2			1	V	DC coupled
VCO inputs							
VHF VCO input sensitivity	13	7	0.3			V rms	At 50 to 125MHz, see Fig.4
MF VCO input sensitivity	16	12	0.3			V rms	At 0.1 to 2.5MHz
VCO input impedance	13,16	7,12		5pF/10kΩ			
DATA, DATA TRANSFER, DATA CLOCK, TEST and ENABLE inputs							
High level	2,3,4 9,10	5,6, 14,15,16	V_{DD}-1			V	
Low level	2,3,4, 9,10	5,6, 14,15,16			1	V	
Rise, fall time	2,3	14,15			200	ns	
Data set up time	3,4	15,16	200			ns	See Fig.5
Clock frequency	3	15			2	MHz	
Transfer pulse width	2	14	500			ns	
CLOCK OUT, BAND							
Current sink	5,15	1,11	0.8			mA	V_{OUT} = 0.5V
Current source	5,15	1,11	0.8			mA	V_{OUT} = V_{DD} -0.5V
LOCK DET							
Current sink	12	8	1.6			mA	V_{OUT} = 0.5V
Φ UP/$\overline{\Phi}$ DN, BAND							
Current sink	13	9	0.8			mA	V_{OUT} = 0.5V
Current source	14	10	0.8			mA	V_{OUT} = V_{DD} -0.5V

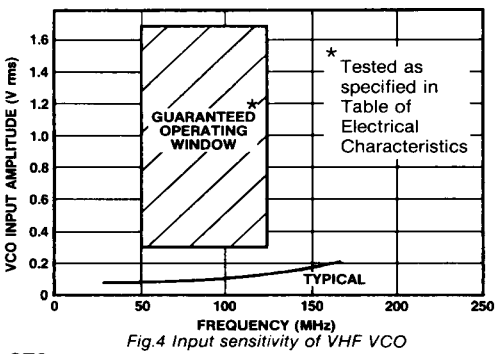

Fig.4 Input sensitivity of VHF VCO

CIRCUIT DESCRIPTION

Crystal Oscillator and Reference Divider

The reference oscillator consists of a Pierce type oscillator intended for use with parallel resonant fundamental crystals. Typical gain and phase characteristics for the oscillator inverter are shown in Fig.6. An external reference oscillator may be used by either capacitively coupling a 1V rms sinewave into the CRYSTAL IN pin or if CMOS logic levels are available by connecting directly to the CRYSTAL IN pin.

The reference oscillator drives a divider to produce a range of comparison frequencies which are selected by decoding the first three bits (DR2, DR1, DR0) of the input data. The possible division ratios and the comparison frequencies if a 4.5MHz crystal is used are shown in Fig.7.

There is a 4.5MHz μP clock drive output available on the CRYSTAL OUT pin.

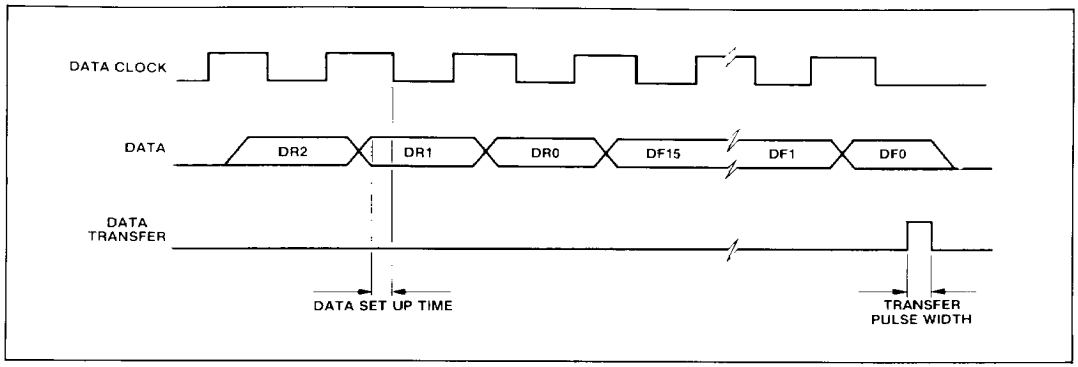

Fig.5 Input data timing diagram

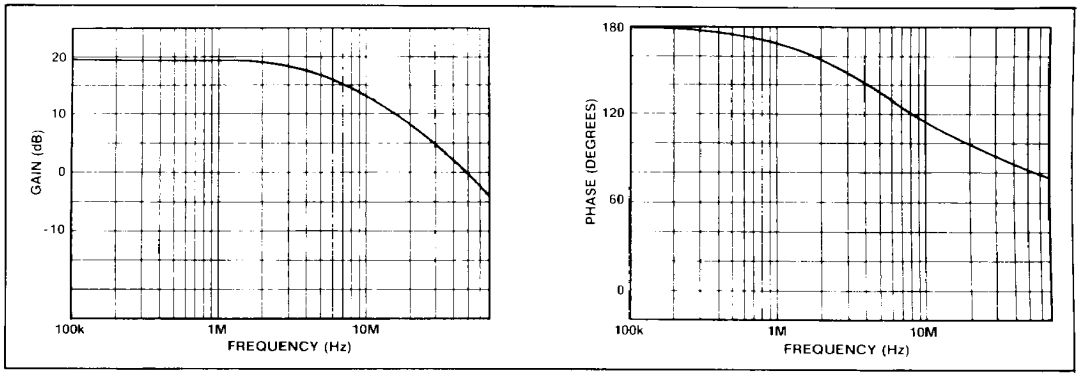

Fig.6 Gain phase characteristics of reference oscillator inverter

BAND Output

The programming bit DR2 is brought out as a BAND output, '1' for MF band and '0' for VHF.

DR2	DR1	DR0	Division Ratio	Comparison Frequency 4.5MHz XTAL	BAND
0	0	0	90	50kHz	VHF
0	0	1	180	25kHz	
0	1	0	450	10kHz	
1	0	0	450	10kHz	MF
1	0	1	500	9kHz	
1	1	0	900	5kHz	

Fig.7 Reference divider division ratios

Programmable Divider

The programmable divider consists of a 12-bit divider preceded on FM by a divide by 15/16 two modulus divider. The F/M input is fed through an amplifier to provide adequate sensitivity.

TEST Input

When the TEST pin is taken to a logic 1, the Φ UP pin is connected to the output of the reference chain divider (COMP FREQ) and the $\Phi\ \overline{DN}$ pin is connected to the output of the 12-bit programmable signal chain divider (PROG DIV); this mode is normally only used in factory testing.

Phase Comparator

The digital phase comparator has three open drain outputs; Φ UP and $\overline{\Phi\ DN}$ drive the charge pump and LOCK DETECT may be integrated to generate a MUTE signal. Waveforms for all these outputs are shown in Fig.8. The duty cycle of Φ UP and $\overline{\Phi\ DN}$ versus phase difference are shown in Fig.9. The phase comparator is linear over a $\pm 2\pi$ range and if the phase gains or slips by more than 2π the phase comparator outputs repeat with a 2π period. Once the phase difference exceeds 2π the comparator will gain or slip one cycle and then try to lock to the new zero phase difference. Note very narrow pulses may be seen on the inactive phase comparator output at the end of the pulse on the active output.

ENABLE Input

When ENABLE is taken to logic '0' both VCO input buffers and the prescaler are switched off to save power. The crystal oscillator, CLOCK OUT and control registers continue working normally, such that when ENABLE is taken to a '1' the device will retune the last programmed frequency.

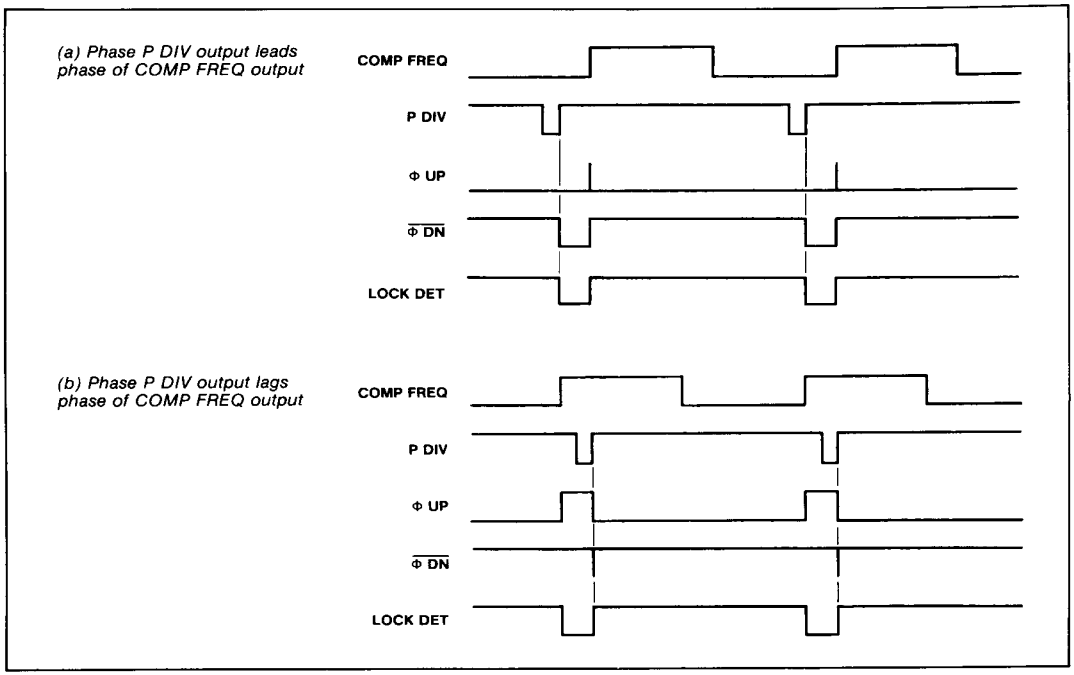

Fig.8 Phase comparator waveforms

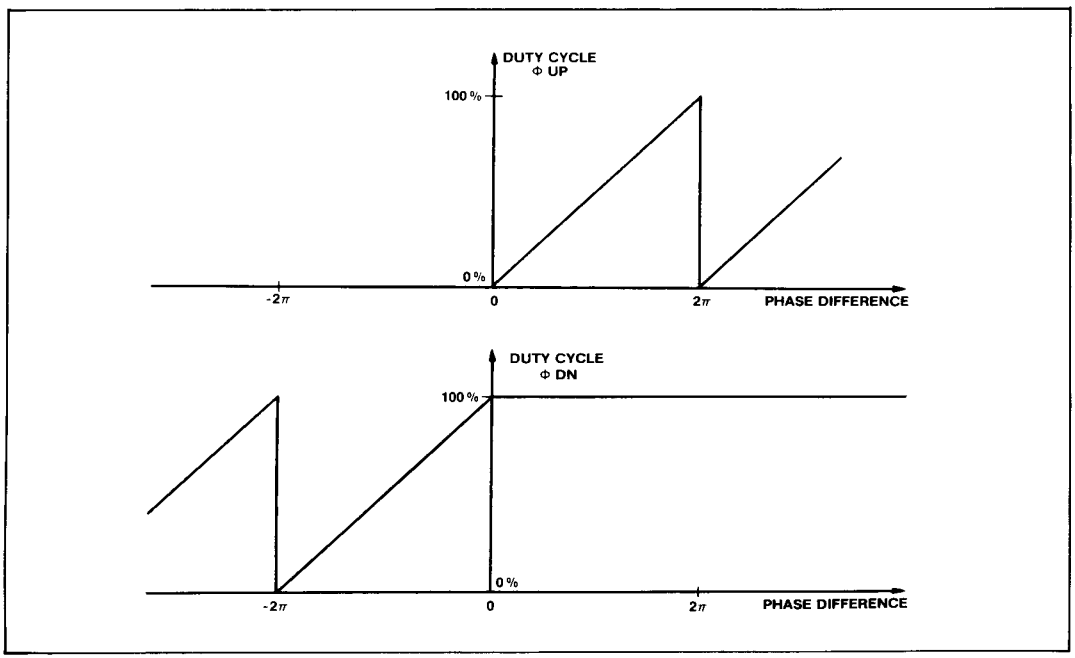

Fig.9 Phase comparator output characteristics

Data Input and Control Register

To control the synthesiser a simple three line serial input is used with Data, Clock and Data Transfer signals. The data consists of 19 bits, the first three DR2, DR1, DR0 control the reference divider, the next sixteen, DF15 to DF0, control the prescaler and programmable divider. Until the synthesiser receives the Data Transfer pulse it will use the previously loaded data; on receiving the pulse it will switch rapidly to the new data. See Fig.5.

APPLICATIONS

A simplified circuit for a synthesiser intended for VHF broadcast receiver applications is shown in Fig.10. When the varicap line drive voltage necessary to tune the required band is greater than 5V, some form of level shifter such as the operational amplifier shown in Fig.10 is required.Pulses from the phase comparator are filtered by R_1, R_2, and C_1. Their values can be determined, given a required natural loop bandwidth ω_n and damping factor δ, by the following equations:

$$R_1C_1 = \frac{K}{\omega_n^2}, R_2C_1 = \frac{2\delta}{\omega_n} \text{ and } K = \frac{K_0 \times V_{CC} \times G}{2\pi N}$$

where

ω - natural loop bandwidth (rad/s)
δ - damping factor
K_0 - VCO gain factor (rad/Vs)
V_{CC} - charge pump supply voltage (V)
N - division ratio = f_{OUT}/f_{COMP}
G - Gain of amplifier

The values in Fig.10 were calculated for:

ω = 3000 rad/s
δ = 0.707
K_0 = 18 Mrad/Vs
V_{CC} = 5V
f_{OUT} = 100MHz
f_{COMP} = 25kHz
G = 2

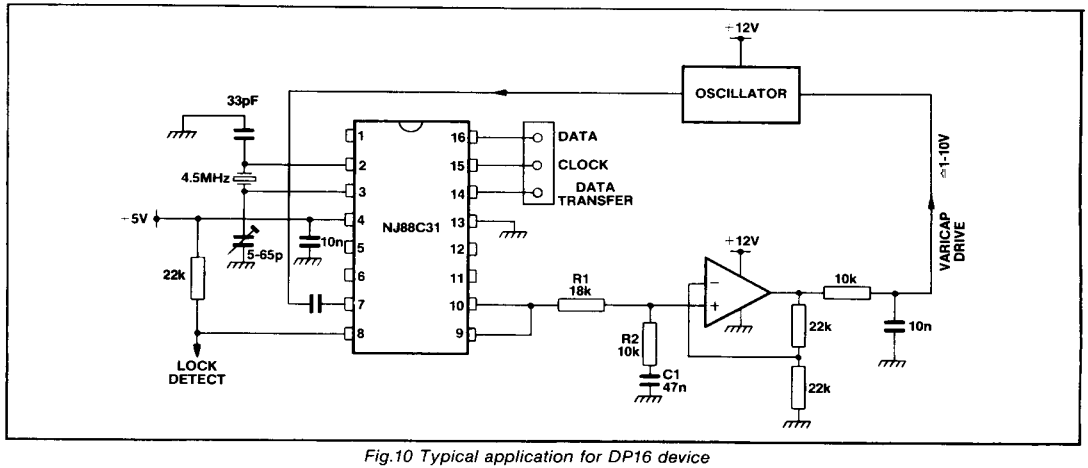

Fig.10 Typical application for DP16 device

Example of Programming

VHF section

For a channel spacing (comparison frequency) of 10kHz when using a crystal oscillator of 4.5MHz, the reference divider ratio will need to be 450 (see Fig.7). This is programmed as binary 010 in the most significant three bits of the 19 bit data word (MSB programmed first).

To obtain a VCO frequency of 125MHz the programmable divider ratio would be:

$$\frac{125 \times 10^6}{10 \times 10^3} = 12500 = 30D4 \text{ Hex.}$$

The programming word would be:

	DR			DF															
Bit No.	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Binary	0	1	0	0	0	1	1	0	0	0	0	1	1	0	1	0	1	0	0
Hex	2			3				0				D				4			

MF section

The four least significant bits of DF are not used in programming the programmable divider ratio, but nevertheless a total of 19 bits must be supplied.

For a channel spacing of 5kHz when using a crystal oscillator of 4.5MHz, the reference divider ratio will be 900 (see Fig.7). This is programmed as 110 in the most significant bits of the 19 bit word (MSB is programmed first).

To obtain a frequency of 2.5MHz the programmable divider ratio would need to be 500. The value programmed into the DP register must be the desired ratio minus one, i.e. in this case 499 which is 1F3 Hex.

The programming word would be:

	DR			DF															
Bit No.	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Binary	1	1	0	0	0	0	1	1	1	1	1	0	0	1	1	X	X	X	X
Hex	6			1				F				3				DON'T CARE			