

**Features**

- Operating voltage: 4.5V~5.5V
- ADM coding algorithm
- DRAM max. interface: 256K×4-bit or 1M×4-bit
- Built-in 2-stage microphone amplifier
- Built-in low pass filter
- Status LED indicator
- Two data rates: 24K/18K bps or bits per second (based on  $f_{OSC}=288kHz$ )
- Max. of four independent section recording capacity
- Operation mode: single-key/multi-keys
- Recorded section display

**Applications**

- Message boxes
- Recorders
- Toys

**General Description**

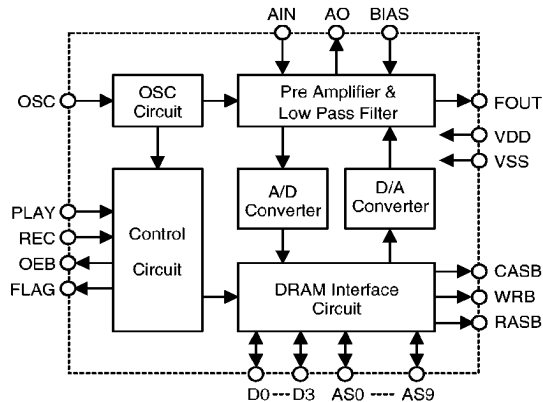
The HT8650 is a single chip CMOS LSI designed for recording applications using an ADM coding technology. It stores encoded data into external DRAMs and re-play sounds after the PLAY key is triggered.

The IC provides two kinds of key operation modes determined by the AS5 pin, namely single-key and multi-key operation modes. In the single-key operation mode, the recorded four sections of data are played sequentially by a toggle trigger. While in the multi-key operation

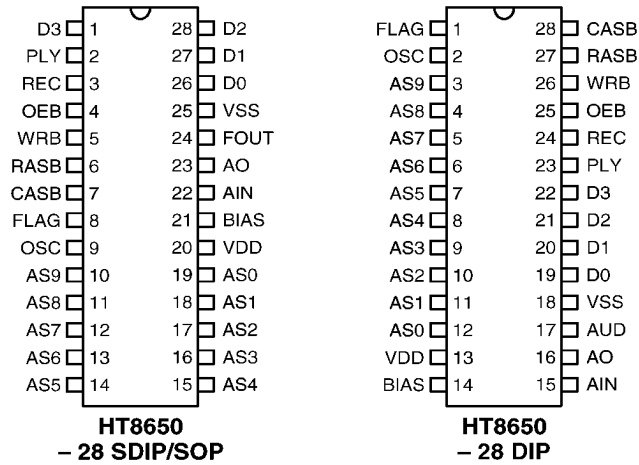
mode, the four recorded sections are played directly by the four keys provided.

Blocks within the IC include a DRAM interface circuit, signal amplifier, internal A/D and D/A and internal low pass filter. There are two sampling rates that can be selected, namely, 18K and 24K bps (based on  $f_{OSC}=288kHz$ ). Higher sampling rates result in sounds of good quality, but will shorten the recording time. In addition, few external components are required for normal applications.

**Block Diagram**

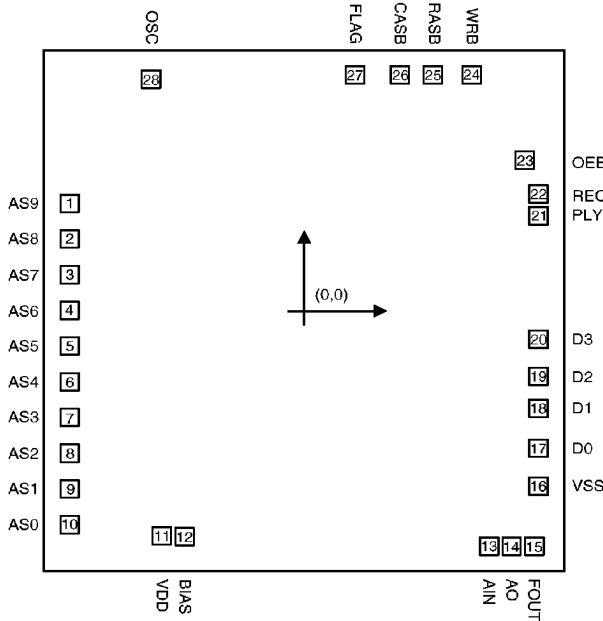


**Pin Assignment**



**Pad Coordinates**

Unit: mil



Pad No.	X	Y	Pad No.	X	Y
1	-68.55	32.98	15	67.41	-71.95
2	-68.55	22.06	16	68.55	-53.59
3	-68.55	11.13	17	68.55	-41.91
4	-68.55	0.21	18	68.55	-29.79
5	-68.55	-10.71	19	68.55	-19.98
6	-68.55	-21.63	20	68.55	-8.63
7	-68.55	-32.56	21	68.55	29.24
8	-68.55	-43.48	22	68.55	35.87
9	-68.55	-54.40	23	64.56	46.24
10	-68.55	-65.32	24	49.09	72.33
11	-41.57	-68.64	25	37.66	72.33
12	-34.94	-68.98	26	28.09	72.33
13	54.10	-71.95	27	14.88	72.33
14	60.73	-71.95	28	-44.80	71.02

Chip size: 149 × 156 (mil)<sup>2</sup>

\* The IC substrate should be connected to VDD in the PCB layout artwork.

**Pin Description (SDIP, SOP)**

Pin No.	Pad Name	I/O	Internal Connection	Description
26~28, 1	D0~D3	I/O	—	Voice data I/O pin and multi-key input
2	PLAY	I/O	NMOS Open Drain Pull-Low	Input: Play/stop trigger input, active high (refer to the functional description) Output: Multi-key common source output
3	REC	I/O	PMOS Open Drain Pull-Low	Input: Record trigger input, active high (refer to the functional description) Output: For IC test only
4	OEB	O	CMOS	DRAM output enable control pin
5	WRB	O	CMOS	Writes an enable signal output for DRAM interface
6	RASB	O	CMOS	Row address strobe output for DRAM interface
7	CASB	O	CMOS	Column address strobe output for DRAM interface
8	FLAG	I/O	NMOS Open Drain Pull-High	Input: Delete a playing section or the system resets. Active low (refer to the functional description) Output: Status indicator with an external LED to indicate an active LSI
9	OSC	I	—	Oscillator external resistor connection pin
10	AS9	I/O	CMOS Pull-High	Input: For IC test only Output: Address output specific to 1Mb DRAM
11	AS8	I/O	CMOS Pull-High	Input: For IC test only Output: Address output to DRAM
12	AS7	I/O	CMOS Pull-High	Input: For IC test only Output: Address output to DRAM
13	AS6	I/O	CMOS Pull-High	Input: DRAM type selection (refer to the functional description) Output: Address output to DRAM
14	AS5	I/O	CMOS Pull-High	Input: Key operation mode selection (refer to the functional description) Output: Address output to DRAM
15	AS4	I/O	CMOS Pull-High	Input: D3 output enable/disable selection (refer to the functional description) Output: Address output to DRAM
16	AS3	I/O	CMOS Pull-High	Input: D2 output enable/disable selection (refer to the functional description) Output: Address output to DRAM
17	AS2	I/O	CMOS Pull-High	Input: D1 output enable/disable selection (refer to the functional description) Output: Address output to DRAM

Pin No.	Pad Name	I/O	Internal Connection	Description
18	AS1	I/O	CMOS Pull-High	Input: D0 output enable/disable selection (refer to the functional description) Output: Address output to DRAM
19	AS0	I/O	CMOS Pull-High	Input: Sampling rate selection (refer to the functional description) Output: Address output to DRAM
20	VDD	I	—	Positive power supply
21	BIAS	I	—	For internal OP bias de-coupling
22	AIN	I	—	Pre-amplifier input pin
23	AO	O	—	Pre-amplifier output pin The amplifier gain is adjusted with a resistor between AIN and AO
24	FOUT	O	—	Audio signal output from an internal low pass filter
25	VSS	I	—	Negative power supply (GND)

### Absolute Maximum Ratings\*

Supply Voltage ..... -0.3V to 6V      Storage Temperature..... -50°C to 125°C  
 Input Voltage..... V<sub>SS</sub>-0.3V to V<sub>DD</sub>+0.3V      Operating Temperature..... -20°C to 70°C

\*Note: These are stress ratings only. Stresses exceeding the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

### Electrical Characteristics

 (T<sub>a</sub>=25°C)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V <sub>DD</sub>	Conditions				
V <sub>DD</sub>	Operating Voltage	—	—	4.5	5	5.5	V
I <sub>DD</sub>	Operating Current	5V	No load, f <sub>OSC</sub> =288kHz	—	180	300	μA
I <sub>STB</sub>	Standby Current	5V	—	—	50	100	μA
I <sub>OL1</sub>	FLAG Sink Current	5V	V <sub>OL1</sub> =0.5V	3	5.0	—	mA
I <sub>OL2</sub>	D0~D3 Sink Current	5V	V <sub>OL2</sub> =0.5V	3	6	—	mA
R <sub>PH</sub>	AS0~ AS9, FLAG, Pull-High Resistor	5V	—	500	1000	—	kΩ

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V <sub>DD</sub>	Conditions				
R <sub>PL</sub>	REC,PLAY Pull-Low Resistor	5V	—	300	600	—	kΩ
V <sub>OUT</sub>	Max. F <sub>OUT</sub> Output Voltage	5V	R <sub>L</sub> >50K	1.5	—	—	V <sub>P-P</sub>
T <sub>TG</sub>	Key Debounce Time	5V	f <sub>OSC</sub> =288kHz	—	30	—	ms
V <sub>IH</sub>	“H” Input Voltage	—	—	0.8V <sub>DD</sub>	—	V <sub>DD</sub>	V
V <sub>IL</sub>	“L” Input Voltage	—	—	0	—	0.2V <sub>DD</sub>	V
f <sub>OSC</sub>	Oscillating frequency	5V	R <sub>OSC</sub> =240K	—	288	—	kHz

## Functional Description

The HT8650 is a single chip LSI for message reminder applications.

The operation modes, DRAM type, sampling rate and recording sections are selected by the connections of the AS0~AS6 pins. Its audio output is filtered by an internal low pass filter to improve sound quality and to minimize external components.

### Initial setting of operation mode

The HT8650 loads the status of AS0~AS6 into a mode register after power is initially turned on or the system is reset. Its built-in pull-high resistors on AS0~AS6 define the operation mode (refer to Table 1). The two operation modes, single-key mode and multi-key mode, can be alternated by the AS5 pin.

State Bit	Functional Description	
	1	0
AS0	Data rate: 24K bps	Data rate: 18K bps
AS1	D0 (section 1) enable	D0 (section 1) not used
AS2	D1 (section 2) enable	D1 (section 2) not used
AS3	D2 (section 3) enable	D2 (section 3) not used
AS4	D3 (section 4) enable	D3 (section 4) not used
AS5	Multi-play-key mode	Single-play-key mode
AS6	DRAM type: 1Mb	DRAM type: 256Kb

Table 1

0: represents a state with an external pull-low resistor of 100kΩ on AS<sub>n</sub>

1: represents a state without an external pull-low resistor on AS<sub>n</sub>

**Single-key operation mode**

- Record function

In the single-key operation mode, the HT8650 provides two kinds of DRAM interfaces with a 4-section memory. The DRAM type and the sum of sections to be recorded are determined by the AS6 and AS1~AS4 pins, respectively. Recording will start at the first section after the REC pin is triggered. It will stop once the section capacity is full. After a section is finished recording, the system enters an idle state, and a FLAG LED flashes. To continue recording, simply press the RECORD key. The system will continue to record the next section, and so on. The linear order of section recording always follow the numerical sequence. The flashing frequency of FLAG LED corresponds with the amount of the sections recorded. For instance, FLAG LED will flash once after one section is recorded, and flash twice after two sections are recorded, etc.

The REC and PLAY trigger pins are both disabled in the process of recording until it is finished. No recording is allowed if the section capacities are all full.

Sampling Rate	DRAM Type	Capacity (secs per section)
18K bps	1Mb × 4/ 1M × 4b	56 secs/section
	256Kb × 4/ 256K × 4b	14 secs/section
24K bps	1Mb × 4/ 1M × 4b	42 secs/section
	256Kb × 4/ 256K × 4b	10.5 secs/section

- Play function

In the single-key operation mode, the numerical sequence stands for the order in which the PLAY key plays the recorded sections. The playing section will stop and its subsequent section is played if the PLAY key is pressed while a section is still playing.

- Function indicator

The FLAG pin functions not only to display

the status of the system but also delete the playing section or reset the system.

The status of the HT8650 is displayed if the FLAG pin is activated as an output.

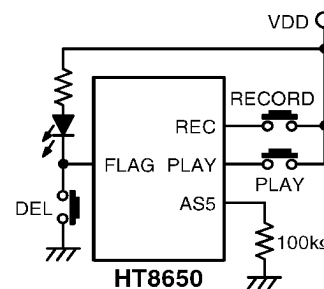
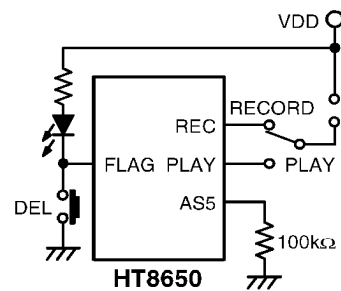
The standby, recording, playing, and sum of the recorded sections can be individually displayed on an external LED. The FLAG LED will flash for 1-second at a 4Hz rate and then is turned off after power is on or during system reset. Then, the chip will enter the standby state.

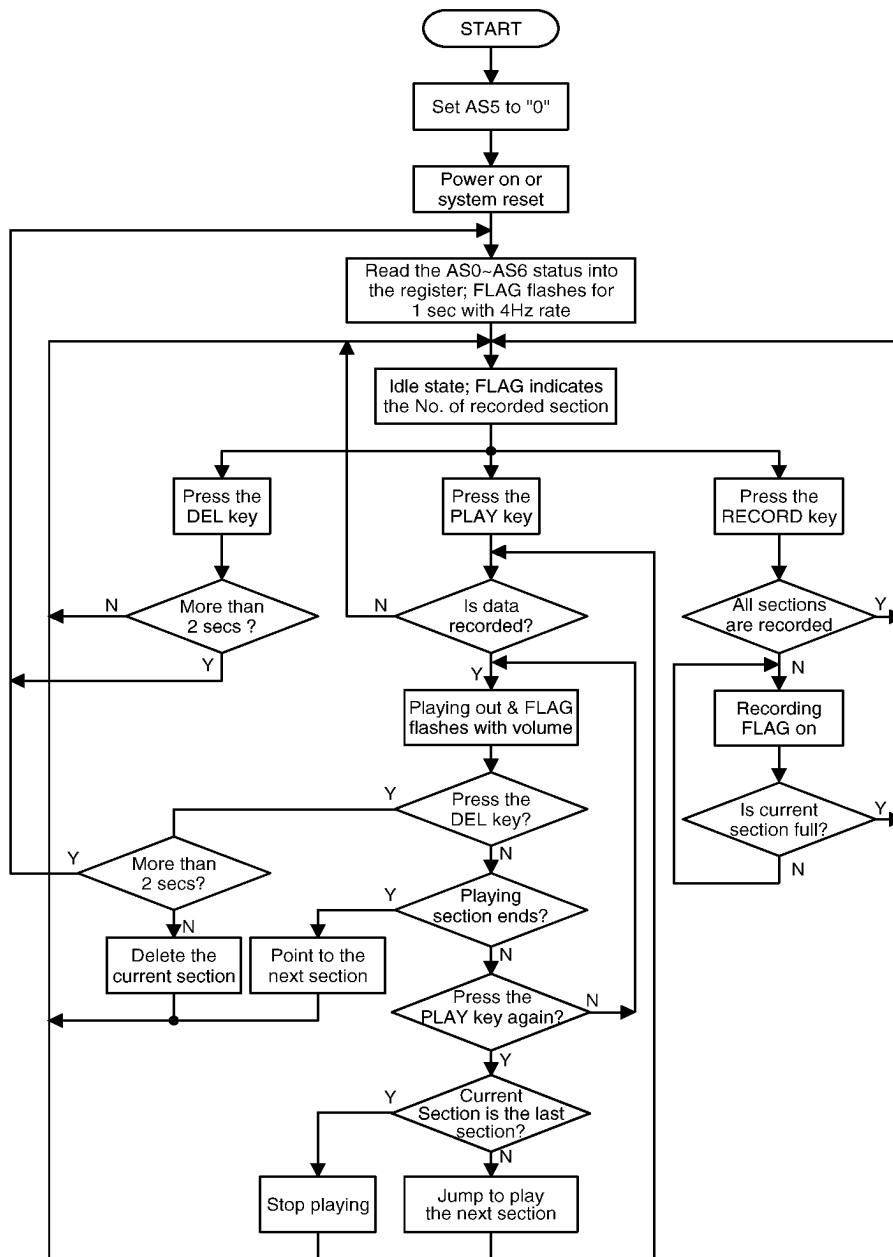
The LED is turned on during recording. Its intensity varies with the sound volume while playing. It is switched on N times within 2 seconds in the standby state if N sections have been recorded.

- Delete function

The DELETE function deletes the playing section. The playing section is deleted if the DEL key is pressed less than 2 seconds. Otherwise, the system is reset if the DEL key is pressed for more than 2 seconds.

- Application diagram & flowchart





**Multi-key operation mode**

• Record function

In the multi-key operation mode, the HT8650 also provides a 4-section memory, the same as that in the single-key operation mode. This record function is similar to the record function in the single-key operation mode, except that its FLAG LED doesn't display the numbers of the recorded sections. They are shown on the corresponding LEDs tied to the D0~D3 pins. In other words, the first LED tied to D0 flashes when the first section is recorded, the second LED tied to D1 flashes when the second section is recorded, and so on.

• Play function

The HT8650 provides four play keys to play sections. A section can be played by selecting its corresponding play key. For example, the first section is played when the first play key is pressed. The third section starts playing when the third play key is pressed, and so on. The playing section can be stopped by pressing one of the four play keys in the process of section playing. Then the section corresponding to the newly triggered key is played instead.

• STOP function

The playing section will stop immediately after the STOP key is pressed.

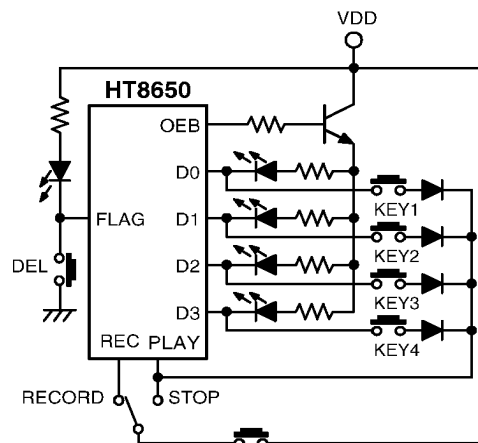
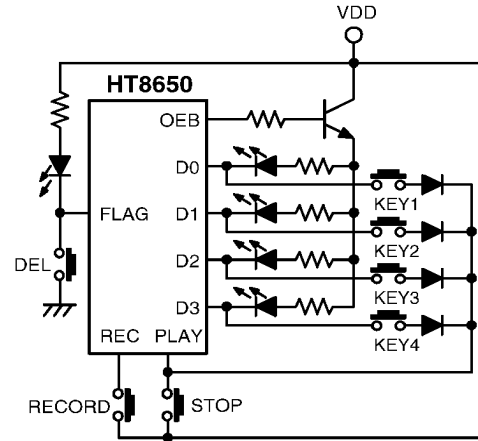
• Indicate function

The FLAG LED is turned on during recording. Its intensity varies with the sound volume while playing. After recording, i.e., in the standby state, the FLAG LED is turned off and the recorded sections are displayed on the LEDs tied to the D0~D3 pins. The LEDs on D0~D3 display the status of sections 1~4, respectively. They will flash during recording or playing. They are turned on once every 2 seconds in the idle state, indicating that a message has been recorded.

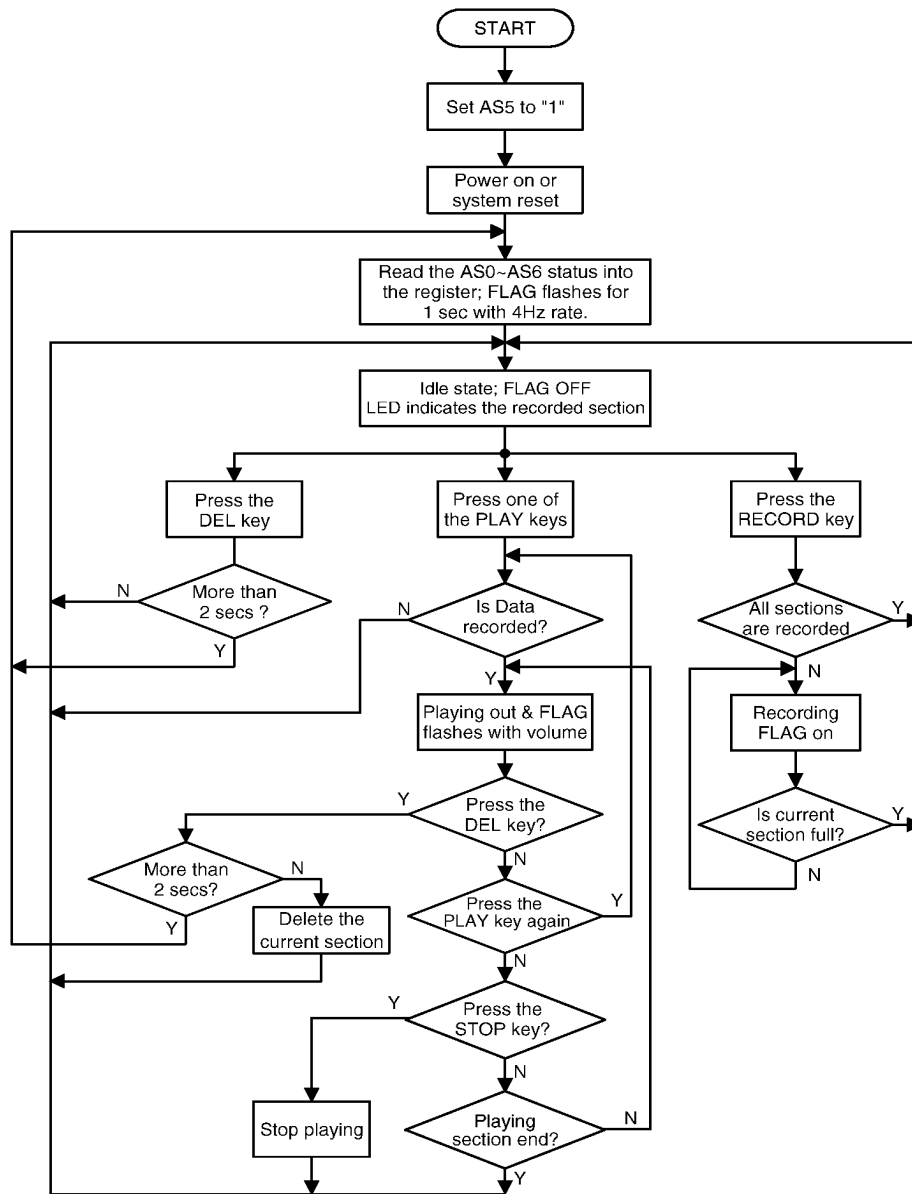
• Delete function

The DELETE function deletes the playing section. The playing section is deleted if the DEL key is pressed for less than 2 seconds. Otherwise, the system resets if the DEL key is pressed more than 2 seconds.

• Application diagram & flowchart



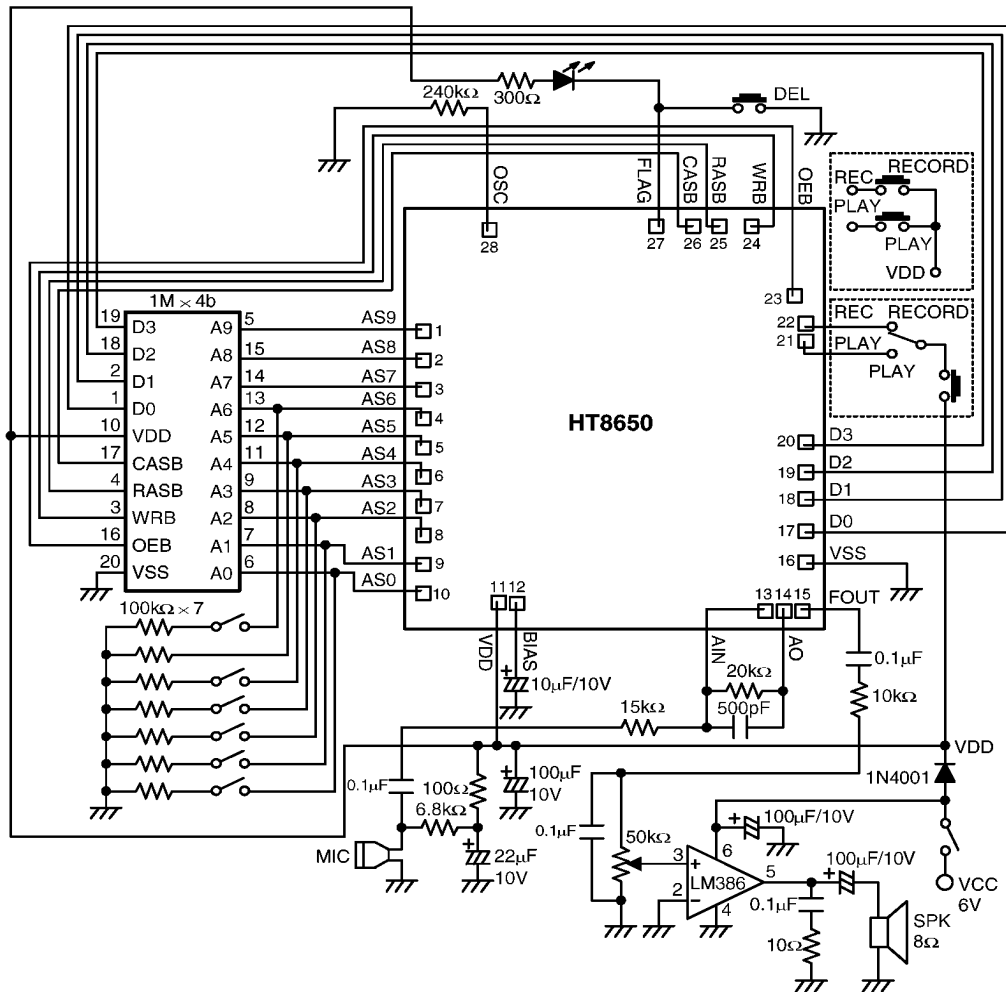




**Application Circuits**

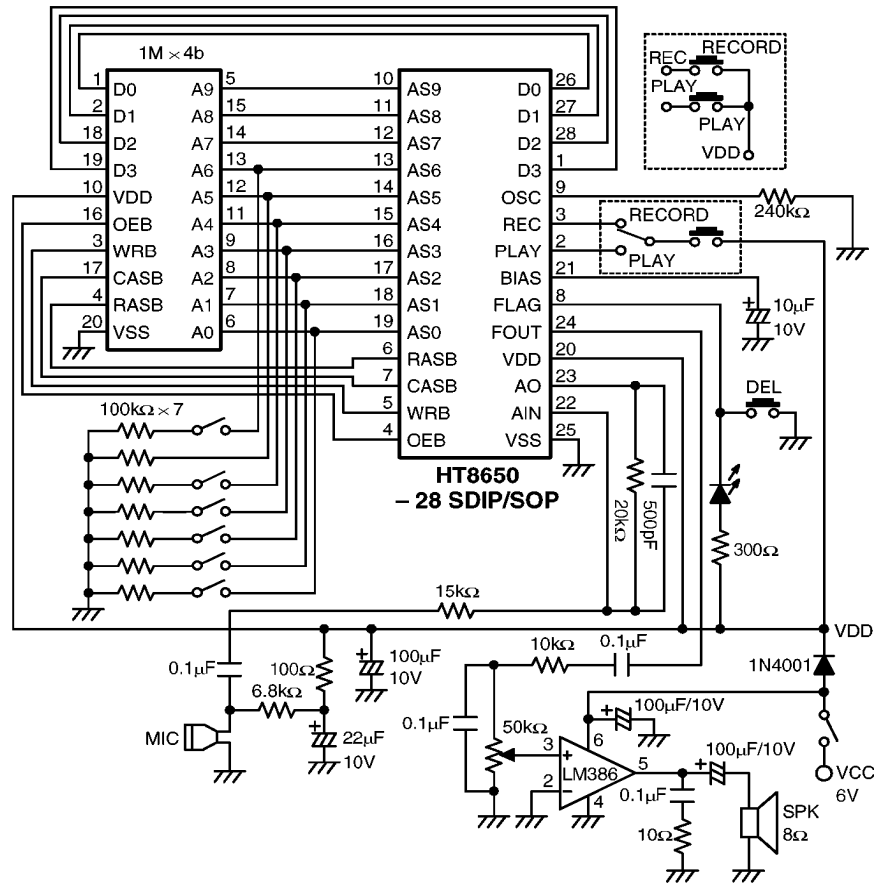
**Single-key operation mode**

- Dice form (application with 1M × 4b DRAM)



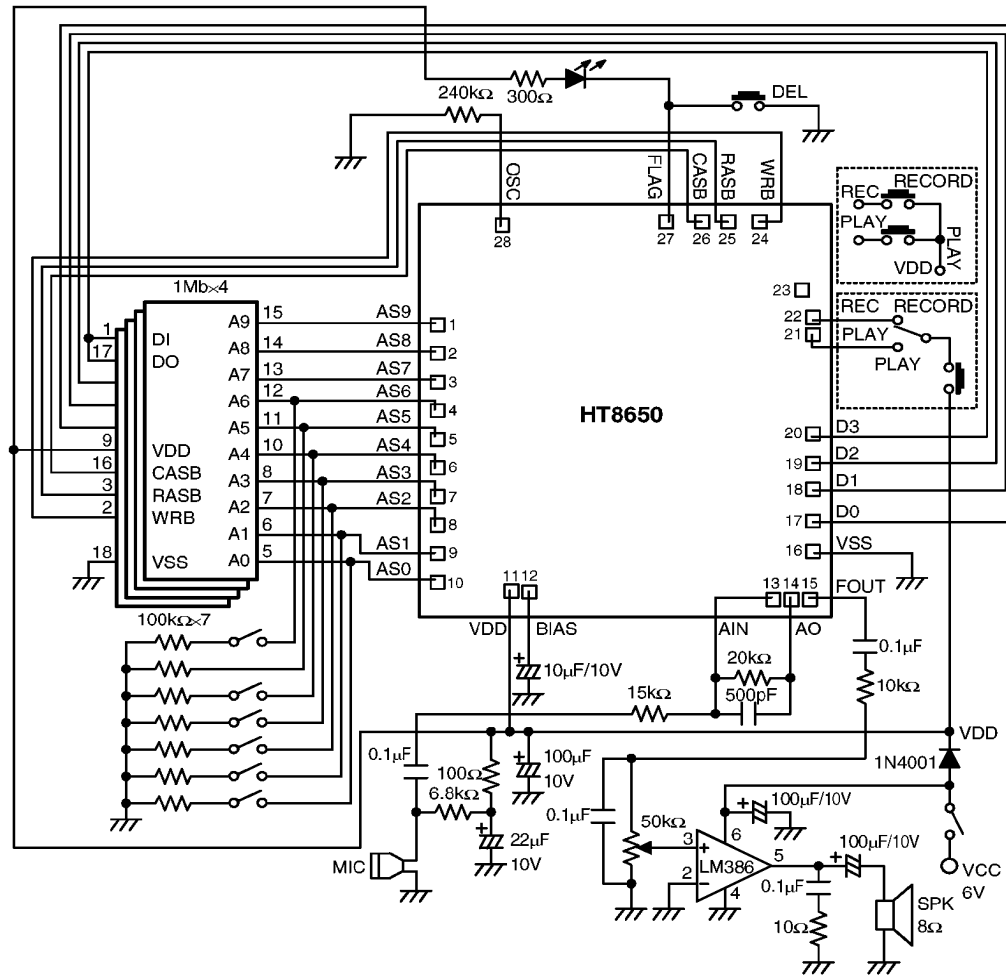
- \* The IC substrate should be connected to VDD in the PCB layout artwork
- \* The key resistance must be less than 200Ω when the DEL key is pressed
- \* The type of DRAM and the total number of sections recorded are decided by AS6 and AS1~ AS4, respectively

- Package form (application with 1M × 4b DRAM)



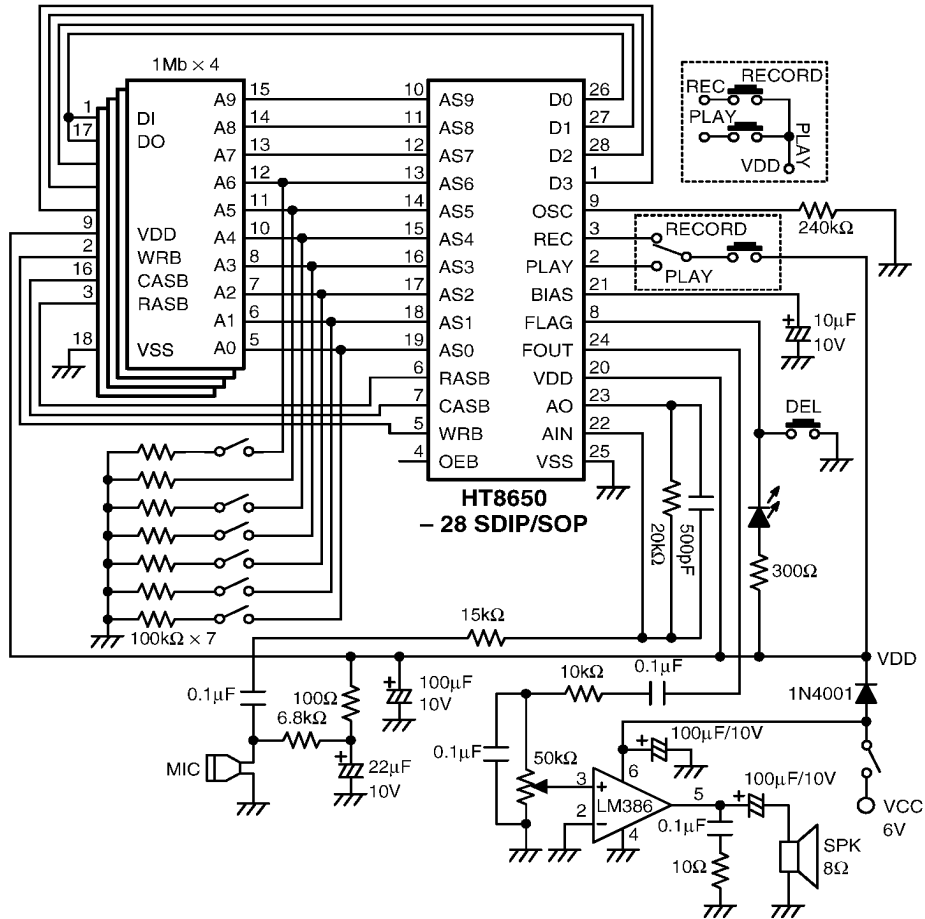
- \* The key resistance must be less than 200Ω when the DEL key is pressed.
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- Dice form (application with 1Mb × 4 DRAMs)



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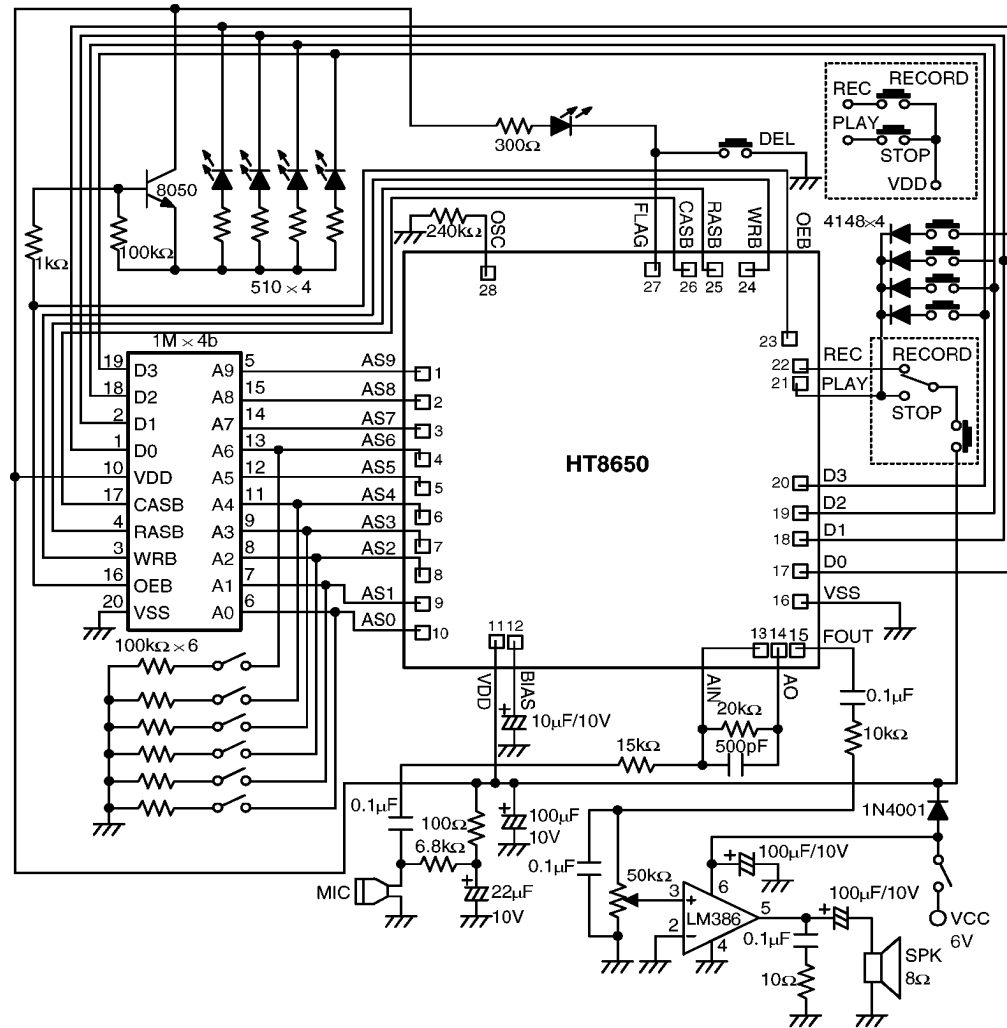
- Package form (application with 1Mb × 4 DRAMs)



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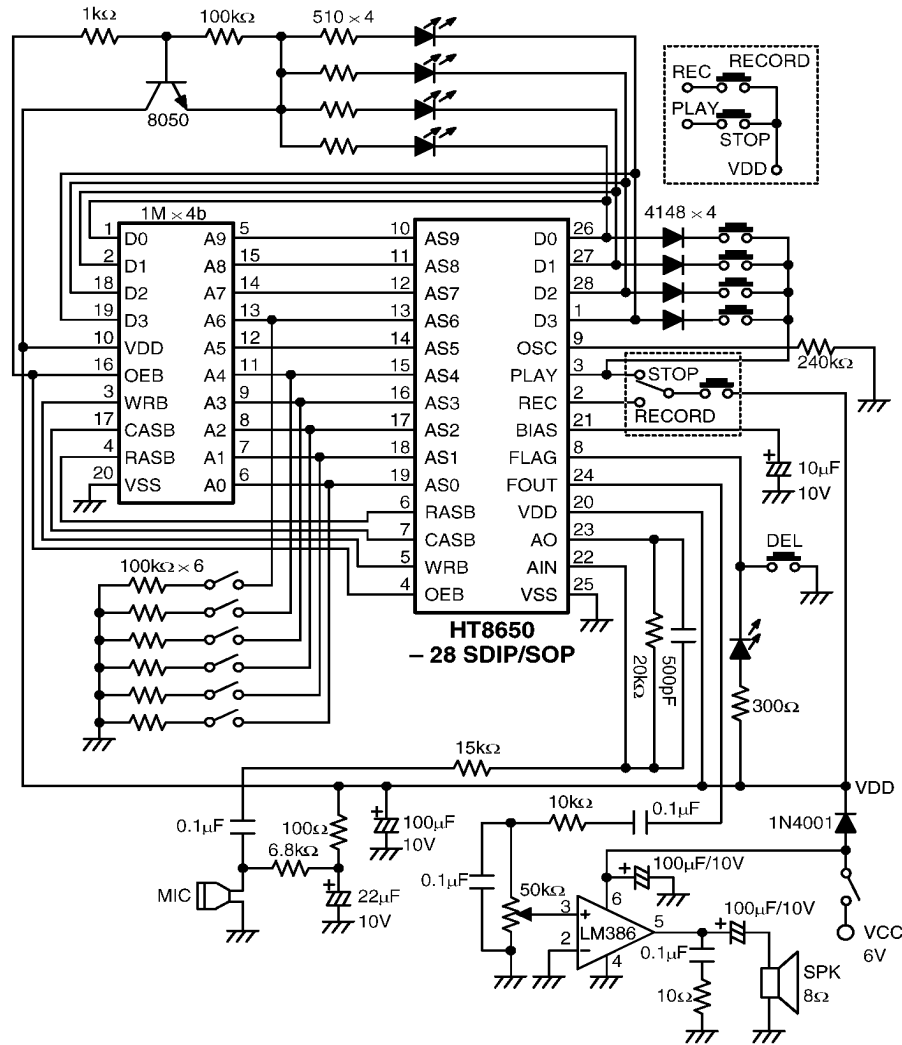
Multi-key operation mode

- Dice form (application with 1M × 4b DRAM)



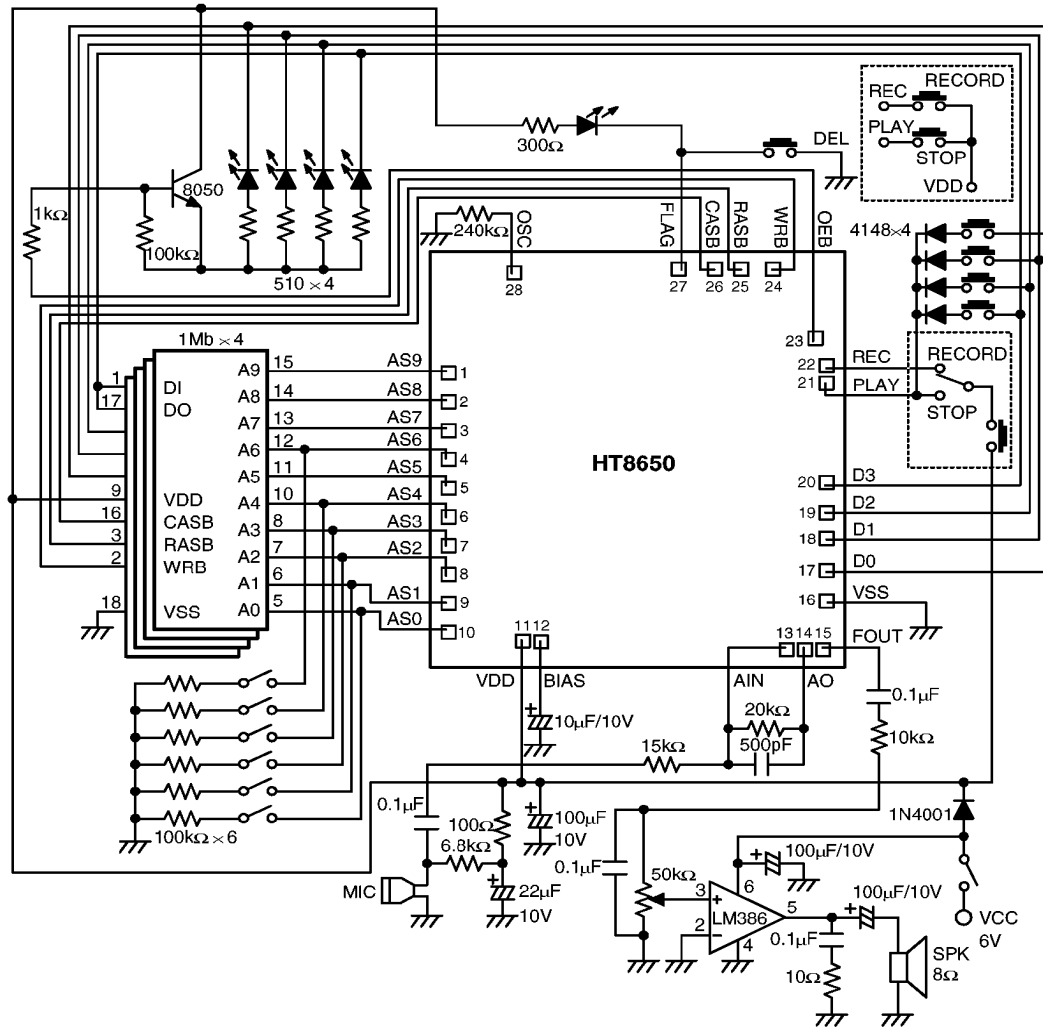
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- Package form (application with 1M × 4b DRAM)



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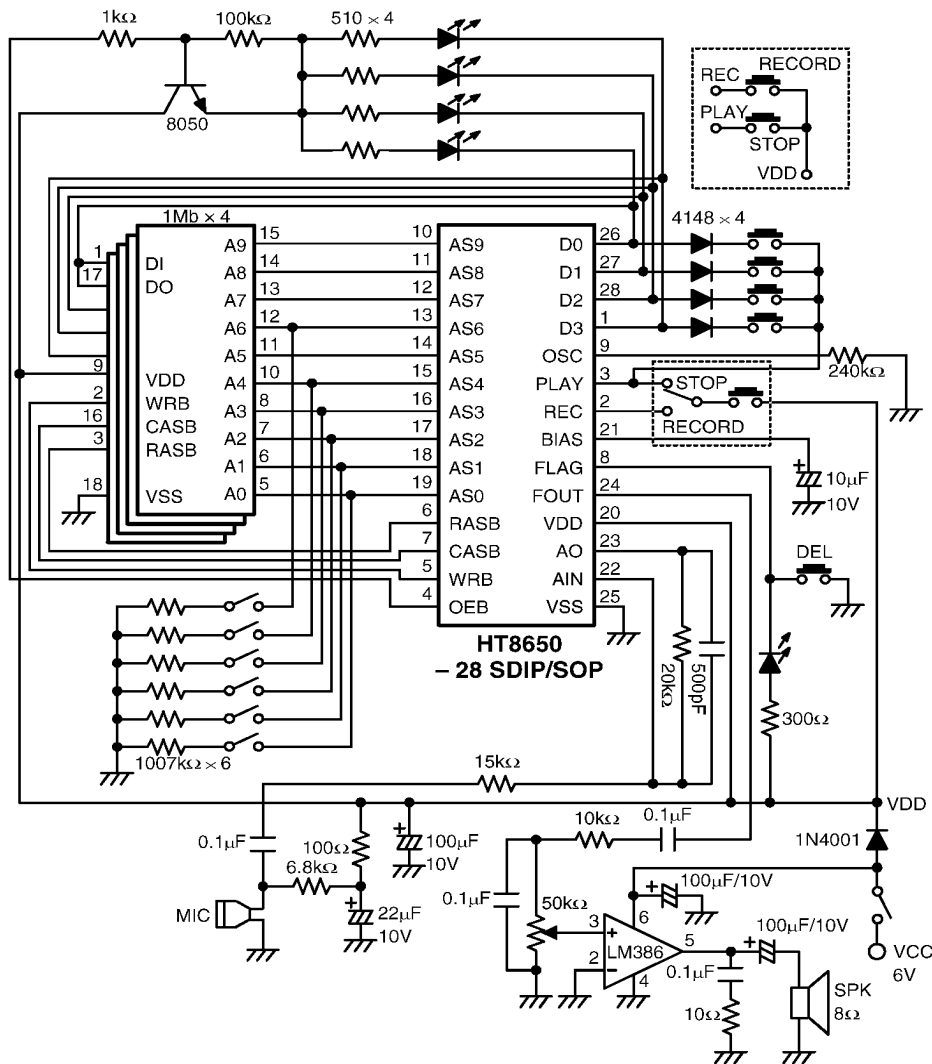
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- Package form (application with 1Mb x 4 DRAMs)



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