HB56D236 Series

2,097,152-word × 36-bit High Density Dynamic RAM Module

HITACHI

ADE-203-210 (Z)
Rev 0
Dec. 20, 1993

Description

The HB56D236 is a 2M × 36-bit dynamic RAM module, mounted 16 pieces of 4 Mbit DRAM (HM514400CS/CLS) sealed in SOJ package and 4 pieces of 2 Mbit DRAM (HM512200BS/BLS) sealed in SOJ package. An outline of the HB56D236 is 72-pin single in-line package

Therefore, the HB56D236 makes high density mounting possible without surface mount technology. The HB56D236 provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ but only on the one side of its module board.

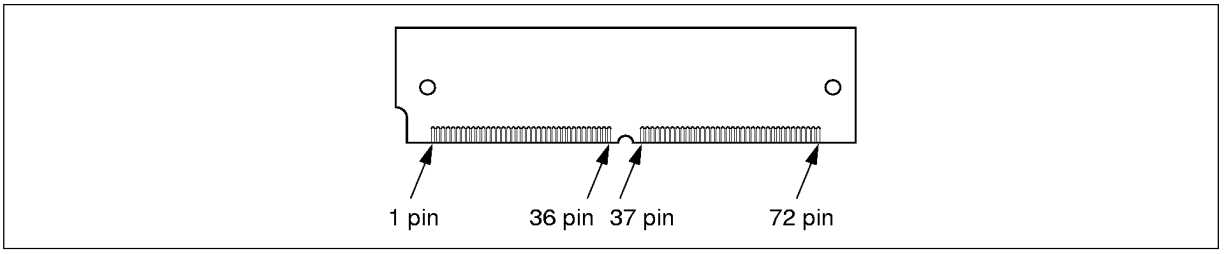
Features

- 72-pin
  - — Lead pitch: 1.27 mm
- Single 5 V (±5%) supply
- High speed
  - — Access time: 60 ns/70 ns/80 ns (max)
- Low power dissipation
  - — Active mode: 5.73 W/5.20 W/4.68 W (max)
  - — Standby mode: 210 mW (max)
    10.5 mW (max) (L-version)
- Fast page mode capability
- 1,024 refresh cycle: 16 ms
  1,024 refresh cycle: 128 ms (L-version)
- 3 variations of refresh
  - — $\overline{\text{RAS}}$ only refresh
  - — $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - — Hidden refresh
- TTL compatible

Ordering Information

Type No.	Access Time	Package	Contact Pad
HB56D236BW-6C	60 ns	72-pin SIP socket type	Gold
HB56D236BW-7C	70 ns		
HB56D236BW-8C	80 ns		
HB56D236BW-6CL	60 ns		
HB56D236BW-7CL	70 ns		
HB56D236BW-8CL	80 ns		
HB56D236SBW-6C	60 ns	72-pin SIP socket type	Solder
HB56D236SBW-7C	70 ns		
HB56D236SBW-8C	80 ns		
HB56D236SBW-6CL	60 ns		
HB56D236SBW-7CL	70 ns		
HB56D236SBW-8CL	80 ns		

Pin Arrangement



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	19	NC	37	DQ17	55	DQ12
2	DQ0	20	DQ4	38	DQ35	56	DQ30
3	DQ18	21	DQ22	39	V_{SS}	57	DQ13
4	DQ1	22	DQ5	40	$\overline{CAS0}$	58	DQ31
5	DQ19	23	DQ23	41	$\overline{CAS2}$	59	V_{CC}
6	DQ2	24	DQ6	42	$\overline{CAS3}$	60	DQ32
7	DQ20	25	DQ24	43	$\overline{CAS1}$	61	DQ14
8	DQ3	26	DQ7	44	$\overline{RAS0}$	62	DQ33
9	DQ21	27	DQ25	45	$\overline{RAS1}$	63	DQ15
10	V_{CC}	28	A7	46	NC	64	DQ34
11	NC	29	NC	47	$\overline{WE}$	65	DQ16
12	A0	30	V_{CC}	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PD1
14	A2	32	A9	50	DQ27	68	PD2
15	A3	33	$\overline{RAS3}$	51	DQ10	69	PD3
16	A4	34	$\overline{RAS2}$	52	DQ28	70	PD4
17	A5	35	DQ26	53	DQ11	71	NC
18	A6	36	DQ8	54	DQ29	72	V_{SS}

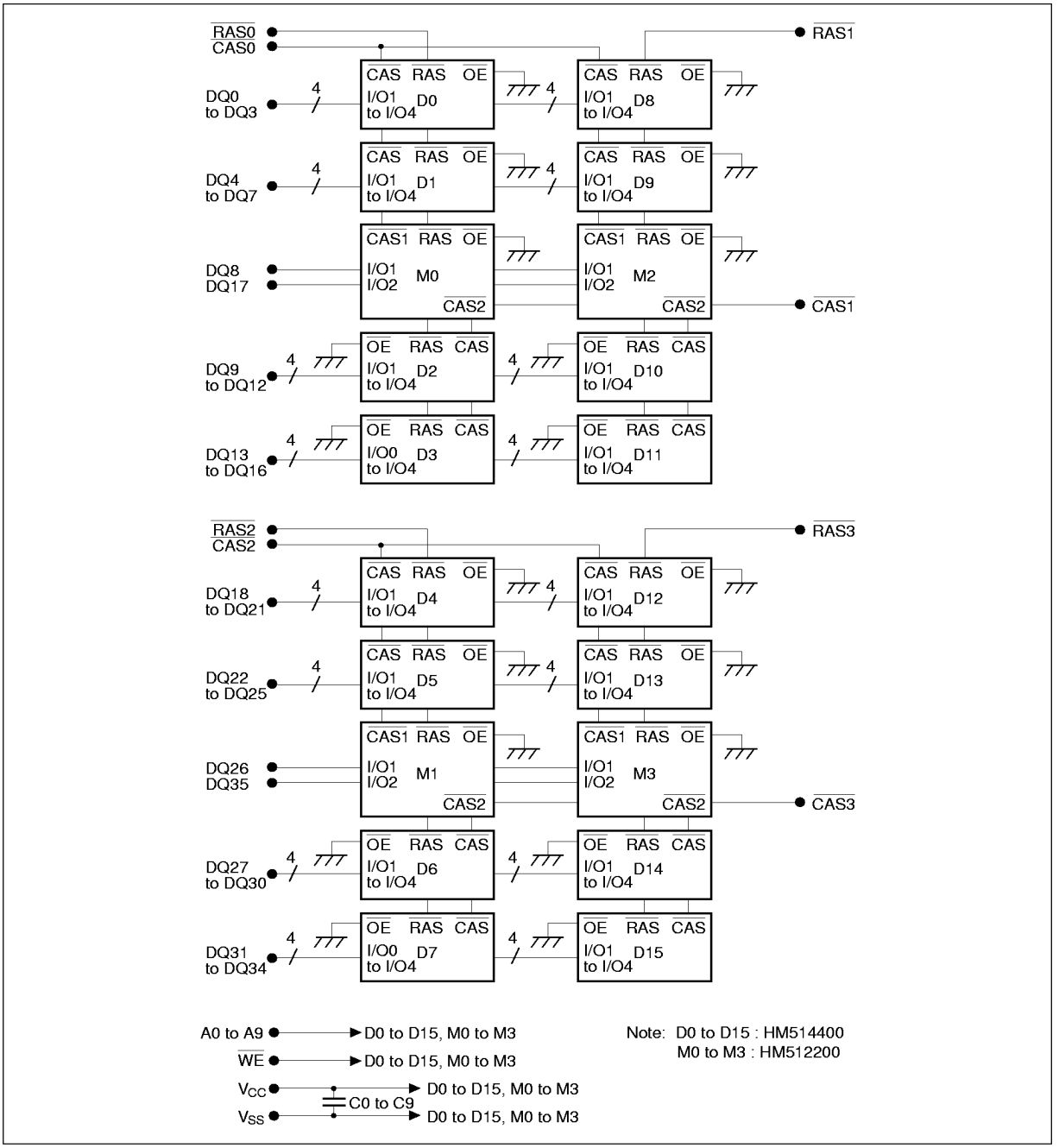
Pin Description

Pin Name	Function
A0 to A9	Address input
A0 to A9	Refresh address input
DQ0 to DQ35	Data-in/data-out
$\overline{CAS0}$ to $\overline{CAS3}$	Column address strobe
$\overline{RAS0}$ to $\overline{RAS3}$	Row address strobe
$\overline{WE}$	Read/write enable
V_{CC}	Power supply (+5 V)
V_{SS}	Ground
PD1 to PD4	Presence detect pin
NC	No connection

Presence Detect Pinout

		HB56D236		
Pin No.	Pin Name	60 ns	70 ns	80 ns
67	PD1	NC	NC	NC
68	PD2	NC	NC	NC
69	PD3	NC	V_{SS}	NC
70	PD4	NC	NC	V_{SS}

Block Diagram



Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	(Input)	Vin	–1.0 to +7.0	V
	(Output)	Vout	–1.0 to +7.0	V
Supply voltage relative to V_{SS}		V_{CC}	–1.0 to +7.0	V
Short circuit output current		Iout	50	mA
Power dissipation		P_T	10	W
Operating temperature		Topr	0 to +70	°C
Storage temperature		Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	–1.0	—	0.8	V	1

Note: 1. All voltage referred to V_{SS}

DC Electrical Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V)

		HB56D236								
		60 ns		70 ns		80 ns				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	**Notes**
Operating current	I_{CC1}	—	1090	—	990	—	890	mA	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = min	1, 2
Standby current	I_{CC2}	—	40	—	40	—	40	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	20	—	20	—	20	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
Standby current (L-version)	I_{CC2}	—	2.0	—	2.0	—	2.0	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} $\overline{WE}$, Add., Din = V_{IH} or V_{IL} Dout = High-Z	4
$\overline{RAS}$-only refresh current	I_{CC3}	—	1090	—	990	—	890	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	100	—	100	—	100	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	1090	—	990	—	890	mA	t_{RC} = min	
First page mode current	I_{CC7}	—	1050	—	950	—	850	mA	t_{PC} = min	1, 3
Battery backup operating current (Standby with CBR refresh) (L-version)	I_{CC10}	—	4.0	—	4.0	—	4.0	mA	t_{RC} = 125 µs t_{RAS} ≤ 1 µs $\overline{WE}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Add., Din = V_{IH} or V_{IL} Dout = High-Z	4
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. V_{CC} – 0.2 V ≤ V_{IH} ≤ 6.5 V and 0 ≤ V_{IL} ≤ 0.2 V.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 5%)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	130	pF	1
Input capacitance ($\overline{WE}$)	C_{I2}	—	165	pF	1
Input capacitance ($\overline{RAS}$)	C_{I3}	—	50	pF	1
Input capacitance ($\overline{CAS}$)	C_{I3}	—	57	pF	1
I/O capacitance (DQ)	$C_{I/O}$	—	24	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V)[*1, *14, *15, *16]

Read, Write and Refresh Cycle (Common parameters)

		HB56D236							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t_{RC}	110	—	130	—	150	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	40	—	50	—	60	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	80	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10000	20	10000	20	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	8
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	9
$\overline{RAS}$ hold time	t_{RSH}	15	—	20	—	20	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	60	—	70	—	80	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	ns	
$\overline{CAS}$ setup time from Din	t_{DZC}	0	—	0	—	0	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	7
Refresh period	t_{REF}	—	16	—	16	—	16	ms	19
Refresh period (L-version)	t_{REF}	—	128	—	128	—	128	ms	19

Read Cycle

		HB56D236							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	ns	2, 3, 17
Access time from $\overline{CAS}$	t_{CAC}	—	15	—	20	—	20	ns	3, 4, 13, 17
Access time from address	t_{AA}	—	30	—	35	—	40	ns	3, 5, 13, 17
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	18
Read command hold time to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	18
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	—	35	—	40	—	ns	
Output buffer turn-off time	t_{OFF1}	0	15	0	20	0	20	ns	6
$\overline{CAS}$ to Din delay time	t_{CDD}	15	—	20	—	20	—	ns	

Write Cycle

		HB56D236							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	10
Write command hold time	t_{WCH}	15	—	15	—	15	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	10	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in hold time	t_{DH}	15	—	15	—	15	—	ns	11

Refresh Cycle

		HB56D236							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	ns	
$\overline{CAS}$ precharge time in normal mode	t_{CPN}	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

		HB56D236							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Fast page mode cycle time	t_{PC}	40	—	45	—	50	—	ns	
Fast page mode $\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	10	—	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASC}	—	100000	—	100000	—	100000	ns	12
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	35	—	40	—	45	ns	3, 13, 17
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35	—	40	—	45	—	ns	

Test Mode Cycle

		HB56D236							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Test mode $\overline{WE}$ setup time	t_{WS}	0	—	0	—	0	—	ns	
Test mode $\overline{WE}$ hold time	t_{WH}	10	—	10	—	10	—	ns	

Counter Test Cycle

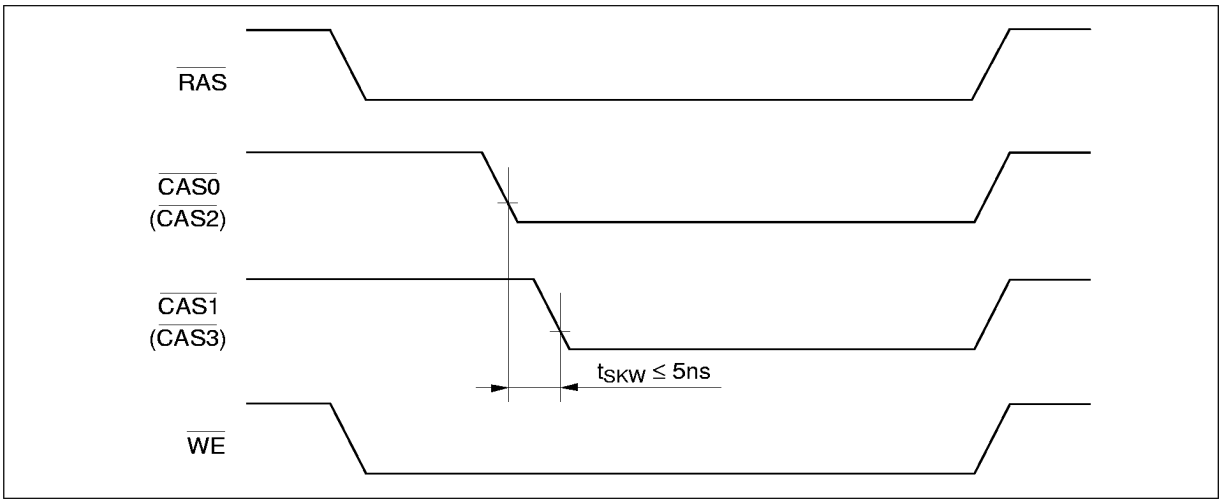
		HB56D236							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ precharge time in counter test cycle	t_{CPT}	40	—	40	—	40	—	ns	

Notes:
1. AC measurements assume t_T = 5 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referred to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operating with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS} is not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is on early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referred to $\overline{CAS}$ leading edge in an early write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh cycles or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle is required.
15. $\overline{CAS0}$ and $\overline{CAS1}$ or $\overline{CAS1}$ and $\overline{CAS2}$ cannot be staggered within the same write/read cycles.
16. Test mode operation specified in this data sheet is 2-bit test function controlled by control address bits ... CA0. This test mode operation can be performed by $\overline{WE}$-and-$\overline{CAS}$-before-$\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of two test bits accord, each other, the condition of the output data is high level. When the state of the test bits do not accord, the condition of the output data is low level. In order to end this test mode operation, perform a $\overline{RAS}$-only refresh cycle or a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.
17. In a test mode read cycle the value of t_{RAC}, t_{AA}, t_{CAC}, t_{OAC} and t_{ACP} is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycle by adding the above value to the specified value in this data sheet.
18. Either t_{RCH} or t_{RRH} must be satisfied.
19. t_{REF} is determined by 1,024 refresh cycles.

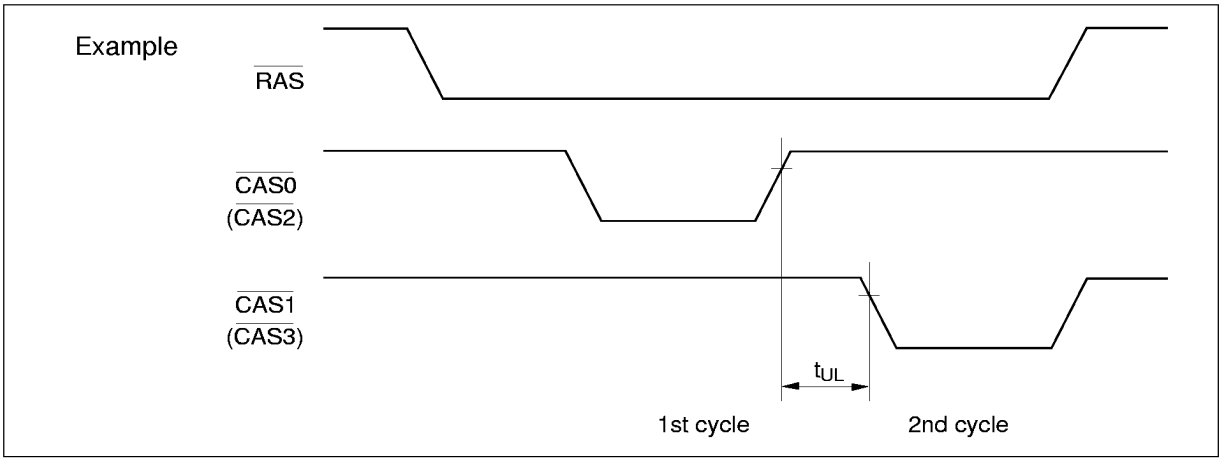
Notes on 2$\overline{CAS}$ control

(1) In one memory cycle, activate both of 2$\overline{CAS}$s ($\overline{CAS0}$ and $\overline{CAS1}$, or $\overline{CAS2}$ and $\overline{CAS3}$) or only one of them or neither of them.

(2) To activate both of 2$\overline{CAS}$s in an early write cycle or a page mode early write cycle, please keep t_{SKW} (skew between $\overline{CAS0}$ and $\overline{CAS1}$, or $\overline{CAS2}$ and $\overline{CAS3}$) 5 ns or less.



(3) If the different $\overline{CAS}$s are activated in the consecutive page cycles, t_{UL}, the period that both $\overline{CAS}$s are high, should be keep t_{CP} spec (t_{CP} min ≤ t_{UL}).



Timing Waveforms

- Refer to the HM514400C Series data sheet.
- The HB56D236BW/SBW writes data only in early write cycle ($t_{WCS} \geq t_{WCS}$ (min)).
  Delayed write cycle is not available ($\overline{OE}$ pin is fixed to V_{SS}).

Physical Outline

Unit: mm/inch